





N-Channel Enhancement Mode MOSFET

CDM301N



SOT-23

SOT-23 Surface Mount Plastic Package RoHS compliant

General Description:

This N-Channel logic level enhancement mode field effect transistor, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. This device has been designed especially for low voltage applications as a replacement for digital transistors. Since bias resistors are not required, this one N-channel FET can replace several different digital transistors, with different bias resistor values.

FEATURE

1. 25V, 0.22A continuous, 0.5A Peak

 $R_{DS(ON)} = 5\Omega @ V_{GS} = 2.7V$

 $R_{DS(ON)} = 4\Omega @ V_{GS} = 4.5V$

- 2. Very low level gate drive requirements allowing direct operation in 3V circuits. VGS(th) < 1.06V.
- 3. Gate-Source Zener for ESD ruggedness. >6kV Human Body Model.
- 4. Replace multiple NPN digital transistors with one DMOS FET.

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Parameter	SYMBOL	VALUE	UNIT
Drain-Source Voltage, Power Supply Voltage	V_{DSS}, V_{CC}	25	V
Gate-Source Voltage, VIN	V_{GSS}, V_{I}	8	V
Drain/Output Current - Continuous	1 1	0.22	Α
Drain/Output Current -Pulsed	I _D , I _O	0.5	Α
Maximum Power Dissipation	P_{D}	0.35	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C
Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100pf / 1500 Ohm)	ESD	6.0	kV

Thermal Resistance

Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	357	°C/W







ELECTRICAL CHARACTERISTICS at $T_a = 25$ °C

Parameter	Symbol	Test Condition	Min	Тур.	Max	Unit	
Zero Input Voltage Output Current	I _{O(off)}	$V_{CC} = 20V, V_{I} = 0V$			1	μΑ	
In and Malla and	$V_{I(off)}$	$V_{CC} = 5V, I_{O} = 10\mu A$			0.5	V	
Input Voltage	$V_{I(on)}$	$V_{\rm O} = 0.3 \text{V}, I_{\rm O} = 0.005 \text{A}$	1			V	
Output to Ground Resistance	R _{O(on)}	$V_1 = 2.7V, I_0 = 0.2A$	-	4	5	Ω	
Off Characteristics							
Drain-Source Breakdown Voltage	V _{(BR)DSS}	VGS = 0V, ID = 250µA	25			V	
Breakdown Voltage Temp. Coefficient	$\Delta BV_{DSS/}$ ΔT_J	Reference to 25°C, I _D = 250µA		25		mV/°C	
		VDS = 20V, VGS = 0V			1.0	μA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =20V, V _{GS} =0V,T _J =55°C	-		10	μA	
Gate-body Leakage current	I _{GSS}	$V_{DS} = 0V$, $V_{GS} = 8V$			100	nA	
On Characteristics ¹							
Gate-Threshold Voltage	VGS(th)	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	0.70	0.85	1.06	V	
VGS(th) Temperature Coefficient	$\Delta V_{GS(th)/}$ ΔT_{J}	Reference to 25 °C, I _D = 250µA		-2.1		mV/°C	
	J	$V_{GS} = 2.7V, I_D = 0.2A$		3.8	5		
Orain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 4.5V, I_D = 0.4A$		3.1	4	Ω	
	(,	V _{GS} =2.7V,I _D =0.2A,T _{i=} 125°C		6.3	9		
On–State Drain Current	I _{D(on)}	$V_{GS} = 2.7V, V_{DS} = 5V$	0.2			Α	
Forward Trans conductance	gf _s	$V_{DS} = 5V, I_{D} = 0.4A$		0.2		S	
Dynamic Characteristics							
Input Capacitance	C_{iss}	V _{GS} = 4.5V	-	9.5			
Output Capacitance	C _{oss}	V _{DS} = 10V		6		рF	
Reverse Transfer Capacitance	C_{rss}	f = 1.0MHz		1.3			
Switching Characteristics ¹							
Total Gate Charge	Q_g	V _{DS} =4.5V,		0.49	0.7		
Gate-Source Charge	Q_gs	I _D =0.2A,	-	0.22		nC	
Gate-Drain Charge	Q_{gd}	V _{GS} =5V		0.07			
Turn-On Delay Time	t _{d(on)}			3.2	8		
Rise Time	t _r	V _{DD} =6V, I _D =0.5A,		6	15	-	
Turn-Off Delay Time	$t_{d(off)}$	R_{GEN} = 50 Ω , V_{GS} = 4.5 V	-	3.5	8	ns	
Fall Time	t _f			3.5	8		
Drain-Source Diode Characteristics and	l Maximum	Ratings					
Maximum Continuous Drain-Source Diode Forward Current	I _S				0.29	Α	
Drain–Source Diode Forward Voltage	V_{SD}	I _S =0.29A, V _{GS} =0V ¹		0.8	1.2	V	

Note:

1. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

CDM301N







Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

(C)

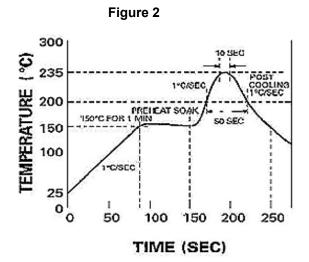
Max 260°C — 40 secs. maximum
Typical 245°C — 3 x reflow

217°C — 210°C — 70 Hosting Zooe

Fro Hosting Zooe

60-190s

Heating time



Reflow profiles in tabular form

Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat - Temperature Range - Time	150-170°C 60-180 seconds	150-200°C 60-180 seconds
Time maintained above: – Temperature – Time	200°C 30-50 seconds	217°C 60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.

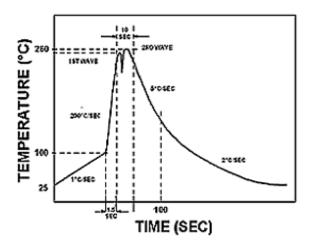




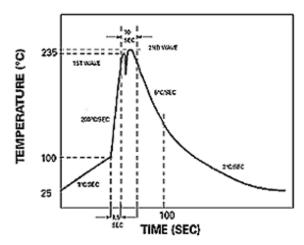


Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used



The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder



Wave Profiles in Tabular Form

Profile Feature	Sn-Pb System	Pb-Free System		
Average Ramp-Up Rate	~200°C/second	~200°C/second		
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec		
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp		
Peak Temperature	235°C	260°C max.		
Time within +0 -5°C of actual Peak	10 seconds	10 seconds		
Ramp-Down Rate	5°C/second max.	5°C/second max		







Typical Characteristic Curves

Fig 1: On-Region Characteristics

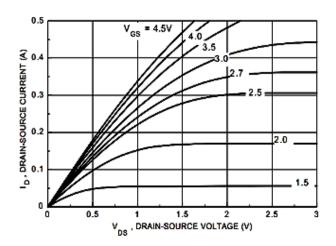


Fig 2: On-Resistance Variation With Temperature

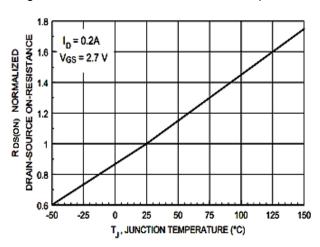


Fig 3: Transfer Characteristics

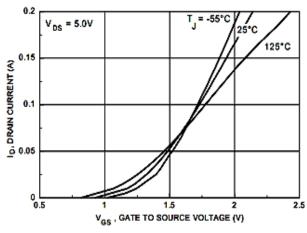


Fig 4: On-Resistance Variation With Drain Current and Gate Voltage

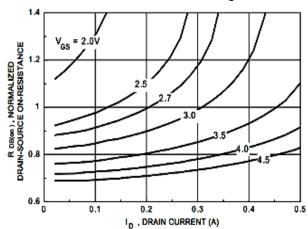


Fig 5:On-Resistance Variation With Gate-to-Source Voltage

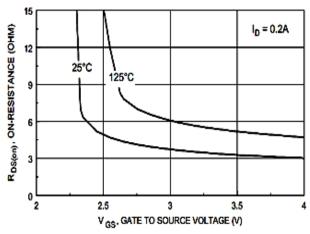
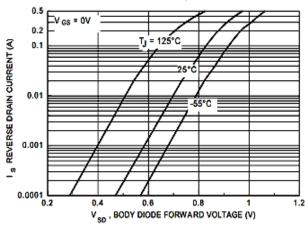


Fig 6: Body Diode Forward Voltage Variation With Source Current Temperature









Typical Characteristic Curves

Fig 7: Gate-Charge Characteristics V_{DS} = 5V I_D = 0.2A 15V

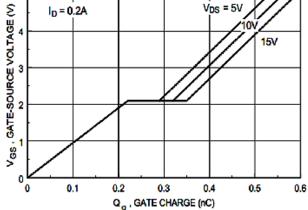


Fig 8: Maximum safe Operating Area

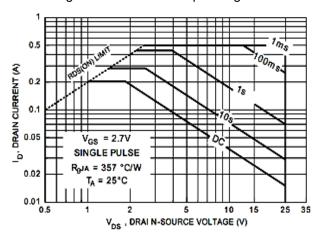


Fig 9: Capacitance Characteristics

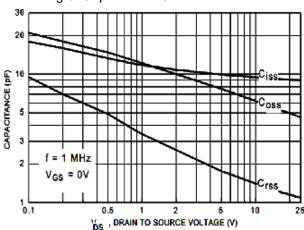


Fig 10: Single Pulse Maximum Power Dissipation

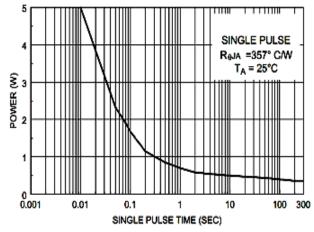
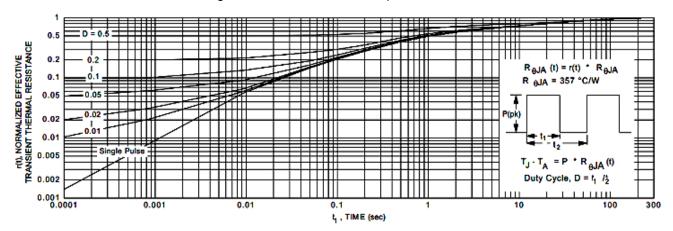


Fig 11: Transient Thermal Response Curve



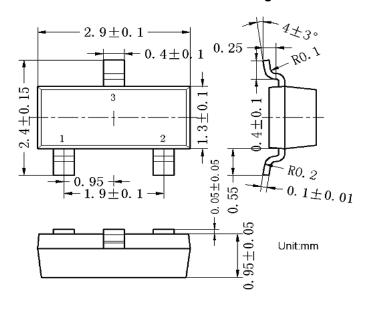






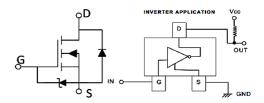
PACKAGE DETAILS

SOT-23 Formed SMD Package

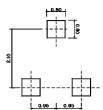


Pin configuration

- 1. Gate
- 2. Source
- 3. Drain



Recommend PCB solder land [Unit: mm]

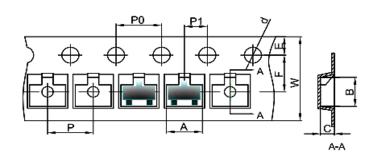








SOT-23 Embossed Carrier Tape

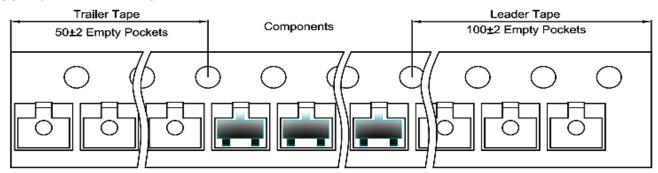


Packaging Description:

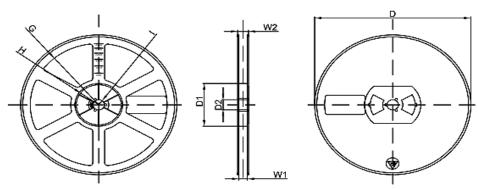
SOT-23 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resln. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 3,000 units per 7" or 17.8cm diameter reel. The reels are clear in color and is made of polystyrene plastic (anti-static coated).

Dimensions are in millimeter										
Pkg type	Α	В	С	d	E	F	P0	Р	P1	W
SOT-23	3.15	2.77	1.22	Ø1.50	1.75	3.50	4.00	4.00	2.00	8.00

SOT-23 TAPE LEADER & TRAILAR



SOT-23 REEL



Dimensions are in millimeter								
Reel Option	D	D1	D2	G	Н	_	W1	W2
7"Dia	Ø178.00	54.40	13.00	R78.00	R25.60	R6.50	9.50	12.30

REEL	Reel Size	Box	Box Size(mm)	Carton	Carton Size(mm)	G.W.(kg)
3000 pcs	7 Inch	45,000 pcs	203×203×195	180,000 pcs	438×438×220	

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Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by Akyga Semi.

- · Temperature 5 °C to 30 °C
- · Humidity between 40 to 70 %RH
- · Air should be clean.
- · Avoid harmful gas or dust.
- · Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- · Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- · Avoid rapid change of temperature.
- · Avoid condensation.
- · Mechanical stress such as vibration and impact shall be avoided.
- · The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.

If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per Akyga Semi quality procedure.

The products are further warranted for another one year after the date of shipment subject to the above conditions in Akyga Semi original packing.

Floor Life of and MSL Level

When the products are opened from the original packing, the floor life will start.

For this, the following JEDEC table may be referred:

	JEDEC MSL Level					
Level	Time	Condition				
1	Unlimited	≤30 °C / 85% RH				
2	1 Year	≤30 °C / 60% RH				
2a	4 Weeks	≤30 °C / 60% RH				
3	168 Hours	≤30 °C / 60% RH				
4	72 Hours	≤30 °C / 60% RH				
5	48 Hours	≤30 °C / 60% RH				
5a	24 Hours	≤30 °C / 60% RH				
6	Time on Label(TOL)	≤30 °C / 60% RH				







Customer Notes

Component Disposal Instructions

- 1. Akyga Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
- 2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the Akyga's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the Akyga Web Site/CD are believed to be accurate and reliable. Akyga however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, Akyga does not assume liability whatsoever, arising out of the application or use of any Akyg product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. Akyga customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and Akyga will not be responsible for any damages resulting from such sale(s).

Akyga strives for continuous improvement and reserves the right to change the specifications of its products without prior notice.