



PRELIMINARY

CY62148

512K x 8 Static RAM

Features

- 4.5V–5.5V operation
- CMOS for optimum speed/power
- Low active power
— 660 mW (max.)
- Low standby power (L version)
— 2.75 mW (max.)
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with CE and OE options

Functional Description

The CY62148 is a high-performance CMOS static RAM organized as 524,288 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}), an active LOW output enable (\overline{OE}), and three-state drivers. This device has

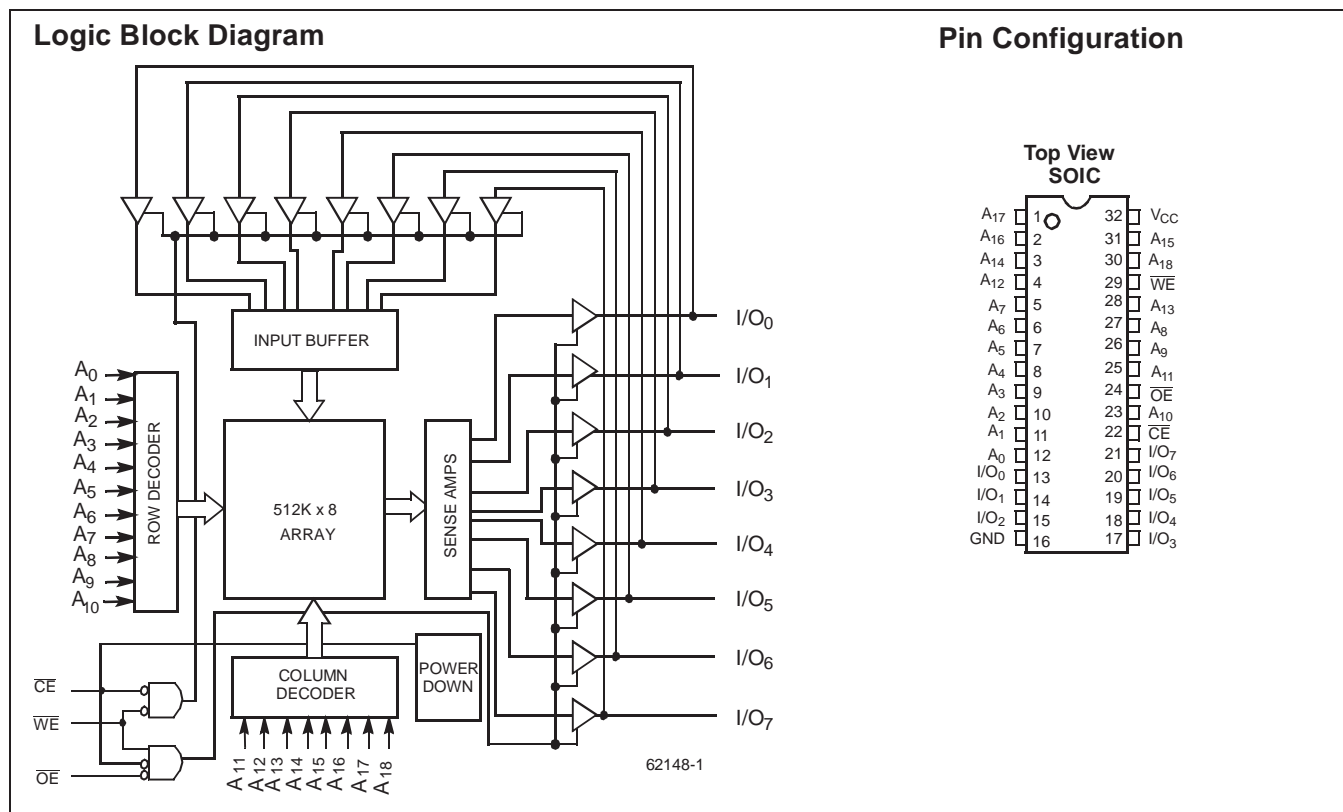
an automatic power-down feature that reduces power consumption by more than 99% when deselected.

Writing to the device is accomplished by taking chip enable one (\overline{CE}) and write enable (\overline{WE}) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

Reading from the device is accomplished by taking chip enable one (\overline{CE}) and output enable (\overline{OE}) LOW while forcing write enable (\overline{WE}). Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE} LOW, and \overline{WE} LOW).

The CY62148 is available in a standard 450-mil-wide body width SOIC package.



Selection Guide

| | | CY62148-55 | CY62148-70 |
|------------------------------|--|------------|------------|
| Maximum Access Time (ns) | | 55 | 70 |
| Maximum Operating Current | | Commercial | 120 mA |
| Maximum CMOS Standby Current | | Commercial | 2 mA |
| | | L | 0.5 mA |

Shaded areas contain advance information



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied..... -55°C to +125°C

Supply Voltage on V_{CC} to Relative GND^[1] -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State^[1] -0.5V to V_{CC} +0.5V

DC Input Voltage^[1] -0.5V to V_{CC} +0.5V

Current into Outputs (LOW) 20 mA

Operating Range

| Range | Ambient Temperature ^[2] | V _{CC} |
|------------|------------------------------------|-----------------|
| Commercial | 0°C to +70°C | 5V ± 10% |
| Industrial | -40°C to +85°C | 5V ± 10% |

Electrical Characteristics Over the Operating Range^[3]

| Parameter | Description | Test Conditions | 62148-55 | | 62148-70 | | Unit |
|------------------|---|---|----------|----------------------|----------|----------------------|------|
| | | | Min. | Max. | Min. | Max. | |
| V _{OH} | Output HIGH Voltage | V _{CC} = Min., I _{OH} = -1 mA | 2.4 | | 2.4 | | V |
| V _{OL} | Output LOW Voltage | V _{CC} = Min., I _{OL} = 2.1 mA | | 0.4 | | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | 2.2 | V _{CC} +0.3 | 2.2 | V _{CC} +0.3 | V |
| V _{IL} | Input LOW Voltage ^[1] | | -0.3 | 0.8 | -0.3 | 0.8 | V |
| I _{IX} | Input Load Current | GND ≤ V _I ≤ V _{CC} | -1 | +1 | -1 | +1 | μA |
| I _{OZ} | Output Leakage Current | GND ≤ V _I ≤ V _{CC} , Output Disabled | -5 | +5 | -5 | +5 | μA |
| I _{CC} | V _{CC} Operating Supply Current | V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC} | | 120 | | 120 | mA |
| I _{SB1} | Automatic CE Power-Down Current — TTL Inputs | Max. V _{CC} , CE ≥ V _{IH} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX} | | 15 | | 15 | mA |
| I _{SB2} | Automatic CE Power-Down Current — CMOS Inputs | Max. V _{CC} , CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f=0 | | 2 | | 2 | mA |
| | | | L | 500 | | 500 | μA |

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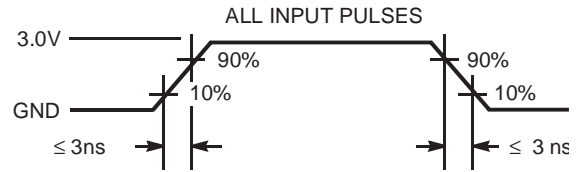
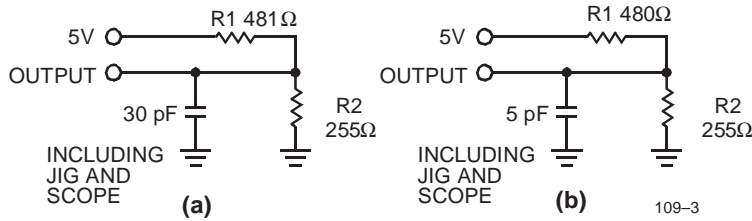
Capacitance^[5]

| Parameter | Description | Test Conditions | Max. | Unit |
|------------------|--------------------|--|------|------|
| C _{IN} | Input Capacitance | T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V | 10 | pF |
| C _{OUT} | Output Capacitance | | 10 | pF |

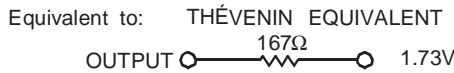
Notes:

1. V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



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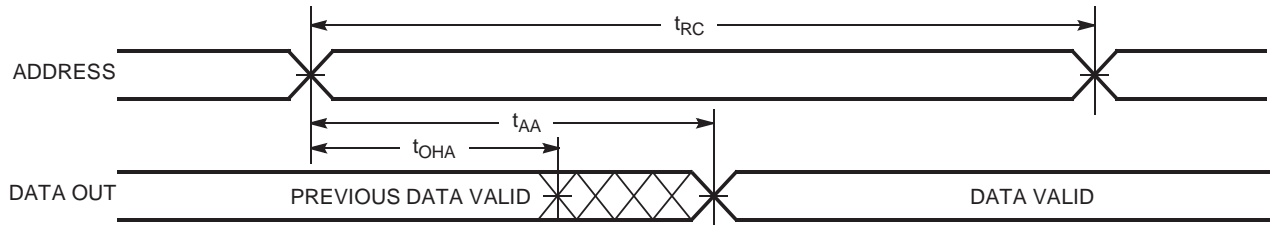
Switching Characteristics^[3,6] Over the Operating Range

| Parameter | Description | 62148-55 | | 62148-70 | | Unit |
|----------------------------------|--|----------|------|----------|------|------|
| | | Min. | Max. | Min. | Max. | |
| READ CYCLE | | | | | | |
| t _{RC} | Read Cycle Time | 55 | | 70 | | ns |
| t _{AA} | Address to Data Valid | | 55 | | 70 | ns |
| t _{OHA} | Data Hold from Address Change | 3 | | 3 | | ns |
| t _{ACE} | \overline{CE} LOW to Data Valid | | 55 | | 70 | ns |
| t _{DOE} | \overline{OE} LOW to Data Valid | | 20 | | 35 | ns |
| t _{LZOE} | \overline{OE} LOW to Low Z | 0 | | 0 | | ns |
| t _{HZOE} | \overline{OE} HIGH to High Z ^[7, 8] | | 20 | | 25 | ns |
| t _{LZCE} | \overline{CE} LOW to Low Z ^[8] | 3 | | 3 | | ns |
| t _{HZCE} | \overline{CE} HIGH to High Z ^[7, 8] | | 20 | | 25 | ns |
| t _{PU} | \overline{CE} LOW to Power-Up | 0 | | 0 | | ns |
| t _{PD} | \overline{CE} HIGH to Power-Down | | 55 | | 70 | ns |
| WRITE CYCLE^[9] | | | | | | |
| t _{WC} | Write Cycle Time | 55 | | 70 | | ns |
| t _{SCE} | \overline{CE} LOW to Write End | 45 | | 60 | | ns |
| t _{AW} | Address Set-Up to Write End | 45 | | 60 | | ns |
| t _{HA} | Address Hold from Write End | 0 | | 0 | | ns |
| t _{SA} | Address Set-Up to Write Start | 0 | | 0 | | ns |
| t _{PWE} | \overline{WE} Pulse Width | 45 | | 50 | | ns |
| t _{SD} | Data Set-Up to Write End | 45 | | 55 | | ns |
| t _{HD} | Data Hold from Write End | 0 | | 0 | | ns |
| t _{LZWE} | \overline{WE} HIGH to Low Z ^[8] | 3 | | 3 | | ns |
| t _{HZWE} | \overline{WE} LOW to High Z ^[7, 8] | | 20 | | 25 | ns |

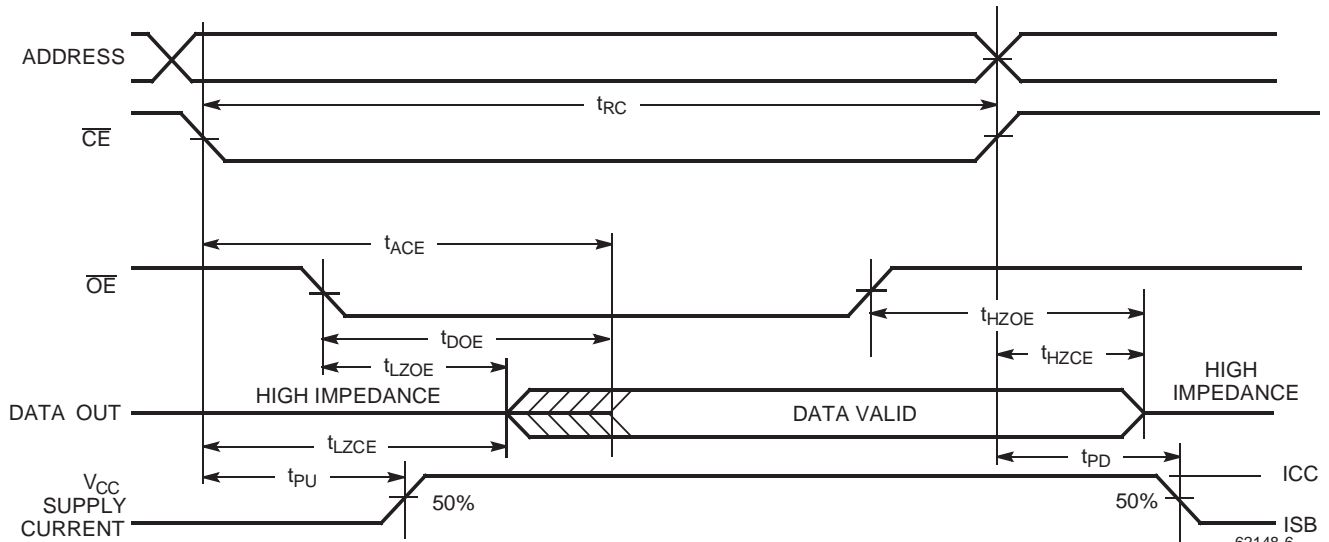
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Notes

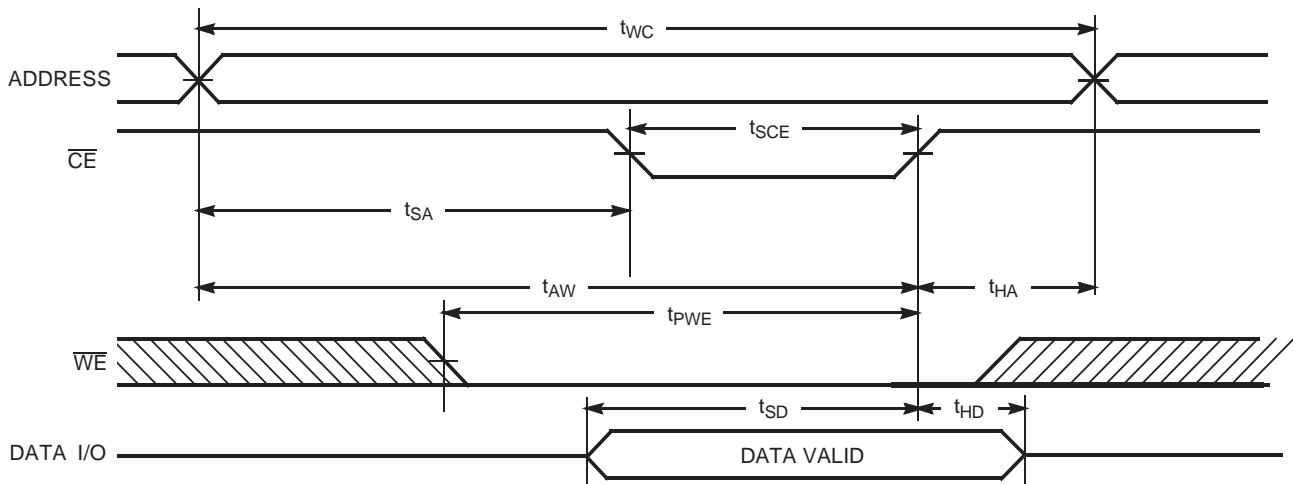
- Test conditions assume signal transition time of 5ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 100pF load capacitance.
- t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW, and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

Switching Waveforms
Read Cycle No.1^[10,11]


62148-5

Read Cycle No. 2 (\overline{OE} Controlled)^[11,12]


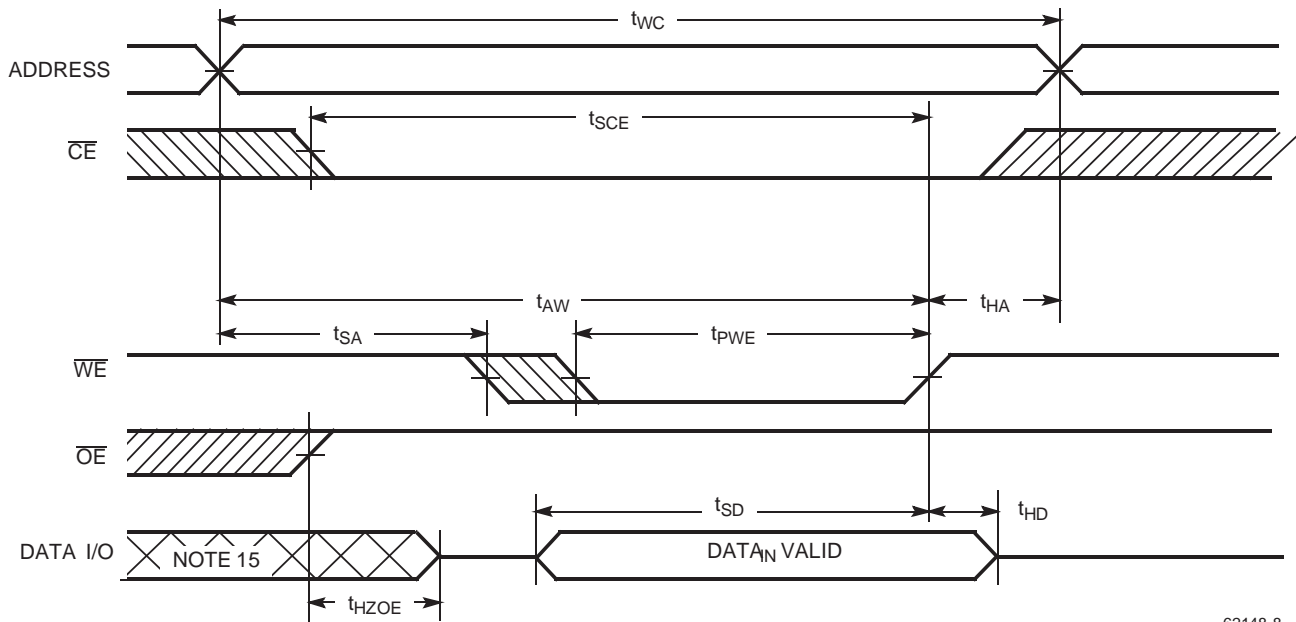
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Write Cycle No. 1 (\overline{CE} Controlled)^[13,14]


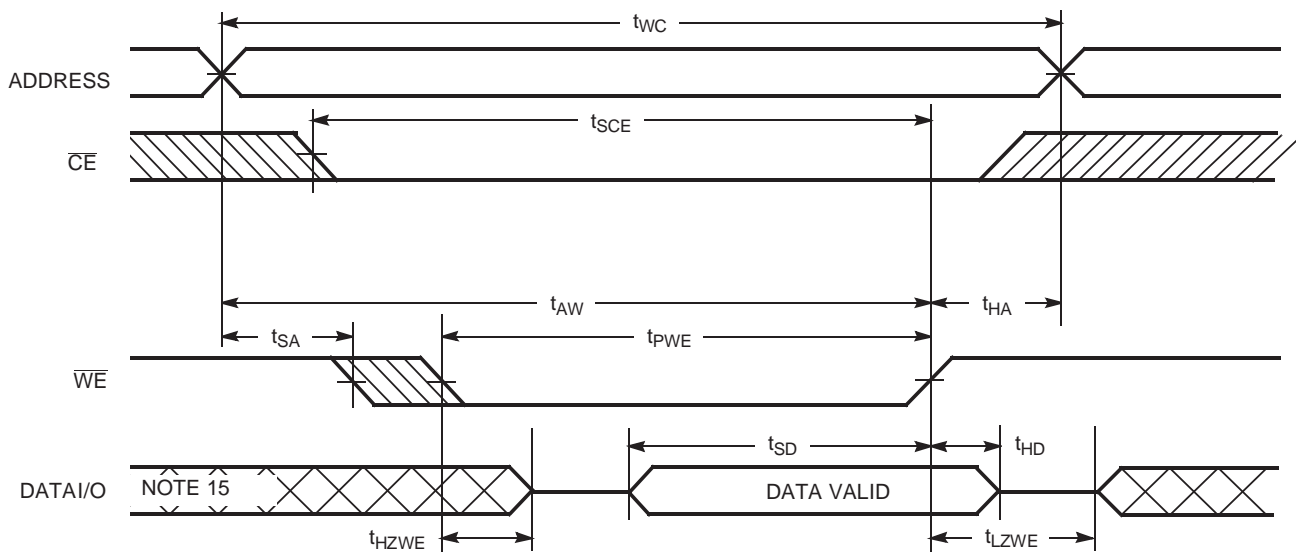
62148-7

Notes:

10. Device is continuously selected. \overline{OE} , \overline{CE} = V_{IL} .
11. \overline{WE} is HIGH for read cycle.
12. Address valid prior to or coincident with \overline{CE} transition LOW.
13. Data I/O is high impedance if \overline{OE} = V_{IH} .
14. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)
Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} HIGH During Write)^[13,14]


62148-8

Write Cycle No.3 (\overline{WE} Controlled, \overline{OE} LOW)^[13,14]


62148-9

Note:

15. During this period the I/Os are in the output state and input signals should not be applied

Truth Table

| CE ₁ | OE | WE | I/O ₀ – I/O ₇ | Mode | Power |
|-----------------|----|----|-------------------------------------|----------------------------|----------------------------|
| H | X | X | High Z | Power-Down | Standby (I _{SB}) |
| X | X | X | High Z | Power-Down | Standby (I _{SB}) |
| L | L | H | Data Out | Read | Active (I _{CC}) |
| L | X | L | Data In | Write | Active (I _{CC}) |
| L | H | H | High Z | Selected, Outputs Disabled | Active (I _{CC}) |

Data Retention Characteristics Over the Operating Range

| Parameter | Description | Conditions | Min. | Max | Unit |
|-------------------|--------------------------------------|--|-----------------|-----|------|
| V _{DR} | V _{CC} for Data Retention | No input may exceed V _{CC} + 0.5V | 2.0 | | V |
| I _{CCDR} | Data Retention Current | V _{CC} = V _{DR} = 2.0V, CE ≥ V _{CC} – 0.3V V _{IN} ≥ V _{CC} – 0.3V or V _{IN} ≤ 0.3V | (Com'l) | 200 | μA |
| | | | (Ind'l) | 500 | μA |
| | | | (Mil) | 2 | mA |
| t _{CDR} | Chip Deselect to Data Retention Time | | 0 | | ns |
| t _R | Operation Recovery Time | | t _{RC} | | ns |

Ordering Information

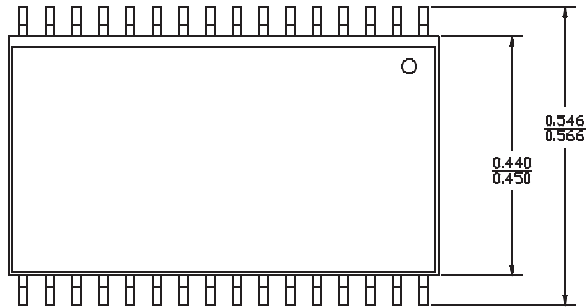
| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|---------------|--------------|-------------------------------|-----------------|
| 55 | CY62148–55SC | S34 | 32-Lead (450-Mil) Molded SOIC | Commercial |
| 55 | CY62148L–55SC | S34 | 32-Lead (450-Mil) Molded SOIC | Commercial |
| 70 | CY62148–70SC | S34 | 32-Lead (450-Mil) Molded SOIC | Commercial |
| 70 | CY62148L–70SC | S34 | 32-Lead (450-Mil) Molded SOIC | Commercial |
| 70 | CY62148-70SI | S34 | 32-Lead (450-Mil) Molded SOIC | Industrial |
| 70 | CY62148L-70SI | S34 | 32-Lead (450-Mil) Molded SOIC | Industrial |

Shaded areas contain advance information.

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Package Diagrams

32-Lead (450 Mil) Molded SOIC S34



DIMENSIONS IN INCHES MIN.
MAX.

