



# CY7C132/CY7C136 CY7C142/CY7C146

## 2Kx8 Dual-Port Static RAM

### Features

- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- 2K x 8 organization
- 0.65-micron CMOS for optimum speed/power
- High-speed access: 15 ns
- Low operating power: I<sub>CC</sub> = 90 mA (max.)
- Fully asynchronous operation
- Automatic power-down
- Master CY7C132/CY7C136 easily expands data bus width to 16 or more bits using slave CY7C142/CY7C146
- **BUSY** output flag on CY7C132/CY7C136; **BUSY** input on CY7C142/CY7C146
- **INT** flag for port-to-port communication (52-pin PLCC/PQFP versions)
- Available in 48-pin DIP (CY7C132/142), 52-pin PLCC and 52-pin TQFP (CY7C136/146)
- Pin-compatible and functionally equivalent to IDT7132/IDT7142

### Functional Description

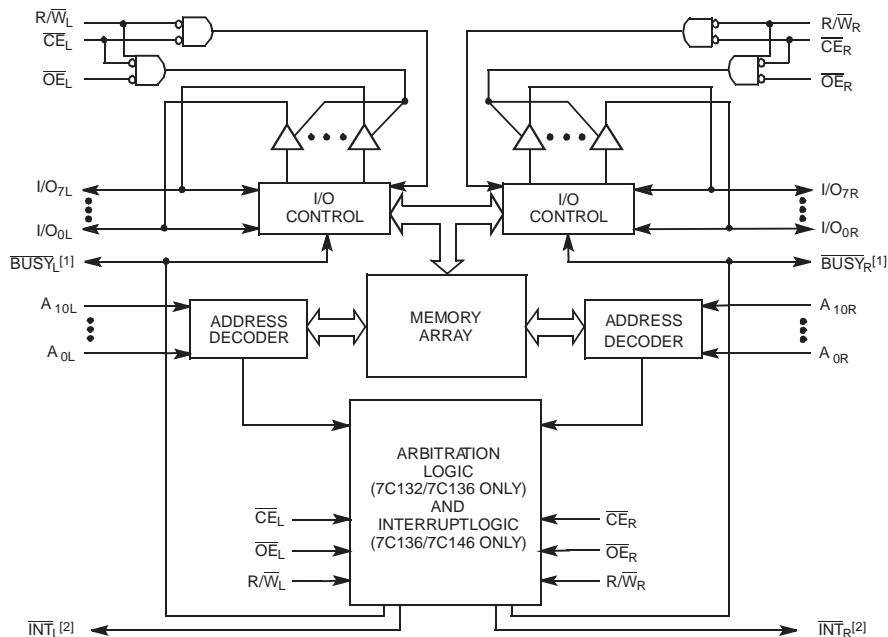
The CY7C132/CY7C136/CY7C142 and CY7C146 are high-speed CMOS 2K by 8 dual-port static RAMs. Two ports are provided to permit independent access to any location in memory. The CY7C132/ CY7C136 can be utilized as either a standalone 8-bit dual-port static RAM or as a MASTER dual-port RAM in conjunction with the CY7C142/CY7C146 SLAVE dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data such as cache memory for DSP, bit-slice, or multiprocessor designs.

Each port has independent control pins; chip enable ( $\overline{CE}$ ), write enable ( $R/\overline{W}$ ), and output enable ( $\overline{OE}$ ). **BUSY** flags are provided on each port. In addition, an interrupt flag ( $\overline{INT}$ ) is provided on each port of the 52-pin PLCC version. **BUSY** signals that the port is trying to access the same location currently being accessed by the other port. On the PLCC version,  $\overline{INT}$  is an interrupt flag indicating that data has been placed in a unique location (7FF for the left port and 7FE for the right port).

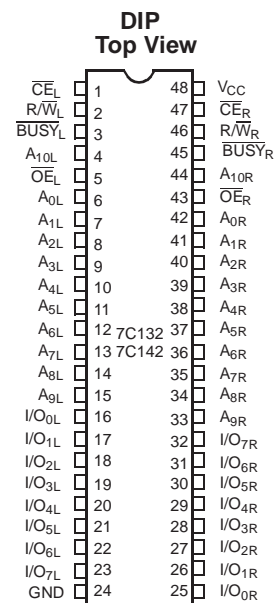
An automatic power-down feature is controlled independently on each port by the chip enable ( $\overline{CE}$ ) pins.

The CY7C132/CY7C142 are available in 48-pin DIP. The CY7C136/CY7C146 are available in 52-pin PLCC and PQFP.

### Logic Block Diagram



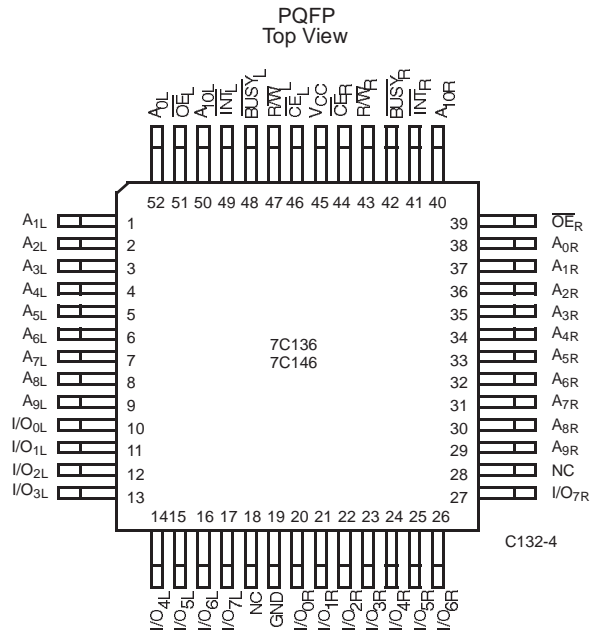
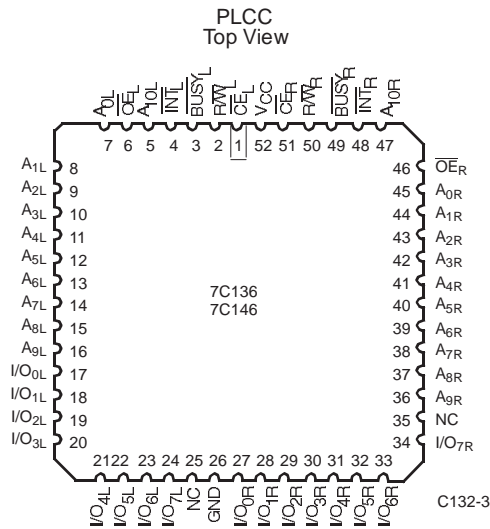
### Pin Configuration



**Notes:**

1. CY7C132/CY7C136 (Master): **BUSY** is open drain output and requires pull-up resistor. CY7C142/CY7C146 (Slave): **BUSY** is input.
2. Open drain outputs; pull-up resistor required.

**Pin Configurations** (continued)



**Selection Guide**

		7C136-15 <sup>[3,4]</sup> 7C146-15	7C132-25 <sup>[3]</sup> 7C136-25 7C142-25 7C146-25	7C132-30 7C136-30 7C142-30 7C146-30	7C132-35 7C136-35 7C142-35 7C146-35	7C132-45 7C136-45 7C142-45 7C146-45	7C132-55 7C136-55 7C142-55 7C146-55
Maximum Access Time (ns)		15	25	30	35	45	55
Maximum Operating Current (mA)	Com'l/Ind	190	170	170	120	90	90
	Military				170	120	120
Maximum Standby Current (mA)	Com'l/Ind	75	65	65	45	35	35
	Military				65	45	45

**Notes:**

- 3. 15 and 25-ns version available in PQFP and PLCC packages only.
- 4. Shaded area contains preliminary information.

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied..... -55°C to +125°C

Supply Voltage to Ground Potential (Pin 48 to Pin 24)..... -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... -0.5V to +7.0V

DC Input Voltage ..... -3.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%
Military <sup>[5]</sup>	-55°C to +125°C	5V ± 10%

**Note:**

- 5. T<sub>A</sub> is the "instant on" case temperature.



**Electrical Characteristics** Over the Operating Range<sup>[6]</sup>

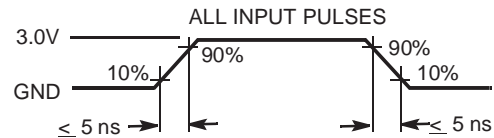
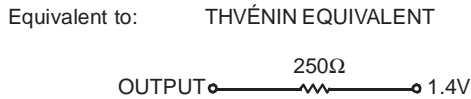
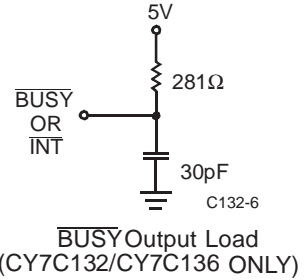
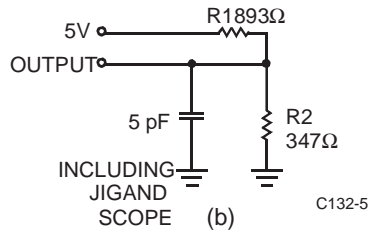
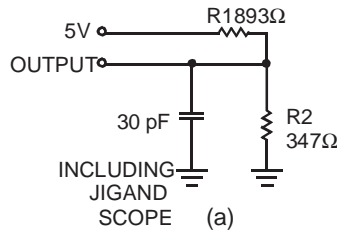
Parameter	Description	Test Conditions	7C136-15 <sup>[3,4]</sup> 7C146-15		7C132-30 <sup>[3]</sup> 7C136-25,30 7C142-30 7C146-25,30		7C132-35 7C136-35 7C142-35 7C146-35		7C132-45,55 7C136-45,55 7C142-45,55 7C146-45,55		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 4.0 mA		0.4		0.4		0.4		0.4	V
		I <sub>OL</sub> = 16.0 mA <sup>[7]</sup>		0.5		0.5		0.5		0.5	
V <sub>IH</sub>	Input HIGH Voltage		2.2		2.2		2.2		2.2		V
V <sub>IL</sub>	Input LOW Voltage			0.8		0.8		0.8		0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-5	+5	-5	+5	-5	+5	-5	+5	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	-5	+5	-5	+5	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[8]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-350		-350		-350		-350	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	$\overline{CE} = V_{IL}$ , Outputs Open, f = f <sub>MAX</sub> <sup>[9]</sup>	Com'l	190		170		120		90	mA
			Mil					170		120	
I <sub>SB1</sub>	Standby Current Both Ports, TTL Inputs	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ , f = f <sub>MAX</sub> <sup>[9]</sup>	Com'l	75		65		45		35	mA
			Mil					65		45	
I <sub>SB2</sub>	Standby Current One Port, TTL Inputs	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ , Active Port Outputs Open, f = f <sub>MAX</sub> <sup>[9]</sup>	Com'l	135		115		90		75	mA
			Mil					115		90	
I <sub>SB3</sub>	Standby Current Both Ports, CMOS Inputs	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0	Com'l	15		15		15		15	mA
			Mil					15		15	
I <sub>SB4</sub>	Standby Current One Port, CMOS Inputs	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, Active Port Outputs Open, f = f <sub>MAX</sub> <sup>[9]</sup>	Com'l	125		105		85		70	mA
			Mil					105		85	

**Capacitance<sup>[10]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz,	15	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = 5.0V	10	pF

**Notes:**

6. See the last page of this specification for Group A subgroup testing information.
7. BUSY and INT pins only.
8. Duration of the short circuit should not exceed 30 seconds.
9. At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency of read cycle of 1/t<sub>rc</sub> and using AC Test Waveforms input levels of GND to 3V.
10. This parameter is guaranteed but not tested.

**AC Test Loads and Waveforms**

**Switching Characteristics** Over the Operating Range<sup>[6, 11]</sup>

Parameter	Description	7C136-15 <sup>[3,4]</sup> 7C146-15		7C132-25 <sup>[3]</sup> 7C136-25 7C142-25 7C146-25		7C132-30 7C136-30 7C142-30 7C146-30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>								
$t_{RC}$	Read Cycle Time	15		25		30		ns
$t_{AA}$	Address to Data Valid <sup>[12]</sup>		15		25		30	ns
$t_{OHA}$	Data Hold from Address Change	0		0		0		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid <sup>[12]</sup>		15		25		30	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid <sup>[12]</sup>		10		15		20	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z <sup>[10, 13]</sup>	3		3		3		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[10, 13, 14]</sup>		10		15		15	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[10, 13]</sup>	3		5		5		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[10, 13, 14]</sup>		10		15		15	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up <sup>[10]</sup>	0		0		0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down <sup>[10]</sup>		15		25		25	ns
<b>WRITE CYCLE<sup>[15]</sup></b>								
$t_{WC}$	Write Cycle Time	15		25		30		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	12		20		25		ns
$t_{AW}$	Address Set-Up to Write End	12		20		25		ns
$t_{HA}$	Address Hold from Write End	2		2		2		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		0		ns
$t_{PWE}$	R/ $\overline{W}$ Pulse Width	12		15		25		ns
$t_{SD}$	Data Set-Up to Write End	10		15		15		ns
$t_{HD}$	Data Hold from Write End	0		0		0		ns
$t_{HZWE}$	R/ $\overline{W}$ LOW to High Z <sup>[10]</sup>		10		15		15	ns
$t_{LZWE}$	R/ $\overline{W}$ HIGH to Low Z <sup>[10]</sup>	0		0		0		ns

**Switching Characteristics** Over the Operating Range<sup>[6, 11]</sup> (continued)

Parameter	Description	7C136-15 <sup>[3,4]</sup> 7C146-15		7C132-25 <sup>[3]</sup> 7C136-25 7C142-25 7C146-25		7C132-30 7C136-30 7C142-30 7C146-30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>BUSY/INTERRUPT TIMING</b>								
t <sub>BLA</sub>	BUSY LOW from Address Match		15		20		20	ns
t <sub>BHA</sub>	BUSY HIGH from Address Mismatch <sup>[16]</sup>		15		20		20	ns
t <sub>BLC</sub>	BUSY LOW from $\overline{CE}$ LOW		15		20		20	ns
t <sub>BHC</sub>	BUSY HIGH from $\overline{CE}$ HIGH <sup>[16]</sup>		15		20		20	ns
t <sub>PS</sub>	Port Set Up for Priority	5		5		5		ns
t <sub>WB</sub>	R/ $\overline{W}$ LOW after BUSY LOW <sup>[17]</sup>	0		0		0		ns
t <sub>WH</sub>	R/ $\overline{W}$ HIGH after BUSY HIGH	13		20		30		ns
t <sub>BDD</sub>	BUSY HIGH to Valid Data		15		25		30	ns
t <sub>DDD</sub>	Write Data Valid to Read Data Valid		Note 18		Note 18		Note 18	ns
t <sub>WDD</sub>	Write Pulse to Data Delay		Note 18		Note 18		Note 18	ns
<b>INTERRUPT TIMING<sup>[19]</sup></b>								
t <sub>WINS</sub>	R/ $\overline{W}$ to $\overline{INTERRUPT}$ Set Time		15		25		25	ns
t <sub>EINS</sub>	$\overline{CE}$ to $\overline{INTERRUPT}$ Set Time		15		25		25	ns
t <sub>INS</sub>	Address to $\overline{INTERRUPT}$ Set Time		15		25		25	ns
t <sub>OINR</sub>	$\overline{OE}$ to $\overline{INTERRUPT}$ Reset Time <sup>[16]</sup>		15		25		25	ns
t <sub>EINR</sub>	$\overline{CE}$ to $\overline{INTERRUPT}$ Reset Time <sup>[16]</sup>		15		25		25	ns
t <sub>INR</sub>	Address to $\overline{INTERRUPT}$ Reset Time <sup>[16]</sup>		15		25		25	ns

**Switching Characteristics** Over the Operating Range<sup>[6, 11]</sup>

Parameter	Description	7C132-35 7C136-35 7C142-35 7C146-35		7C132-45 7C136-45 7C142-45 7C146-45		7C132-55 7C136-55 7C142-55 7C146-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>								
t <sub>RC</sub>	Read Cycle Time	35		45		55		ns
t <sub>AA</sub>	Address to Data Valid <sup>[12]</sup>		35		45		55	ns
t <sub>OHA</sub>	Data Hold from Address Change	0		0		0		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid <sup>[12]</sup>		35		45		55	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid <sup>[12]</sup>		20		25		25	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[10, 13]</sup>	3		3		3		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[10, 13, 14]</sup>		20		20		25	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[10, 13]</sup>	5		5		5		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[10, 13, 14]</sup>		20		20		25	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up <sup>[10]</sup>	0		0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down <sup>[10]</sup>		35		35		35	ns

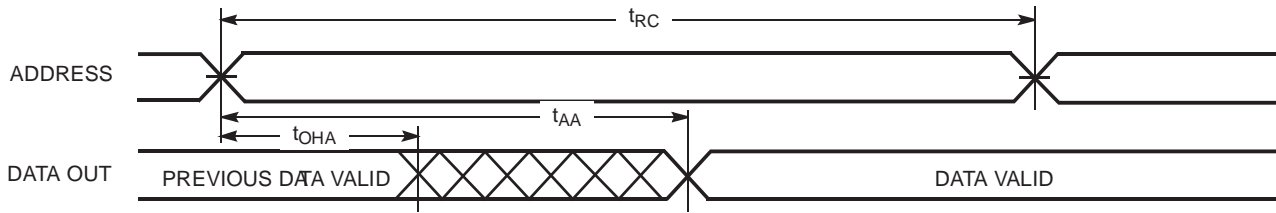


Switching Characteristics Over the Operating Range<sup>[6, 11]</sup> (continued)

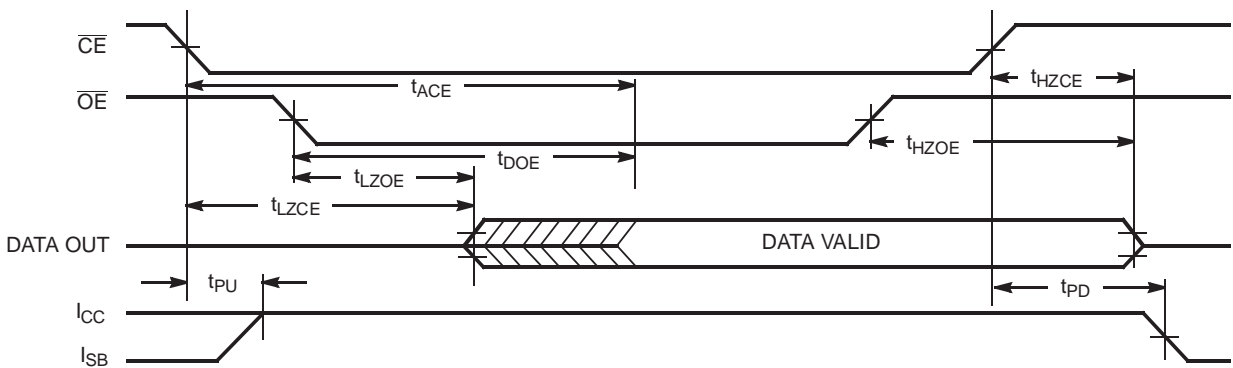
		7C132-35 7C136-35 7C142-35 7C146-35	7C132-45 7C136-45 7C142-45 7C146-45	7C132-55 7C136-55 7C142-55 7C146-55		
<b>WRITE CYCLE<sup>[15]</sup></b>						
t <sub>WC</sub>	Write Cycle Time	35	45	55		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	30	35	40		ns
t <sub>AW</sub>	Address Set-Up to Write End	30	35	40		ns
t <sub>HA</sub>	Address Hold from Write End	2	2	2		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0	0	0		ns
t <sub>PWE</sub>	R/ $\overline{W}$ Pulse Width	25	30	30		ns
t <sub>SD</sub>	Data Set-Up to Write End	15	20	20		ns
t <sub>HD</sub>	Data Hold from Write End	0	0	0		ns
t <sub>HZWE</sub>	R/ $\overline{W}$ LOW to High Z <sup>[10]</sup>		20	20		25 ns
t <sub>LZWE</sub>	R/ $\overline{W}$ HIGH to Low Z <sup>[10]</sup>	0	0	0		ns
<b>BUSY/INTERRUPT TIMING</b>						
t <sub>BLA</sub>	$\overline{BUSY}$ LOW from Address Match		20	25		30 ns
t <sub>BHA</sub>	$\overline{BUSY}$ HIGH from Address Mismatch <sup>[16]</sup>		20	25		30 ns
t <sub>BLC</sub>	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		20	25		30 ns
t <sub>BHC</sub>	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH <sup>[16]</sup>		20	25		30 ns
t <sub>PS</sub>	Port Set Up for Priority	5	5	5		ns
t <sub>WB</sub>	R/ $\overline{W}$ LOW after $\overline{BUSY}$ LOW <sup>[17]</sup>	0	0	0		ns
t <sub>WH</sub>	R/ $\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	30	35	35		ns
t <sub>BDD</sub>	$\overline{BUSY}$ HIGH to Valid Data		35	45		45 ns
t <sub>DDD</sub>	Write Data Valid to Read Data Valid		Note 18	Note 18		Note 18 ns
t <sub>WDD</sub>	Write Pulse to Data Delay		Note 18	Note 18		Note 18 ns
<b>INTERRUPT TIMING<sup>[19]</sup></b>						
t <sub>WINS</sub>	R/ $\overline{W}$ to $\overline{INTERRUPT}$ Set Time		25	35		45 ns
t <sub>EINS</sub>	$\overline{CE}$ to $\overline{INTERRUPT}$ Set Time		25	35		45 ns
t <sub>INS</sub>	Address to $\overline{INTERRUPT}$ Set Time		25	35		45 ns
t <sub>OINR</sub>	$\overline{OE}$ to $\overline{INTERRUPT}$ Reset Time <sup>[16]</sup>		25	35		45 ns
t <sub>EINR</sub>	$\overline{CE}$ to $\overline{INTERRUPT}$ Reset Time <sup>[16]</sup>		25	35		45 ns
t <sub>INR</sub>	Address to $\overline{INTERRUPT}$ Reset Time <sup>[16]</sup>		25	35		45 ns

Notes:

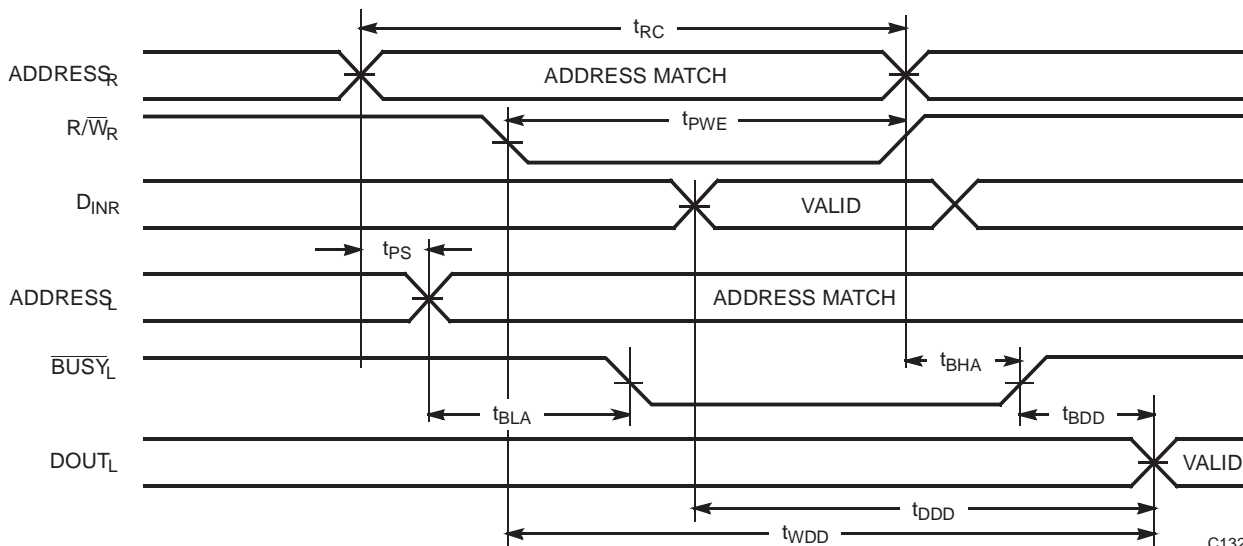
- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
- AC test conditions use V<sub>OH</sub> = 1.6V and V<sub>OL</sub> = 1.4V.
- At any given temperature and voltage condition for any given device, t<sub>HZCE</sub> is less than t<sub>LZCE</sub> and t<sub>HZOE</sub> is less than t<sub>LZOE</sub>.
- t<sub>LZCE</sub>, t<sub>LZWE</sub>, t<sub>HZOE</sub>, t<sub>LZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are tested with C<sub>L</sub> = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and R/ $\overline{W}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
- CY7C142/CY7C146 only.
- A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:  
  - $\overline{BUSY}$  on Port B goes HIGH.
  - Port B's address toggled.
  - $\overline{CE}$  for Port B is toggled.
  - R/ $\overline{W}$  for Port B is toggled during valid read.
- 52-pin PLCC and PQFP versions only.

**Switching Waveforms**
**Read Cycle No. 1 (Either Port-Address Access)<sup>[20, 21]</sup>**


C132-7

**Read Cycle No. 2 (Either Port- $\overline{CE}/\overline{OE}$ )<sup>[20, 22]</sup>**


C132-8

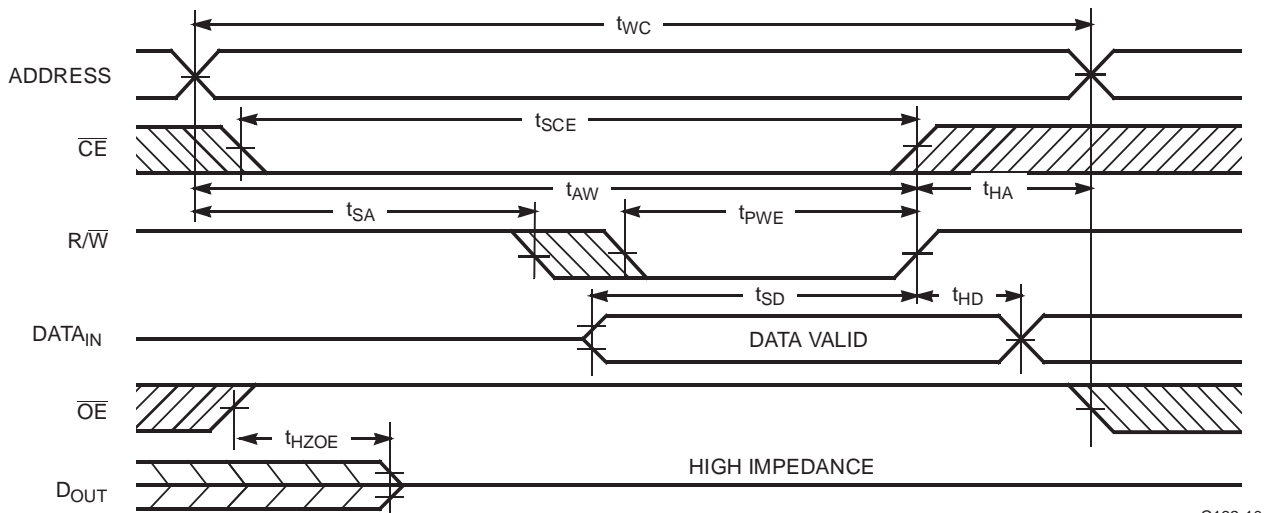
**Read Cycle No. 3 (Read with BUSY Master: CY7C132 and CY7C136)**


C132-9

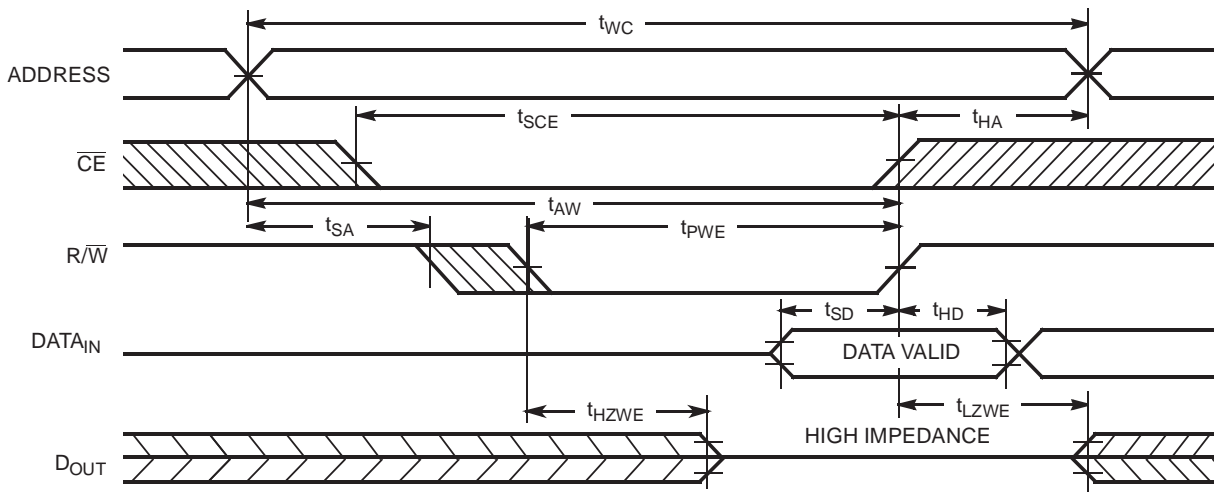
**Notes:**

20. R/ $\overline{W}$  is HIGH for read cycle.
21. Device is continuously selected,  $\overline{CE} = V_{IL}$  and  $\overline{OE} = V_{IL}$ .
22. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms** (continued)

**Write Cycle No.1 ( $\overline{OE}$  Three-States Data I/Os-Either Port)<sup>[15, 23]</sup>**


C132-10

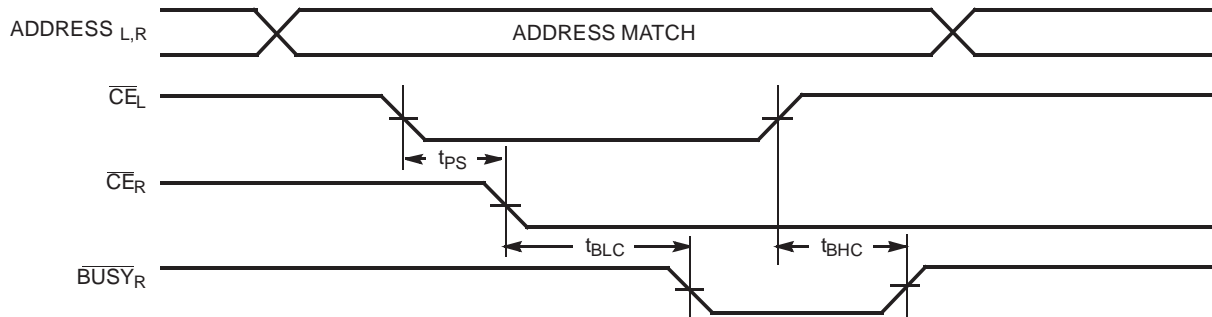
**Write Cycle No. 2 ( $R/\overline{W}$  Three-States Data I/Os-Either Port)<sup>[15, 24]</sup>**


C132-11

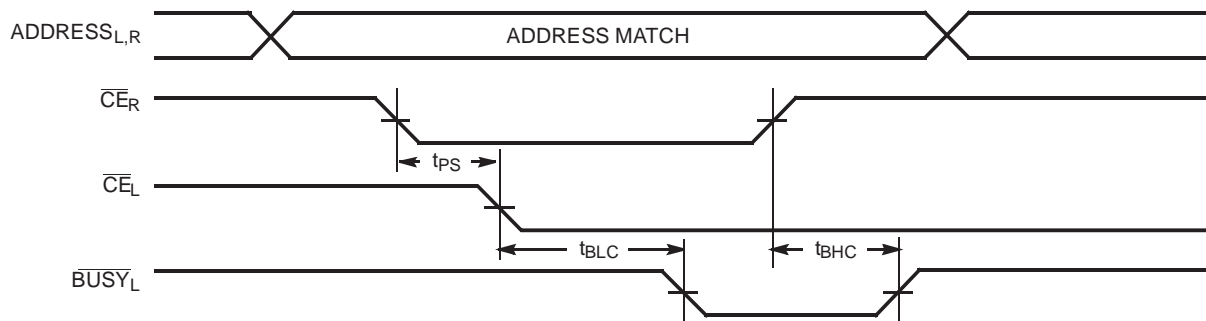
**Notes:**

23. If  $\overline{OE}$  is LOW during a  $R/\overline{W}$  controlled write cycle, the write pulse width must be the larger of  $t_{PWE}$  or  $t_{HZWE} + t_{SD}$  to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required  $t_{SD}$ .
24. If the  $\overline{CE}$  LOW transition occurs simultaneously with or after the  $R/\overline{W}$  LOW transition, the outputs remain in a high-impedance state.



**Switching Waveforms (continued)**
**Busy Timing Diagram No. 1 ( $\overline{CE}$  Arbitration)**
 $\overline{CE}_L$  Valid First:


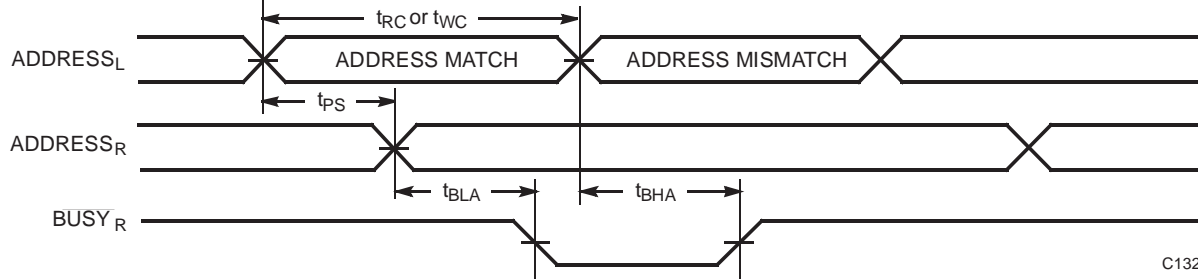
C132-12

 $\overline{CE}_R$  Valid First:


C132-13

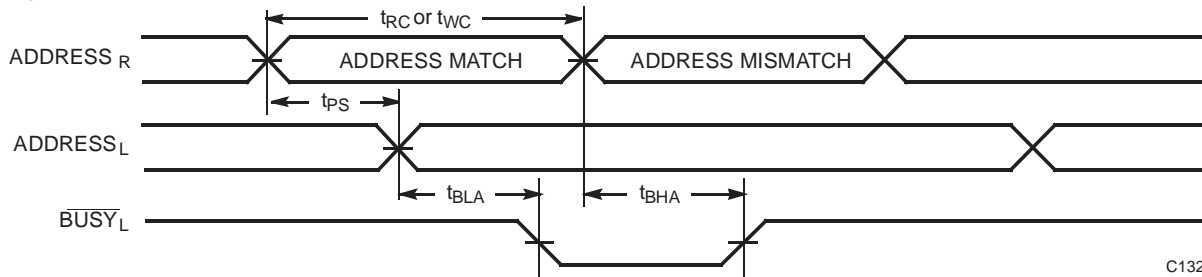
**Busy Timing Diagram No. 2 (Address Arbitration)**

Left Address/valid First:

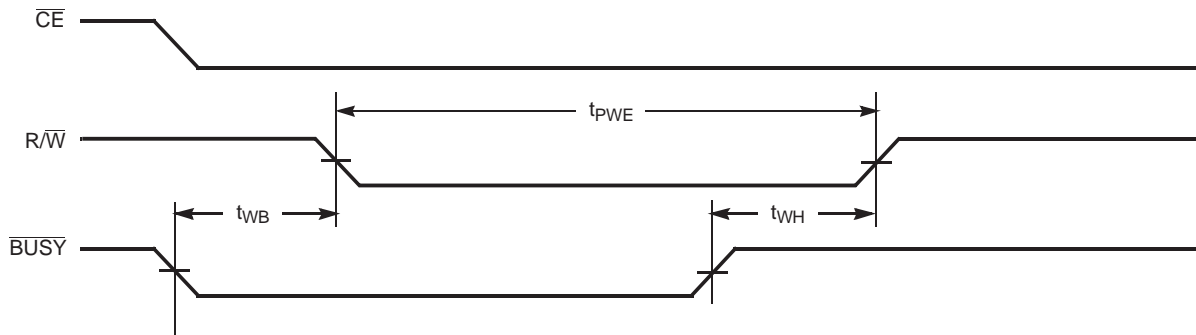


C132-14

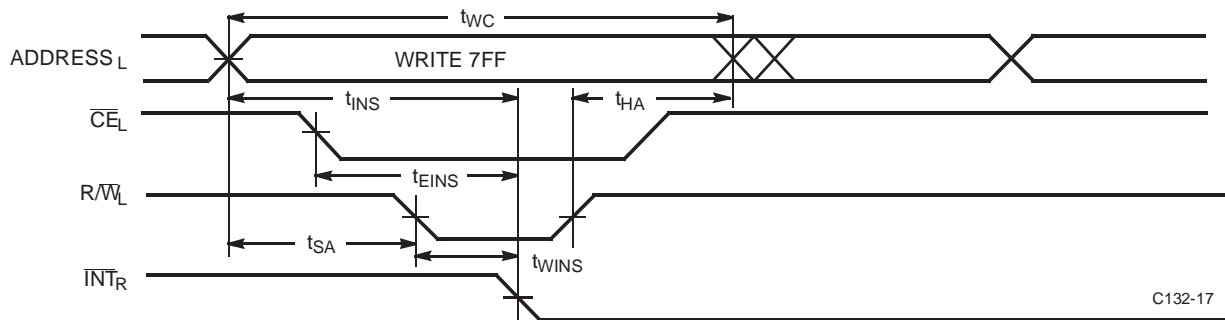
Right Address Valid First:



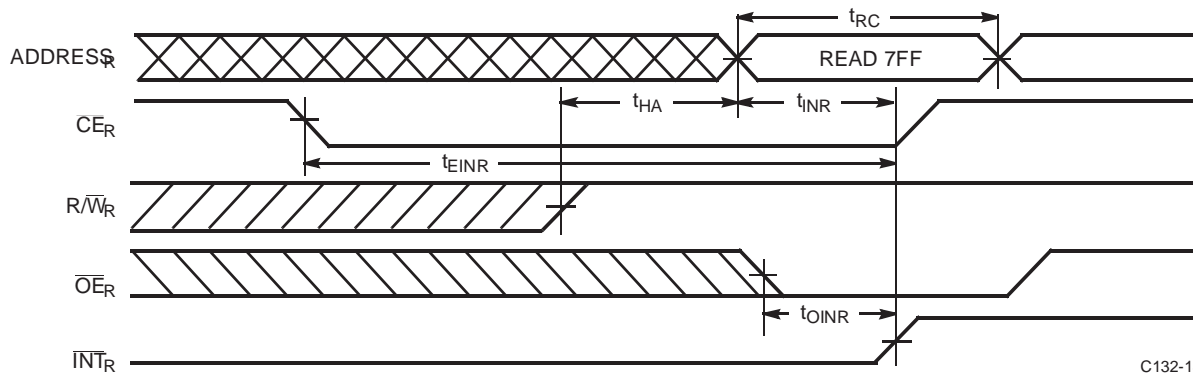
C132-15

**Switching Waveforms (continued)**
**Busy Timing Diagram No. 3 (Write with  $\overline{\text{BUSY}}$ , Slave: CY7C142/CY7C146)**


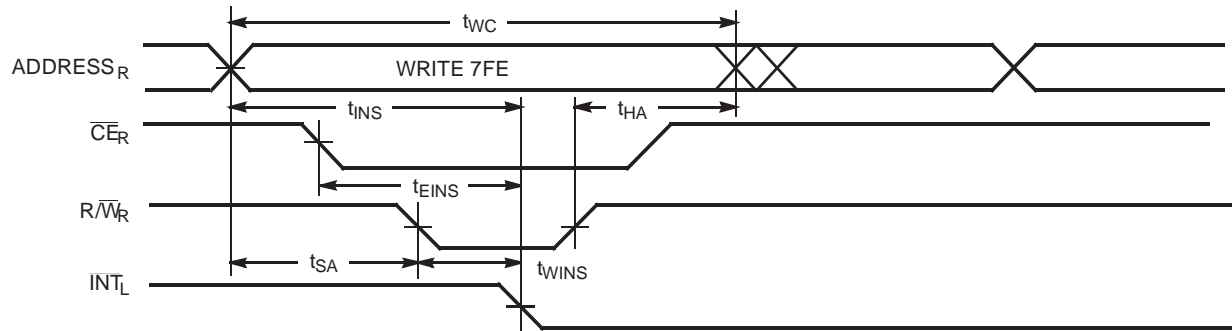
C132-16

**Interrupt Timing Diagrams<sup>[19]</sup>**
**Left Side Sets  $\overline{\text{INT}}_{\text{R}}$ :**


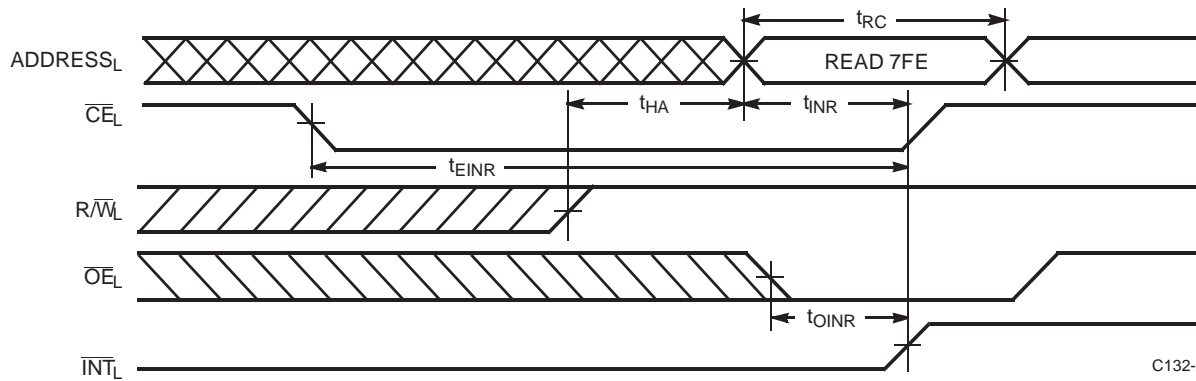
C132-17

**Right Side Clears  $\overline{\text{INT}}_{\text{R}}$ :**


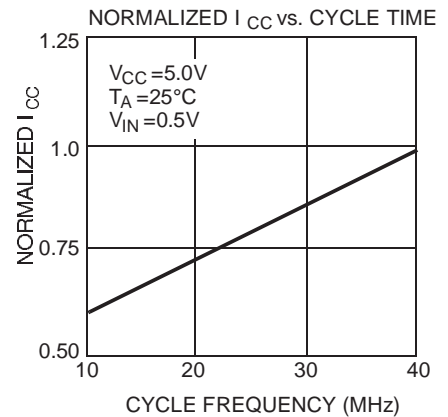
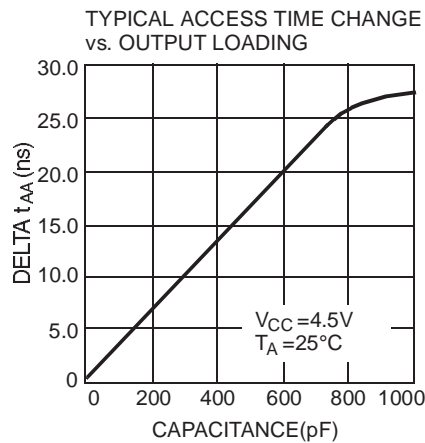
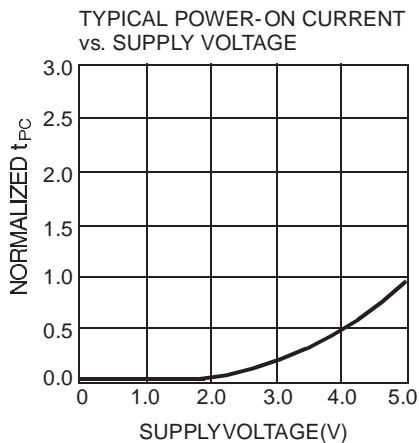
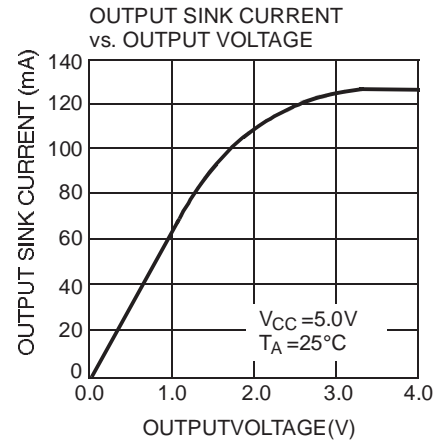
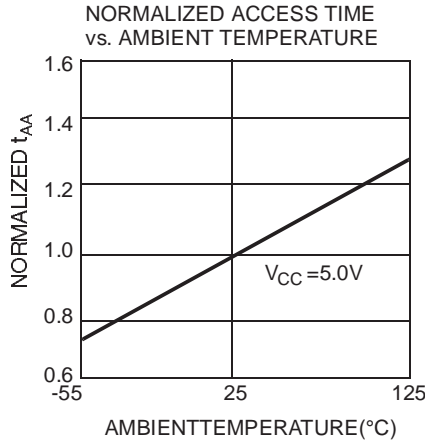
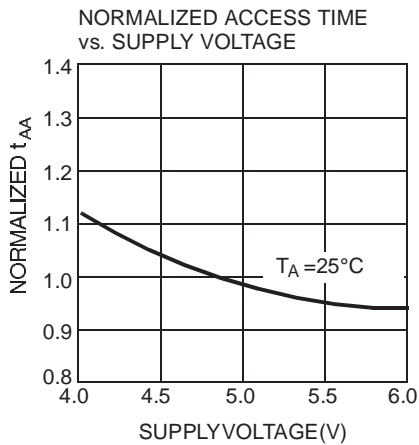
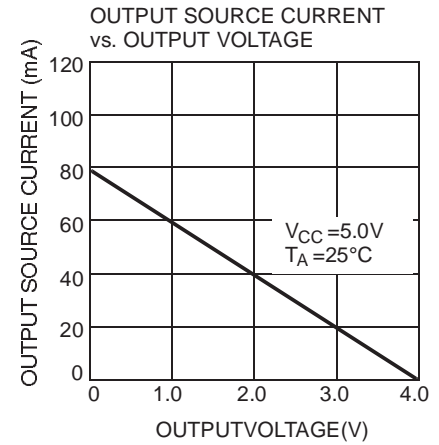
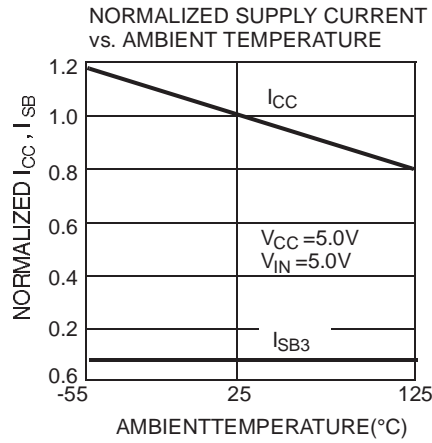
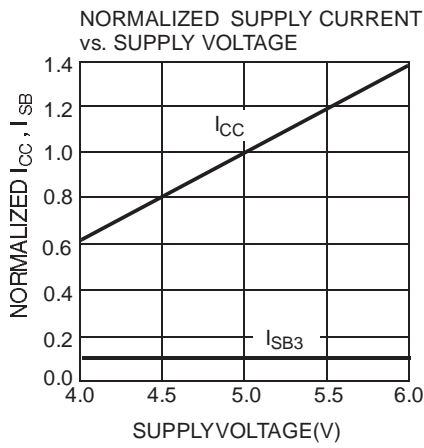
C132-18

**Interrupt Timing Diagrams<sup>[19]</sup> (continued)**
**Right Side Sets  $\overline{INT}_L$ :**


C132-19

**Right Side Clears  $\overline{INT}_L$ :**


C132-20

**Typical DC and AC Characteristics**




**Ordering Information**

<b>Speed (ns)</b>	<b>Ordering Code</b>	<b>Package Name</b>	<b>Package Type</b>	<b>Operating Range</b>
30	CY7C132-30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132-30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C132-35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132-35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C132-35DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
45	CY7C132-45PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132-45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C132-45DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
55	CY7C132-55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132-55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C132-55DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
<b>Speed (ns)</b>	<b>Ordering Code</b>	<b>Package Name</b>	<b>Package Type</b>	<b>Operating Range</b>
15	CY7C136-15JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136-15NC	N52	52-Pin Plastic Quad Flatpack	
25	CY7C136-25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136-25NC	N52	52-Pin Plastic Quad Flatpack	
30	CY7C136-30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136-30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C136-30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C136-35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136-35NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C136-35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C136-35LMB	L69	52-Square Leadless Chip Carrier	Military
45	CY7C136-45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136-45NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C136-45JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C136-45LMB	L69	52-Square Leadless Chip Carrier	Military
55	CY7C136-55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136-55NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C136-55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C136-55LMB	L69	52-Square Leadless Chip Carrier	Military

Shaded area contains preliminary information.



**Ordering Information** (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C142-30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C142-30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C142-35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C142-35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C142-35DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military
45	CY7C142-45PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C142-45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C142-45DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military
55	CY7C142-55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C142-55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C142-55DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C136-15JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136-15NC	N52	52-Pin Plastic Quad Flatpack	
25	CY7C146-25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146-25NC	N52	52-Pin Plastic Quad Flatpack	
30	CY7C146-30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146-30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C146-30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C146-35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146-35NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C146-35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C146-35LMB	L69	52-Square Leadless Chip Carrier	Military
45	CY7C146-45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146-45NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C146-45JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C146-45LMB	L69	52-Square Leadless Chip Carrier	Military
55	CY7C146-55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146-55NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C146-55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C146-55LMB	L69	52-Square Leadless Chip Carrier	Military

Shaded area contains preliminary information.

**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**

Parameter	Subgroups
$V_{OH}$	1, 2, 3
$V_{OL}$	1, 2, 3
$V_{IH}$	1, 2, 3
$V_{IL}$ Max.	1, 2, 3
$I_{IX}$	1, 2, 3
$I_{OZ}$	1, 2, 3
$I_{CC}$	1, 2, 3
$I_{SB1}$	1, 2, 3
$I_{SB2}$	1, 2, 3
$I_{SB3}$	1, 2, 3
$I_{SB4}$	1, 2, 3

**Switching Characteristics**

Parameter	Subgroups
<b>READ CYCLE</b>	
$t_{RC}$	7, 8, 9, 10, 11
$t_{AA}$	7, 8, 9, 10, 11
$t_{ACE}$	7, 8, 9, 10, 11
$t_{DOE}$	7, 8, 9, 10, 11
<b>WRITE CYCLE</b>	
$t_{WC}$	7, 8, 9, 10, 11
$t_{SCE}$	7, 8, 9, 10, 11
$t_{AW}$	7, 8, 9, 10, 11
$t_{HA}$	7, 8, 9, 10, 11
$t_{SA}$	7, 8, 9, 10, 11
$t_{PWE}$	7, 8, 9, 10, 11
$t_{SD}$	7, 8, 9, 10, 11
$t_{HD}$	7, 8, 9, 10, 11
<b>BUSY/INTERRUPT TIMING</b>	
$t_{BLA}$	7, 8, 9, 10, 11
$t_{BHA}$	7, 8, 9, 10, 11
$t_{BLC}$	7, 8, 9, 10, 11
$t_{BHC}$	7, 8, 9, 10, 11
$t_{PS}$	7, 8, 9, 10, 11
$t_{WINS}$	7, 8, 9, 10, 11
$t_{EINS}$	7, 8, 9, 10, 11
$t_{INS}$	7, 8, 9, 10, 11
$t_{OINR}$	7, 8, 9, 10, 11
$t_{EINR}$	7, 8, 9, 10, 11
$t_{INR}$	7, 8, 9, 10, 11
<b>BUSY TIMING</b>	
$t_{WB}^{[25]}$	7, 8, 9, 10, 11
$t_{WH}$	7, 8, 9, 10, 11
$t_{BDD}$	7, 8, 9, 10, 11

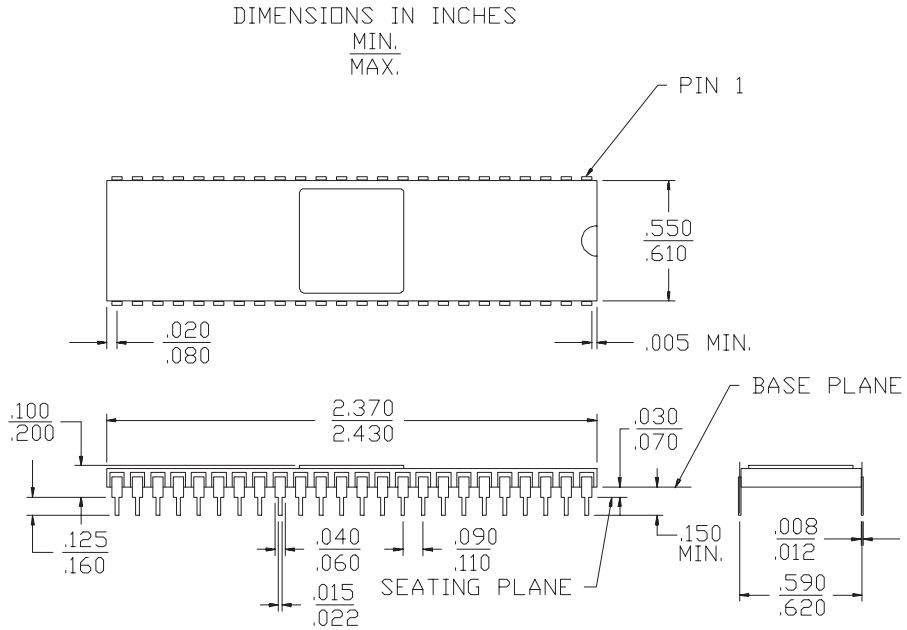
**Note:**

25. CY7C142/CY7C146 only.

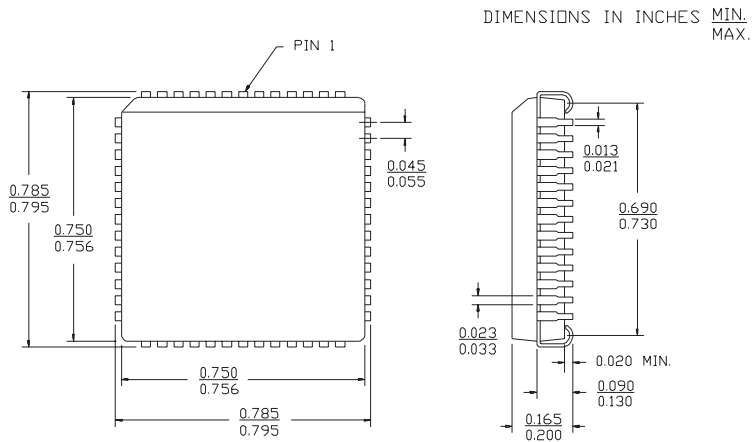
Document #: 38-00061-K

**Package Diagrams**

**48-Lead (600-Mil) Sidebrazed DIP D26**



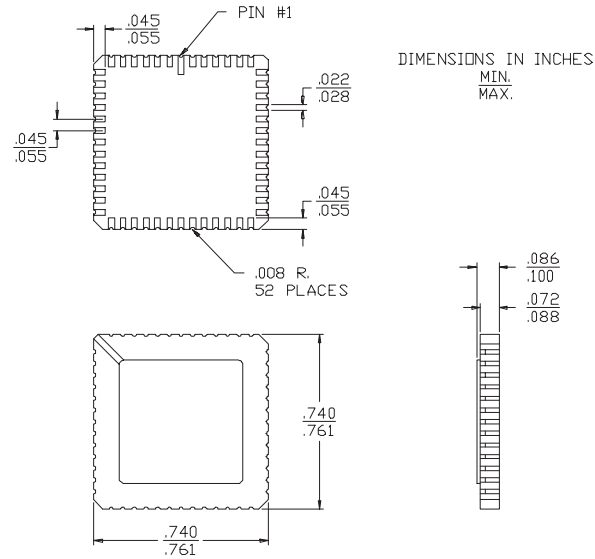
**52-Lead Plastic Leaded Chip Carrier J69**



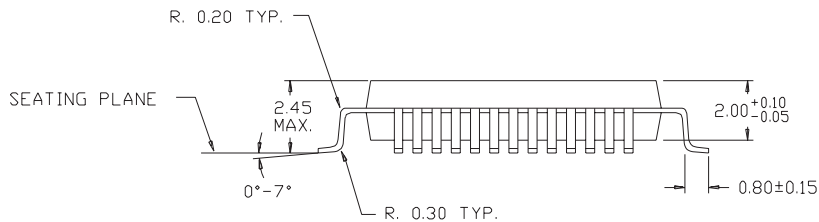
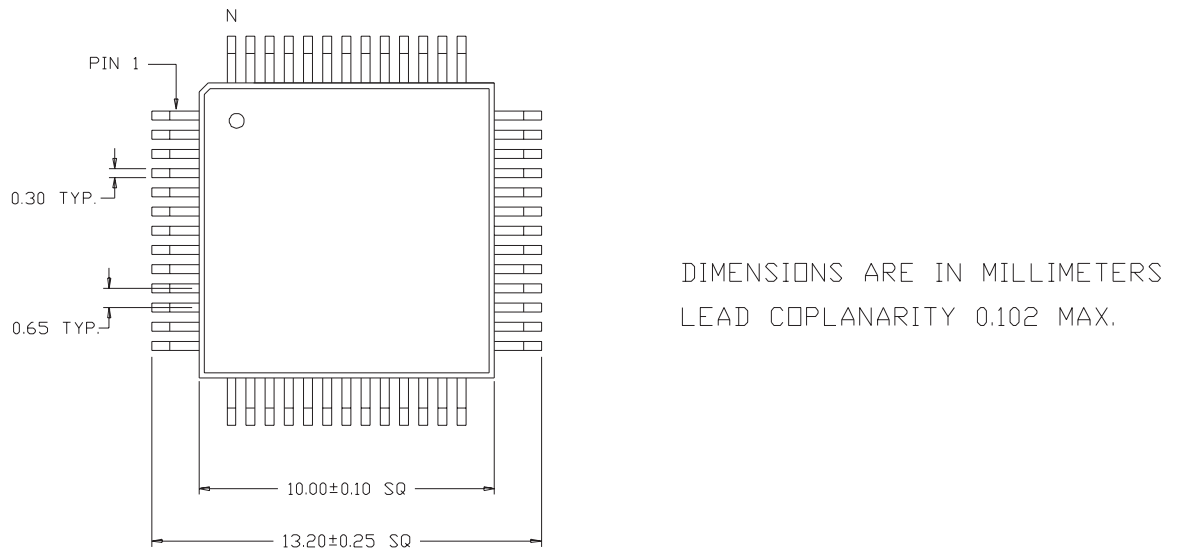


Package Diagrams (continued)

52-Square Leadless Chip Carrier L69



52-Lead Plastic Quad Flatpack N52



Package Diagrams (continued)

**48-Lead (600-Mil) Molded DIP P25**

