



COMPLEMENTARY PAIR ENHANCEMENT MODE MOSFET

Product Summary

Device	V _{(BR)DSS}	R _{DS(on) max}	I _D T _A = +25°C
Q2	40V	24mΩ @ V _{GS} = 10V	6.9A
QZ	40 V	32mΩ @ V _{GS} = 4.5V	6.0A
Q1	-40V	45mΩ @ V _{GS} = -10V	-5.1A
		55mΩ @ V _{GS} = -4.5V	-4.5A

Description

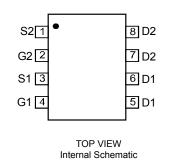
This new generation MOSFET has been designed to minimize the onstate resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- DC-DC Converters
- Power Management Functions
- Backlighting



Top View

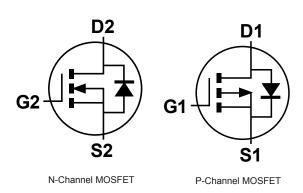


Features and Benefits

- Low Input Capacitance
- Low On-Resistance
- Fast Switching Speed
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish Matte Tin annealed over Copper leadframe Solderable per MIL-STD-202, Method 208 (3)
- Weight: 0.074 grams (approximate)



Ordering Information (Note 4)

Part Number	Case	Packaging
DMC4047LSD-13	SO-8	2,500/Tape & Reel

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.

See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green"

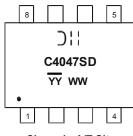
and Lead-free.

Notes:

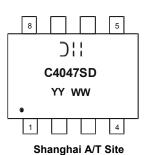
Alalogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and
 <1000ppm antimony compounds.

4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



Chengdu A/T Site



): | = Manufacturer's Marking
C4047SD = Product Type Marking Code
YYW<u>W</u> = Date Code Marking
YY or YY = Year (ex: 13 = 2013)
WW = Week (01 - 53)
<u>YY</u> = Date Code Marking for SAT (Shanghai Assembly/ Test site)
<u>YY</u> = Date Code Marking for CAT (Chengdu Assembly/ Test site)

DMC4047LSD Document number: DS36206 Rev. 4 - 2



Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value_Q2	Value_Q1	Units		
Drain-Source Voltage	V _{DSS}	40	-40	V		
Gate-Source Voltage	V _{GSS}	±20	±20	V		
Continuous Drain Current (Note C) V = 10V	Steady State	T _A = +25°C T _A = +70°C	ID	7.0 5.6	-5.1 -4.1	А
Continuous Drain Current (Note 6) V _{GS} = 10V	t<10s	T _A = +25°C T _A = +70°C	ID	9.0 7.2	-6.5 -5.2	A
Maximum Body Diode Forward Current (Note 6)	Is	2.5	-2.5	А		
Pulsed Drain Current (10µs pulse, duty cycle = 1	I _{DM}	70	-40	А		
Avalanche Current (Notes 7) L = 0.1mH	I _{AR}	20	20	А		
Repetitive Avalanche Energy (Notes 7) L = 0.1m	E _{AR}	20	20	mJ		

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Units
Total Dower Dissinction (Note 5)	T _A = +25°C	D	1.3	W
Total Power Dissipation (Note 5)	T _A = +70°C	PD	0.8	
Thermal Registeries, Junction to Ambient (Note 5)	Steady state		98	°C/W
Thermal Resistance, Junction to Ambient (Note 5)	t<10s	$R_{ ext{ heta}JA}$	59	
Total Power Dissipation (Note 6)	T _A = +25°C	PD	1.8	W
	T _A = +70°C	FD	1.1	
Thermal Registeres, Junction to Ambient (Note 6)	Steady state	D	71	°C/W
Thermal Resistance, Junction to Ambient (Note 6)	t<10s	$R_{\theta JA}$	43	
Thermal Resistance, Junction to Case (Note 6)	$R_{\theta JC}$	11.8		
Operating and Storage Temperature Range		T _{J,} T _{STG}	-55 to +150	°C

Electrical Characteristics N-Channel Q2 (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)			•	•		·
Drain-Source Breakdown Voltage	BV _{DSS}	40	_	_	V	$V_{GS} = 0V, I_D = 250\mu A$
Zero Gate Voltage Drain Current	I _{DSS}	_	—	1	μA	V _{DS} = 40V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	_	—	±100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 8)						·
Gate Threshold Voltage	V _{GS(th)}	1.4	—	2.4	V	$V_{DS} = V_{GS}, I_D = 250 \mu A$
Static Drain-Source On-Resistance	D	_	15	24	m0	V _{GS} = 10V, I _D = 6A
	R _{DS(ON)}	_	20	32	mΩ	V _{GS} = 4.5V, I _D = 5A
Diode Forward Voltage	V _{SD}	_	0.7	1.0	V	V _{GS} = 0V, I _S = 1.0A
DYNAMIC CHARACTERISTICS (Note 9)						·
Input Capacitance	Ciss	—	1060	—		V _{DS} = 20V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	Coss	_	84	—	pF	
Reverse Transfer Capacitance	Crss	_	58	_		
Gate Resistance	R _G	_	1.6	_	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1.0MHz
Total Gate Charge (V _{GS} = 4.5V)	Qg	_	8.8	—		
Total Gate Charge (V _{GS} = 10V)	Qg	_	19.1	—	nC	V _{DS} = 20V. I _D = 8A
Gate-Source Charge	Q _{gs}	_	3.0	—		$v_{\rm DS} = 20v, I_{\rm D} = 6A$
Gate-Drain Charge	Q _{gd}	_	2.5	_		
Turn-On Delay Time	t _{D(on)}		5.3	_		V _{DD} = 25V, R _L = 2.5Ω
Turn-On Rise Time	tr		7.1	_	nS	
Turn-Off Delay Time	t _{D(off)}		15.1	_	ns	V_{GS} = 10V, R_G = 3 Ω
Turn-Off Fall Time	tf		4.8	_	1	
Body Diode Reverse Recovery Time	t _{rr}		10.5	—	nS	I _F = 8A, di/dt = 100A/μs
Body Diode Reverse Recovery Charge	Q _{rr}	_	4.15	_	nC	I _F = 8A, di/dt = 100A/µs

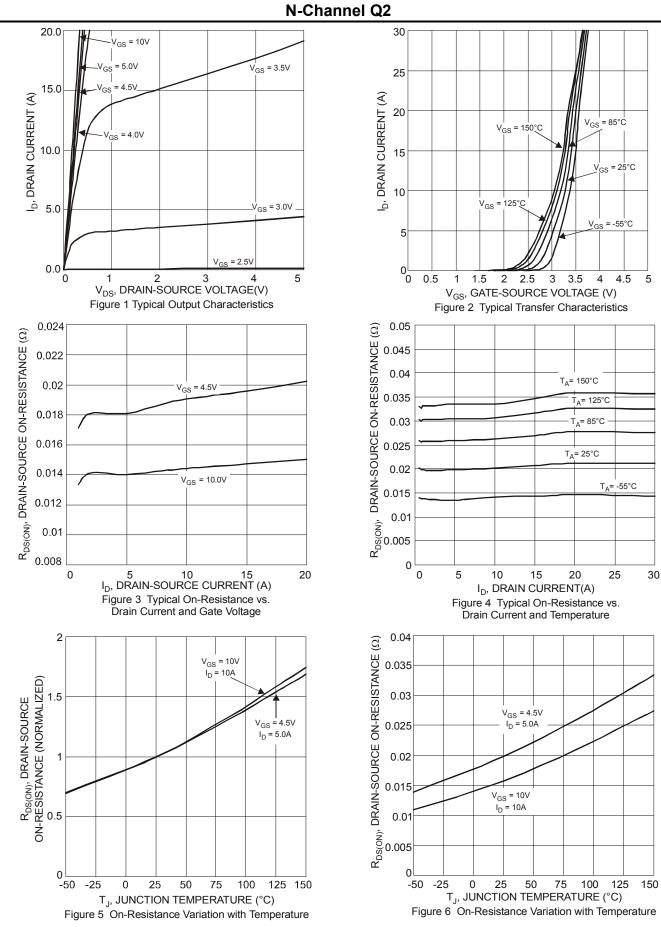


Electrical Characteristics P-Channel Q1 (@T_A = +25°C, unless otherwise specified.)

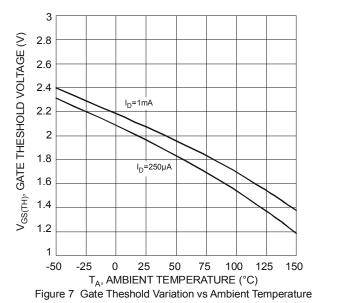
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)				•		
Drain-Source Breakdown Voltage	BV _{DSS}	-40	_		V	V _{GS} = 0V, I _D = -250µA
Zero Gate Voltage Drain Current	I _{DSS}	_		-1	μA	V_{DS} = -40V, V_{GS} = 0V
Gate-Source Leakage	I _{GSS}	_	_	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	V _{GS(th)}	-1.0	_	-2.2	V	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$
Statia Drain Course On Desistance		_	33	45		V _{GS} = -10V, I _D = -5A
Static Drain-Source On-Resistance	R _{DS(ON)}		40	55	mΩ	V _{GS} = -4.5V, I _D = -4A
Diode Forward Voltage	V _{SD}	_	-0.7	-1.0	V	V _{GS} = 0V, I _S = -1.0A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C _{iss}		1154	_		V _{DS} = -20V, V _{GS} = 0V f = 1.0MHz
Output Capacitance	C _{oss}	_	84	_	pF	
Reverse Transfer Capacitance	Crss	_	66	_		
Gate Resistance	R _G	_	12.6	_	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz
Total Gate Charge (V _{GS} = -4.5V)	Qg	_	10.6	_		
Total Gate Charge (V _{GS} = -10V)	Qg	_	21.5	_		VDS = -20V, ID = -4.9A
Gate-Source Charge	Q _{gs}	_	2.2	_	nC	
Gate-Drain Charge	Q _{gd}	_	3.3	_		
Turn-On Delay Time	t _{D(on)}	_	8.7	_		V _{DS} = -20V, I _D = -3.9A V _{GS} = -4.5V, R _G = 1Ω
Turn-On Rise Time	tr		19.6		1	
Turn-Off Delay Time	t _{D(off)}	_	34.9		nS	
Turn-Off Fall Time	t _f	_	25.5	_		
Body Diode Reverse Recovery Time	t _{rr}		9.61	_	nS	I _S = -3.9A, dl/dt = 100A/µs
Body Diode Reverse Recovery Charge	Q _{rr}		3.30	_	nC	I _S = -3.9A, dl/dt = 100A/µs

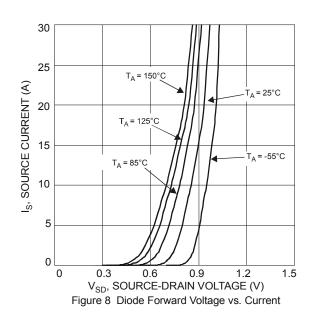
 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
 6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
 7. IAR and EAR rating are based on low frequency and duty cycles to keep TJ = +25°C
 8. Short duration pulse test used to minimize self-heating effect.
 9. Guaranteed by design. Not subject to product testing. Notes:





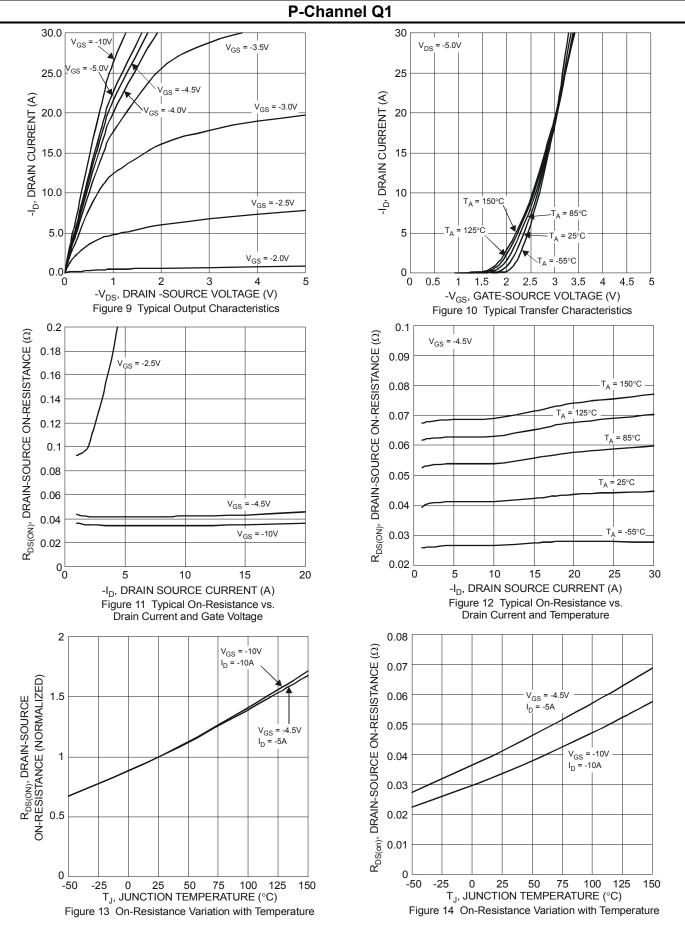








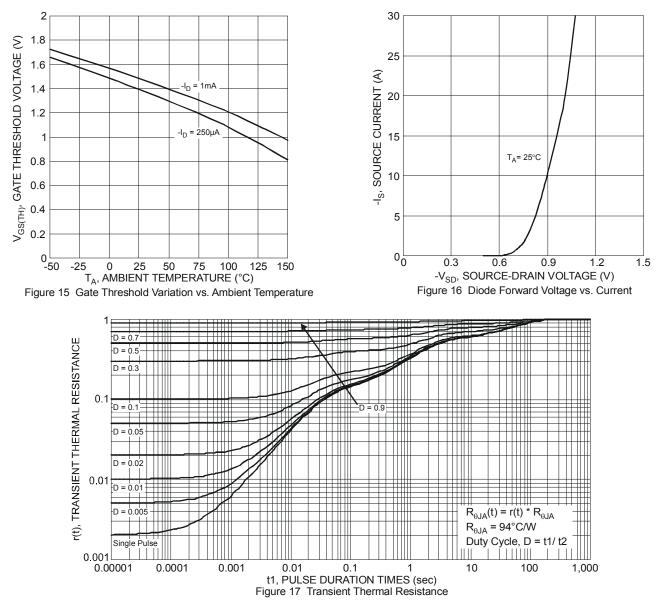
DMC4047LSD



DMC4047LSD Document number: DS36206 Rev. 4 - 2 6 of 9 www.diodes.com



DMC4047LSD





Max 1.75

0.20

1.50

0.25

0.5

4.95

6.10

3.95

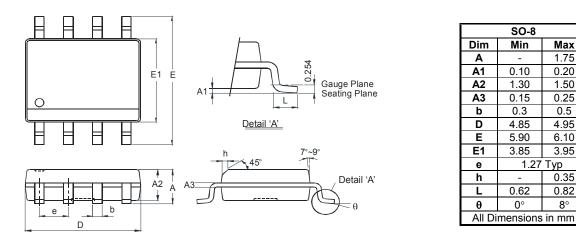
0.35

0.82

8°

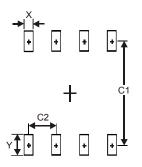
Package Outline Dimensions

Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.



Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



Dimensions	Value (in mm)
Х	0.60
Y	1.55
C1	5.4
C2	1.27



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