

***SED2020***  
***CMOS VFD Driver***  
***Technical Manual***

***S-MOS Systems, Inc.***  
***October, 1996***  
***Version 1.0 (Preliminary)***

S-MOS Systems, Inc. • 150 River Oaks Parkway • San Jose, CA 95134 • Tel: (408) 922-0200 • Fax: (408) 922-0238

■ 7932909 0004041 754 ■

**THIS PAGE INTENTIONALLY BLANK**

---

## Table of Contents

---

<b>1.0 GENERAL DESCRIPTION .....</b>	<b>5</b>
1.1 Description .....	5
1.2 Features .....	5
<b>2.0 BLOCK DIAGRAM .....</b>	<b>7</b>
<b>3.0 PIN CONFIGURATION .....</b>	<b>9</b>
3.1 SED2020FOA .....	9
3.2 SED2020FOB .....	10
3.3 Pin Description .....	11
<b>4.0 ELECTRICAL CHARACTERISTICS .....</b>	<b>13</b>
4.1 Absolute Maximum Ratings .....	13
4.2 Recommended Operating Conditions .....	13
4.3 DC Electrical Characteristics .....	14
4.4 AC Electrical Characteristics .....	14
4.5 Timing Chart .....	15
<b>5.0 TYPICAL CONNECTIONS .....</b>	<b>17</b>
5.1 Example of connecting SED2020F's to VFD (1) <1 bit serial> .....	17
5.2 Example of connecting SED2020F's to VFD (2) <4 bits serial> .....	18

**THIS PAGE INTENTIONALLY BLANK**

## **1.0 GENERAL DESCRIPTION**

### **1.1 DESCRIPTION**

The SED2020F<sub>OAVOB</sub> is a CMOS LSI dot-matrix vacuum fluorescent display anode and grid driver. It has 20 high-voltage anode outputs in 2 × 10 blocks.

The SED2020F<sub>OAVOB</sub> is TTL, LSTTL, CMOS and HSCMOS compatible, allowing direct interface to a wide range of standard devices. It has independent serial inputs and outputs for each 10-element block which feature data transfer rates of up to 4 Mbits/s. All inputs have internal pull-ups and serial outputs have a minimum fanout of one standard TTL load. The serial data transfer system simplifies controller requirements. The SED2020F<sub>OAVOB</sub> can also be configured for 4-bit parallel data transfer.

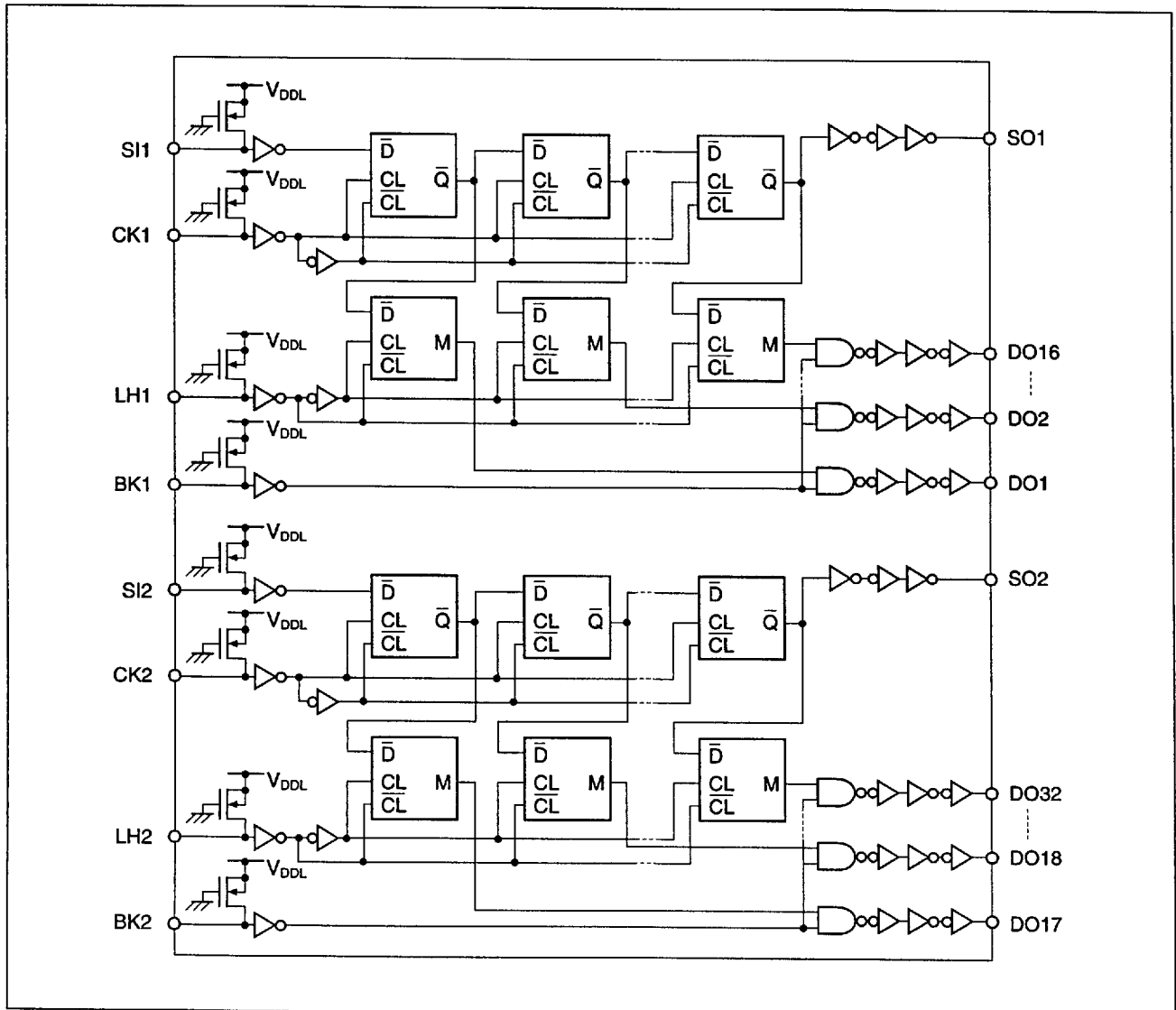
SED2020F<sub>OAVOB</sub> uses a 5V logic supply and a 30 to 70V display supply, and is available in 44- or 46-pin plastic flatpacks.

### **1.2 FEATURES**

- 20 anode or grid output drivers
- 70V, 10mA grid drive capability
- Up to 4 Mbits/s serial data transfer rate
- Daisy-chain data transfer system for cascaded operation
- Can be configured for 4-bit parallel data transfer
- Silicon-gate CMOS technology
- 5V logic supply
- 30 to 70V display supply
- 44- or 46-pin plastic flatpack (QFP2-44pin [F<sub>OB</sub>] and QFP1-46pin [F<sub>OA</sub>])

THIS PAGE INTENTIONALLY BLANK

## 2.0 BLOCK DIAGRAM

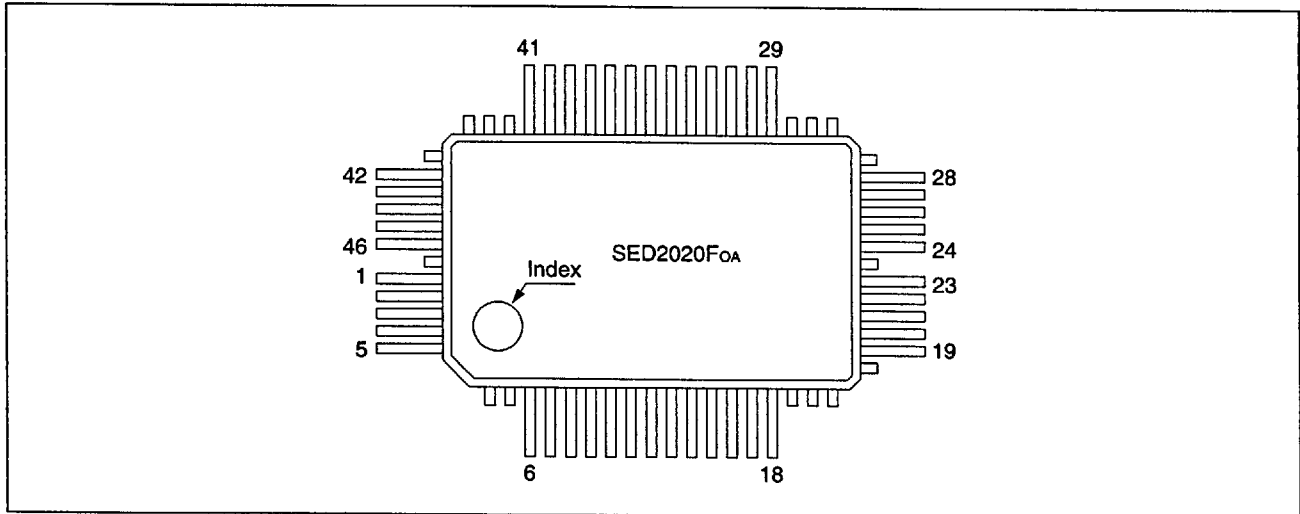


THIS PAGE INTENTIONALLY BLANK



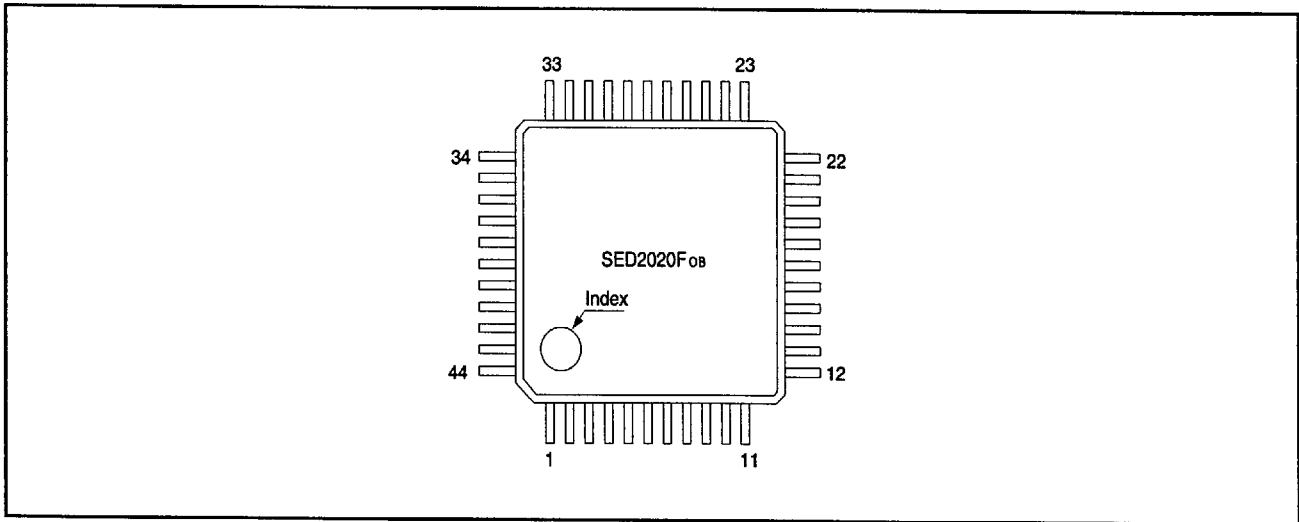
### 3.0 PIN CONFIGURATION

#### 3.1 SED2020F<sub>0A</sub>



Pin		Pin		Pin		Pin	
Number	Name	Number	Name	Number	Name	Number	Name
1	SI2	13	DO16	25	NC	37	DO3
2	CK2	14	DO17	26	SO1	38	DO2
3	LH2	15	DO18	27	NC	39	DO1
4	V <sub>DDL</sub>	16	DO19	28	NC	40	NC
5	V <sub>SS</sub>	17	DO20	29	NC	41	NC
6	V <sub>DDH</sub>	18	NC	30	DO10	42	BK2
7	NC	19	NC	31	DO9	43	BK1
8	DO11	20	NC	32	DO8	44	LH1
9	DO12	21	SO2	33	DO7	45	CK1
10	DO13	22	NC	34	DO6	46	SI1
11	DO14	23	NC	35	DO5		
12	DO15	24	NC	36	DO4		

3.2 SED2020F<sub>08</sub>



Pin		Pin		Pin		Pin	
Number	Name	Number	Name	Number	Name	Number	Name
1	V <sub>DDH</sub>	12	NC	23	DO10	34	BK2
2	DO11	13	NC	24	DO9	35	BK1
3	DO12	14	NC	25	DO8	36	NC
4	DO13	15	SO2	26	DO7	37	LH1
5	DO14	16	NC	27	DO6	38	CK1
6	DO15	17	NC	28	DO5	39	SI1
7	DO16	18	NC	29	DO4	40	SI2
8	DO17	19	NC	30	DO3	41	CK2
9	DO18	20	SO1	31	DO2	42	LH2
10	DO19	21	NC	32	DO1	43	V <sub>DDL</sub>
11	DO20	22	NC	33	NC	44	V <sub>SS</sub>

## 3.0 Pin Configuration

3.3 – 3.3

### 3.3 PIN DESCRIPTION

Number		Name	Description
SED2020F <sub>0A</sub>	SED2020F <sub>0B</sub>		
1	40	SI2	Serial data input 2
2	41	CK2	Serial data input clock 2
3	42	LH2	Active-HIGH data latch input 2
4	43	V <sub>DDL</sub>	5V logic supply input
5	44	V <sub>SS</sub>	Ground
6	1	V <sub>DDH</sub>	30 to 70V output driver supply input. Referenced to V <sub>SS</sub>
7	36	NC	No connection
8 to 17	2 to 11	DO11 to DO20	Parallel data outputs
18 to 20	12 to 14	NC	No connection
21	15	SO2	Serial data output 2
22 to 25	16 to 19	NC	No connection
26	20	SO1	Serial data output 2
27 to 29	21, 22	NC	No connection
30 to 39	23 to 32	DO10 to DO1	Parallel data outputs
40, 41	33	NC	No connection
42	34	BK2	Active-HIGH blanking input 2. Used to disable output circuitry while parallel data is being latched.
43	35	BK1	Active-HIGH blanking input 1. Used to disable output circuitry while parallel data is being latched.
44	37	LH1	Active-HIGH data latch input 1
45	38	CK1	Serial data input clock 1
46	39	SI1	Serial data input 1

**THIS PAGE INTENTIONALLY BLANK**

## 4.0 ELECTRICAL CHARACTERISTICS

### 4.1 ABSOLUTE MAXIMUM RATINGS

 $V_{SS} = 0V, T_a = -10 \text{ to } 70^\circ\text{C}$ 

Parameter	Symbol	Ratings	Unit
Supply voltage (driver)	$V_{DDH}$	-0.3 to 70	V
Supply voltage (logic)	$V_{DDL}$	-0.3 to 7	V
Driver output voltage	$V_{DO}$	$V_{SS} - 0.3$ to $V_{DDH} + 0.3$	V
Input/output voltage	$V_{IO}$	$V_{SS} - 0.3$ to $V_{DDL} + 0.3$	V
Driver high level output current	$I_{OHDO}$	-15 to 0	mA
Driver low level output current	$I_{OLDO}$	0 to 3	mA
Power dissipation	$P_D$	0 to 250	mW
Operating temperature	$T_{OPR}$	-10 to 70	$^\circ\text{C}$
Storage temperature	$T_{STG}$	-65 to 150	$^\circ\text{C}$
Soldering temperature and time	$T_{SOL}$	260 $^\circ\text{C}$ , 10s (at lead)	—

### 4.2 RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage (driver)	$V_{DDH}$		30	60	70	V
Supply voltage (logic)	$V_{DDL}$		4.5	5.0	5.5	V
Input voltage	$V_I$		0	—	$V_{DDL}$	V
Input logic level	$V_{LL}$	TTL input level	—	1.55	—	
Driver high level output current	$I_{OHDO}$	Grid output	—	-10	—	mA
		Anode output	—	-0.5	—	mA
Clock frequency	$f_{clock}$	Cascade connection	0	—	4	MHz
Clock pulse width	$tw_{clock}$		125	—	—	ns
Setup time	$t_{setup}$		125	—	—	ns
Hold time	$t_{hold}$		0	—	—	ns
Latch pulse width	$tw_{latch}$		250	—	—	ns

## 4.3 DC ELECTRICAL CHARACTERISTICS

 $V_{DDL} = 5V, V_{DDH} = 60V, T_a = 25^\circ C$ 

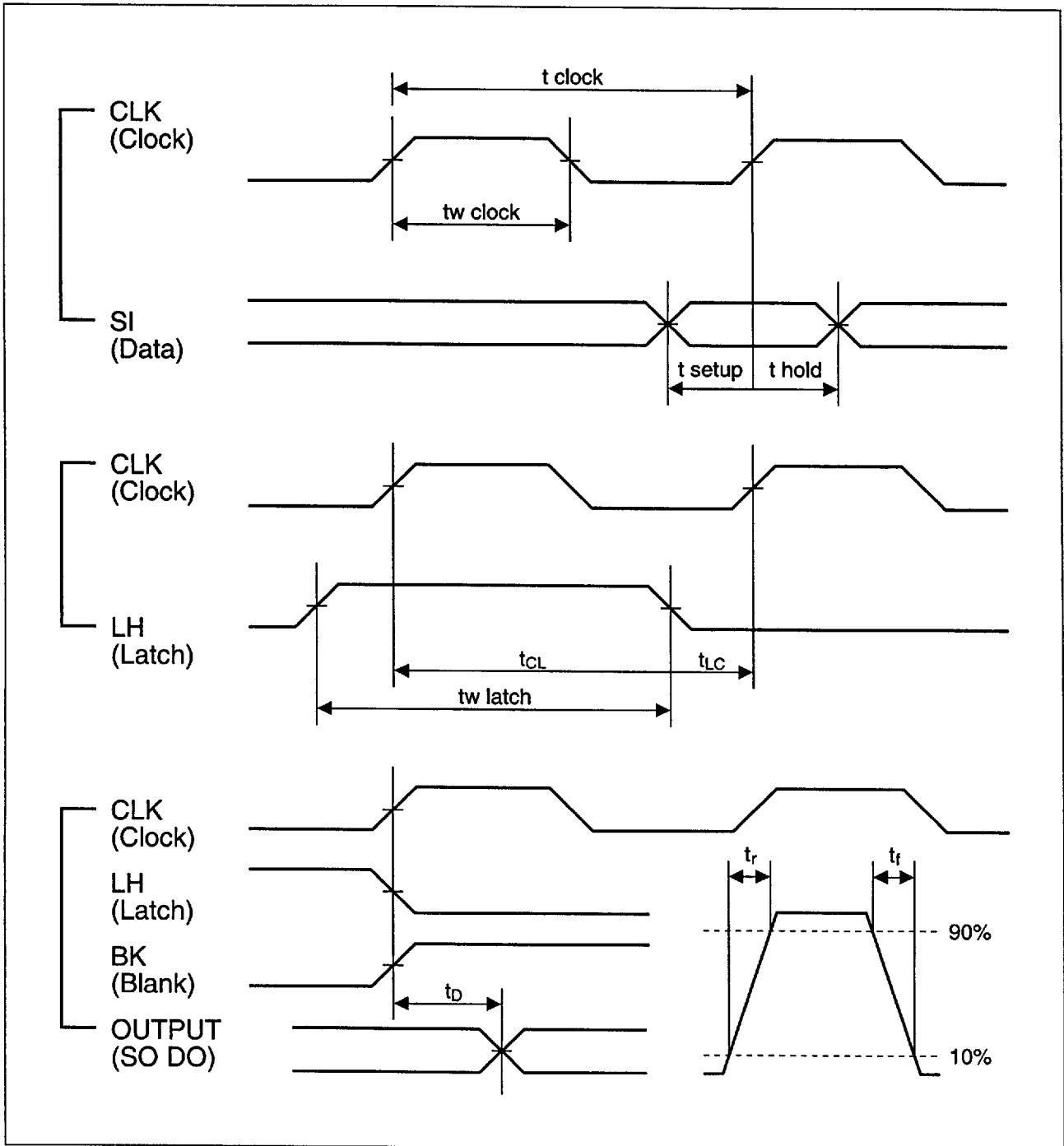
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High level input voltage	$V_{IH}$		2.4	—	$V_{DDL}$	V
Low level input voltage	$V_{IL}$		0	—	0.7	V
High level input current	$I_{IH}$	$V_{IH} = 5.3V$	—	33	100	$\mu A$
Low level input current	$I_{IL}$	$V_{IL} = 0V$	-160	-100	—	$\mu A$
High level output current	$I_{OH(SO)}$	$V_{OH} = 4.6V$	—	-1.4	-0.44	mA
Low level output current	$I_{OL(SO)}$	$V_{OL} = 0.4V$	1.6	2.1	—	mA
Supply current ( $V_{DDL}$ )	$I_{DDL}$	f clock = 4MHz	—	—	5	mA
Supply current ( $V_{DDH}$ )	$I_{DDH}$	At all drivers output "H"	—	—	2.0	mA
Driver high level output current	$I_{OHDO}$	$V_{OHDO} = 55V$ at output "H"	—	—	-10	mA
Driver low level output current	$I_{OLDO}$	$V_{OLDO} = 5V$ at output "L"	1	—	—	mA

## 4.4 AC ELECTRICAL CHARACTERISTICS

 $V_{DDL} = 5V, V_{DDH} = 60V, T_a = 25^\circ C$ 

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Clock latch delay time	tCL	1. Input signal conditions (1) Amplitude: 0–5V (2) Rise/fall time should be 15ns or less. (3) Measuring voltage should be 2.5V.	125	—	—	ns
Latch clock delay time	tLC		0	—	—	ns
Output(SO) rise time	tr (SO)		—	—	50	ns
Output(SO) fall time	tf (SO)	2. Output signal conditions (1) Standard loads are: 13pF, 10M $\Omega$ (2) Measuring voltage should be 2.5V or 1/2 of the amplitude.	—	—	50	ns
Clock(SO) delay time	tp (SO)		—	—	125	ns
Output(DO) rise time	tr (DO)		—	—	1	$\mu s$
Output(DO) fall time	tf (DO)		—	—	1	$\mu s$
BK–DO transfer time	tp (DO)		—	—	2	$\mu s$

4.5 TIMING CHART



4.5 – 4.5

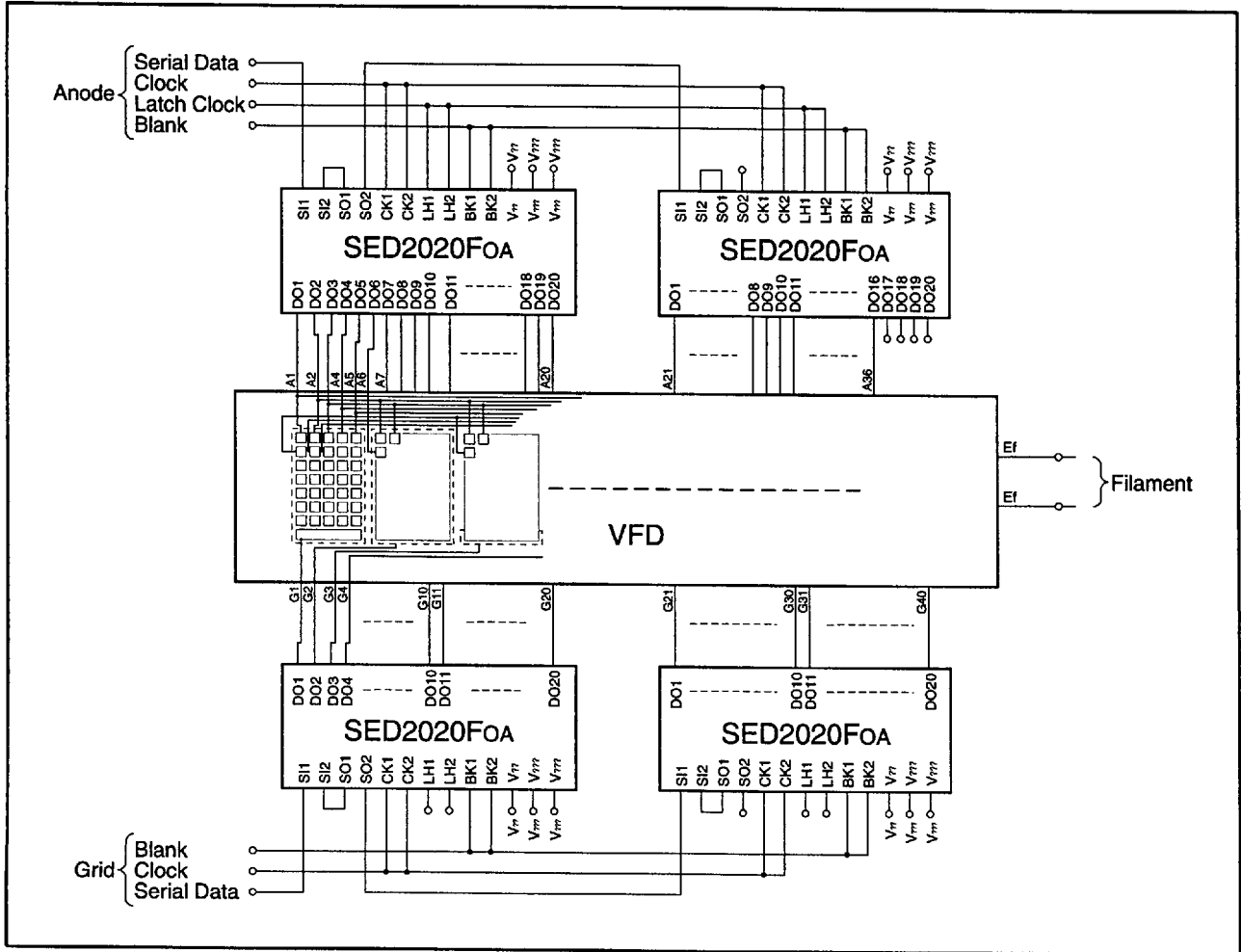
## 4.0 Electrical Characteristics

**THIS PAGE INTENTIONALLY BLANK**



# 5.0 TYPICAL CONNECTIONS

## 5.1 EXAMPLE OF CONNECTING SED2020F'S TO VFD (1) <1 BIT SERIAL>



5.2 EXAMPLE OF CONNECTING SED2020F'S TO VFD (2) <4 BITS SERIAL>

