Preliminary

MOS Memories

FUJITSU

■ MB811000-12, MB811000-15

1,048,576-Bit Dynamic Random Access Memory

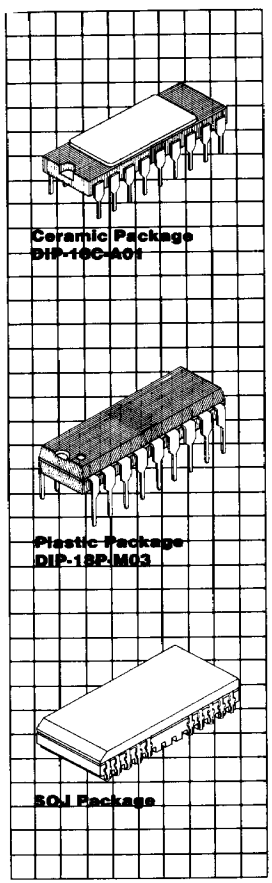
Description

The Fujitsu MB811000 is a fully decoded, dynamic NMOS random access memory organized as 1,048,576 one-bit words. The design is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

The MB811000 features "page mode" which allows high speed random access of up to 1024-bits within the same row. Additionally, the MB811000 offers new functional enhancements that make it more versatile than previous dynamic RAMs. Multiplexed row and column address inputs permits the MB811000 to be housed in a Jedec standard 18-pin dual in-line package or 20 lead SOJ package.

The MB811000 is fabricated using silicon gate NMOS and Fujitsu's advanced Triple-layer Polysilicon process. This process, coupled with an innovative stacked capacitor memory cell, permits maximum circuit density and minimal chip size. Dynamic circuitry is used in the design, including dynamic sense amplifiers.

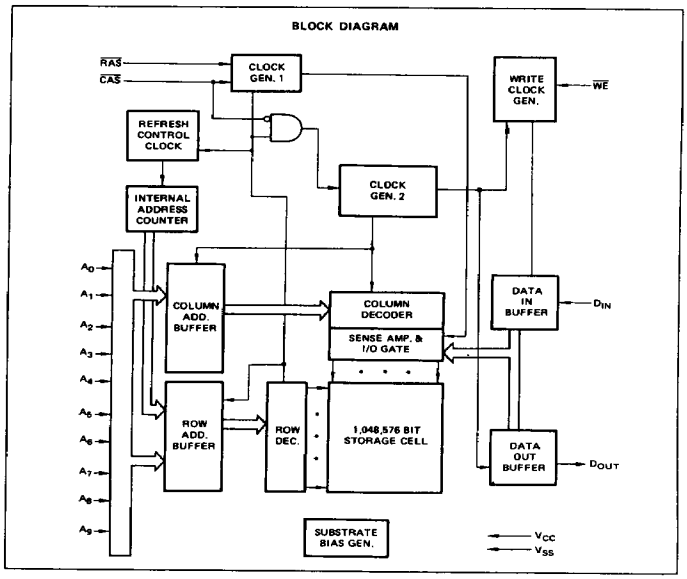
Clock timing requirements are noncritical, and the power supply tolerance is very wide. All inputs are TTL compatible.

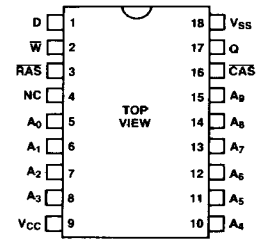


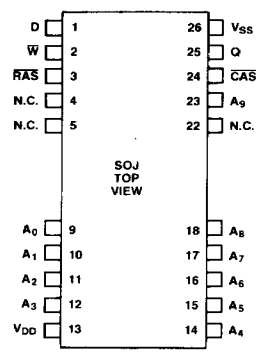
Features

- 1,048,576 x 1-bit organization
- Silicon-gate, NMOS, single transistor cell
- Access time (t_{RAC})
  120 ns max. (MB811000-12)
  150 ns max. (MB811000-15)
- Cycle time (t_{RC})
  230 ns min. (MB811000-12)
  260 ns min. (MB811000-15)
- Page cycle time (t_{PC})
  120 ns min. (MB811000-12)
  150 ns min. (MB811000-15)
- Single 5V supply, ±10% tolerance
- Low power dissipation
  550 mW max. (MB811000-12)
  490 mW max. (MB811000-15)
  25 mW max. at standby
- Refresh 8 ms/512 cycles
- $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$ and hidden refresh capability
- High speed read-write cycle capability
- Output unlatched at cycle end allows two dimensional chip select
- On chip address and data-in latches
- Industry standard 18-pin DIP package

MB811000 Block Diagram and Pin Assignment







Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} relative to V_{SS}	V_{CC}	−1 to +7	V
Storage temperature Ceramic / Plastic	T_{STG}	−55 to +150 / −55 to +125	°C
Power dissipation	P_D	1.0	W
Short circuit output current		50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Recommended Operating Conditions

(Referenced to V_{SS})

Parameter	Symbol	Value Min	Value Typ	Value Max	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C (ambient)
	V_{SS}	0	0	0	V	
Input High Voltage All Inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage All Inputs	V_{IL}	−2.0		0.8	V	

Capacitance
($T_A = 25°C$)

Parameter	Symbol	Value Min	Typ	Max	Unit
Input Capacitance A_0 to A_8, D	C_{IN1}			7	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$	C_{IN2}			8	pF
Output Capacitance Q	C_{OUT}			7	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB811000-12 Min	MB811000-12 Max	MB811000-15 Min	MB811000-15 Max	Unit
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = Min.)	I_{CC1}		100		90	mA
STANDBY CURRENT Power Supply Current ($\overline{RAS}$/$\overline{CAS}$ = V_{IH})	I_{CC2}		4.5		4.5	mA
REFRESH CURRENT 1* Average Power Supply Current ($\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH}; t_{RC} = Min.)	I_{CC3}		90		80	mA
PAGE MODE CURRENT* Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = Min.)	I_{CC4}		45		40	mA
REFRESH CURRENT 2* Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$; t_{RC} = Min.)	I_{CC5}		90		80	mA
INPUT LEAKAGE CURRENT Any Input, (V_{IN} = 0V to 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)	I_{IL}	−10	10	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data is disabled, V_{OUT} = 0V to 5.5V)	I_{OL}	−10	10	−10	10	μA
OUTPUT LEVEL Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}		0.4		0.4	V
OUTPUT LEVEL Output High Voltage (I_{OH} = −5.0 mA)	V_{OH}	2.4		2.4		V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol Alternate	Symbol *Standard	MB811000-12 Min	MB811000-12 Max	MB811000-15 Min	MB811000-15 Max	Unit
Time between Refresh		t_{REF}	TRVRV		8		8	ms
Random Read/Write Cycle Time		t_{RC}	TRELREL	230		260		ns
Read-Write Cycle Time		t_{RWC}	TRELREL	285		325		ns
Access Time from $\overline{RAS}$	*4,6	t_{RAC}	TRELQV		120		150	ns
Access Time from $\overline{CAS}$	*5,6	t_{CAC}	TCELQV		60		75	ns
Output Buffer Turn off Delay		t_{OFF}	TCEHQZ	0	25	0	35	ns
Transition Time		t_T	TT	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	TREHREL	100		100		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	TRELREH	120	100000	150	100000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	TCELREH	60		75		ns
$\overline{CAS}$ Pulse Width		t_{CAS}	TCELCEH	60	100000	75	100000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	TRELCEH	120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	*4,7	t_{RCD}	TRELCEL	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	TCEXREL	0		0		ns
Row Address Set Up Time		t_{ASR}	TAVREL	0		0		ns
Row Address Hold Time		t_{RAH}	TRELAX	12		15		ns
Column Address Set Up Time		t_{ASC}	TAVCEL	0		0		ns
Column Address Hold Time		t_{CAH}	TCELAX	20		25		ns
Read Command Set Up Time		t_{RCS}	TWHCEL	0		0		ns
Read Command Hold Time Referenced to $\overline{CAS}$	*10	t_{RCH}	TCEHWX	0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	*10	t_{RRH}	TREHWX	20		20		ns
Write Command Set Up Time	*8	t_{WCS}	TWLCEL	0		0		ns
Write Command Pulse Width		t_{WP}	TWLWH	20		25		ns
Write Command Hold Time		t_{WCH}	TCELWH	20		25		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	TWLREH	50		60		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	TWLCEH	50		60		ns
Data In Set Up Time		t_{DS}	TDVCEL	0		0		ns
Data In Hold Time		t_{DH}	TCELDX	20		25		ns
$\overline{CAS}$ to $\overline{W}$ Delay	*8	t_{CWD}	TCELWL	60		75		ns
$\overline{CAS}$ Precharge Time (Normal Cycle)		t_{CPN}		22		25		ns
$\overline{RAS}$ to $\overline{W}$ Delay	*8	t_{RWD}		120		150		ns

Notes: *1. An initial pause of 200 μs is required after power up, followed by any 8 $\overline{RAS}$ cycles, before proper device operation is achieved. If the internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh initialization cycles are required.

*2. AC characteristics assume t_T = 5 ns.

*3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

*4. t_{RCD} is specified as a reference point only. If $t_{RCD} \leq t_{RCD}$ (Max.) the specified maximum value of t_{RAC} (Max.) can be met. If $t_{RCD} > t_{RCD}$ (Max.) then t_{RAC} in increased by the amount that t_{RCD} exceeds t_{RCD} (Max.)

*5. Assumes that $t_{RCD} > t_{RCD}$ (Max.).

*6. Measured with a load equivalent to 2 TTL loads and 100 pF.

*7. t_{RCD} (Min.) = t_{RAH} (Min.) + 2 t_T + t_{ASC} (Min.).

*8. t_{WCS} and t_{CWD} are non restrictive operating parameters, and are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$ (Min.), the cycle is an early write cycle, and the data out pin will remain open circuit (High Impedance) throughout the entire cycle.
If $t_{CWD} > t_{CWD}$ (Min.), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.

*10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol Alternate	Symbol *Standard	MB811000-12 Min	MB811000-12 Max	MB811000-15 Min	MB811000-15 Max	Unit
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$		t_{FCS}	TCELREL	0		0		ns
Refresh Hold Time for $\overline{CAS}$ Referenced to $\overline{RAS}$		t_{FCH}	TRELCEX	20		20		ns
Page Mode Read/Write Cycle Time		t_{PC}	TCELCEL	120		150		ns
Page Mode Read-Write Cycle Time		t_{PRWC}	TCEHCEH	175		215		ns
Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	TCEHCEL	50		65		ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time		t_{RPC}	TREHCEL	20		20		ns
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle		t_{CPR}	TCEHCEL	25		30		ns

Notes: *These symbols are described in IEEE STD. 662-1980: IEEE Standard terminology for semiconductor memory.

Description

Simplified Timing Requirement

The MB811000 has improved circuitry that eases timing requirements for high speed access operations. The MB811000 can operate under the conditions of t_{RCD} (max.) = t_{CAC}, thus providing optimal timing for address multiplexing. In addition, the MB811000 has minimal hold times for Addresses (t_{CAH}), Write-Enable (t_{WCH}) and Data-in (t_{DH}). The MB811000 provides higher throughput in inter-leaved memory system applications. Fujitsu has made the timing requirements that are referenced to $\overline{RAS}$ non-restrictive and deleted them from the data sheet. These include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. As a result, the hold times of the Column Address, D and $\overline{W}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{W}$ Delay) are not restricted by t_{RCD}.

Fast Read-Write Cycle

The MB811000 has a fast read-modify-write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{W}$ when $\overline{CAS}$ goes "low". When $\overline{W}$ is "low", the MB811000 goes into the early write mode in which the output floats and the common I/O bus can be used on the system level. When $\overline{W}$ goes "low", after t_{CWD} following a $\overline{CAS}$ transition to "low", the MB811000 goes into the delayed write mode. The output then contains the data from the cell selected and the data from D is written into the cell selected. Therefore, a very fast read-write cycle (t_{RWC} = t_{RC}) is possible with the MB811000.

Address Inputs

A total of twenty binary input address bits are required to decode any 1 of 1,048,576 cell locations within the MB811000. Ten row-address bits are established on the input pins (A_0 through A_9) and are latched with the Row Address Strobe ($\overline{RAS}$). Ten column address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All row addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold/Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row addresses to column addresses.

Write Enable

The read or write mode is selected with the $\overline{W}$ input. A logic "high" on $\overline{W}$ dictates read mode. A logic "low" dictates write mode. The data input is disabled when the read mode is selected.

Data Input

Data is written into the MB811000 during a write or read-write cycle. The last falling edge of $\overline{W}$ or $\overline{CAS}$ is a strobe for the data-in (D) register. In a write cycle, if $\overline{W}$ is brought "low" (write mode) before $\overline{CAS}$, D is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{W}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D is strobed by $\overline{W}$, and set-up and hold times are referenced to $\overline{W}$.

Data Output

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high impedance state until $\overline{CAS}$ is brought "low". In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when $t_{RCD(max)}$ is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after $t_{RCD(max)}$. Data remains valid until $\overline{CAS}$ in returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

Description
(Continued)

Page Mode

Page mode operation permits strobing the row address into the MB811000 while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row address doesn't change. Thus, the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Access and cycle times are decreased because the time normally required to strobe a new row address is eliminated.

$\overline{RAS}$-Only Refresh

Refresh of dynamic memory cells is accomplished by performing a memory cycle at each of the 512 row-addresses (A_0~ A_8) at least every 8 ms. $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought "low". Strobing each of the 512 row-addresses (A_0 ~ A_8) with $\overline{RAS}$ will cause all bits in each row to be refreshed. $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh

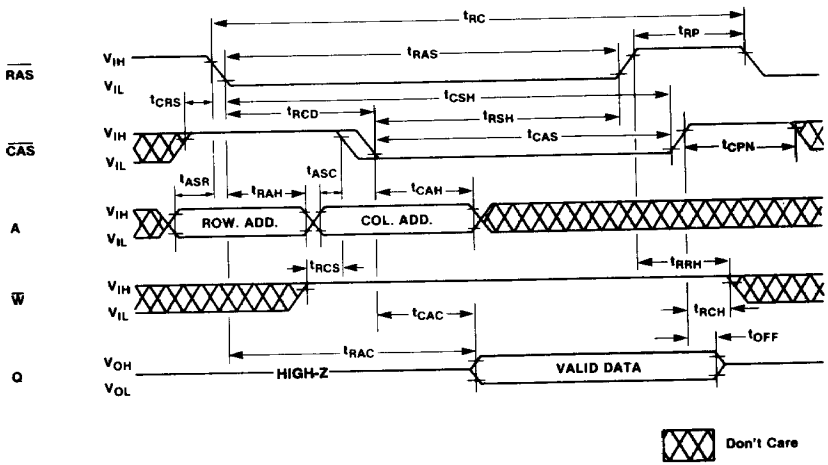
$\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB811000 offers an alternate refresh method. If $\overline{CAS}$ is held "low" for the specified period (t_{FCS}) before $\overline{RAS}$ goes to "low", on-chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

Hidden Refresh

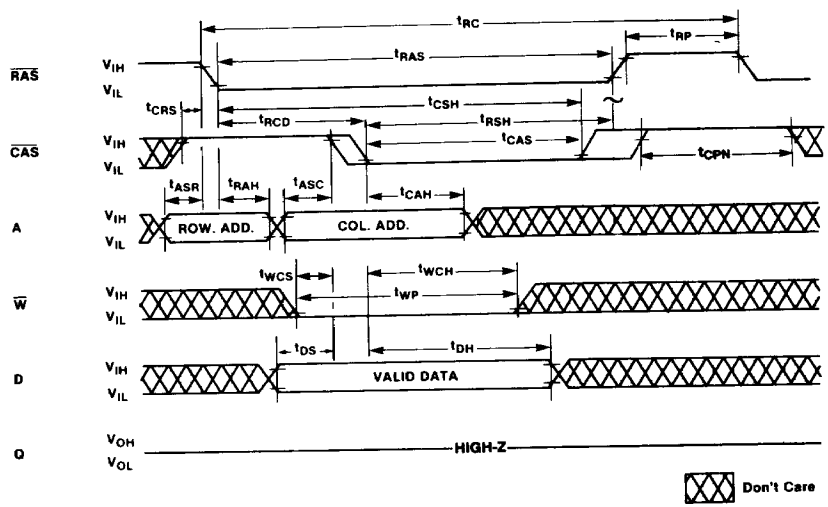
A hidden refresh cycle may take place while maintaining the latest valid data at the out-put by extending the $\overline{CAS}$ active time. For the MB811000, a hidden refresh cycle is a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. The internal refresh address counter provides the refresh addresses as in a normal $\overline{CAS}$-before-$\overline{RAS}$ cycle.

Timing Diagrams

Read Cycle

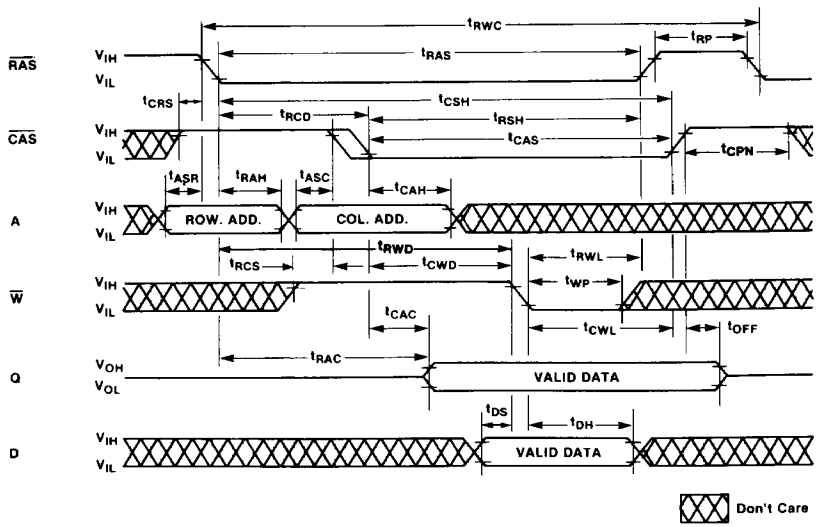


Write Cycle (Early Write)



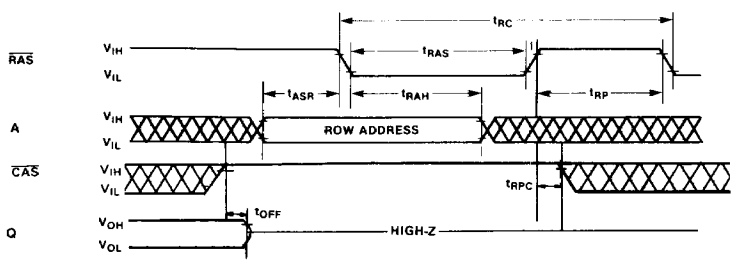
Timing Diagrams
(Continued)

Read-Write/Read-Modify-Write Cycle



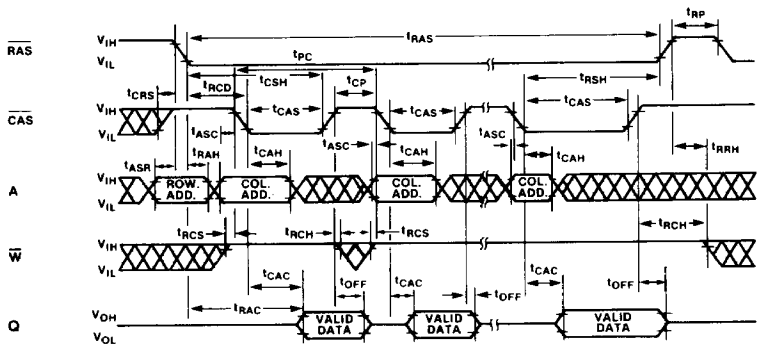
"RAS-Only" Refresh Cycle

NOTE: W, D = Don't Care, $A_9 = V_{IH}$ or V_{IL}

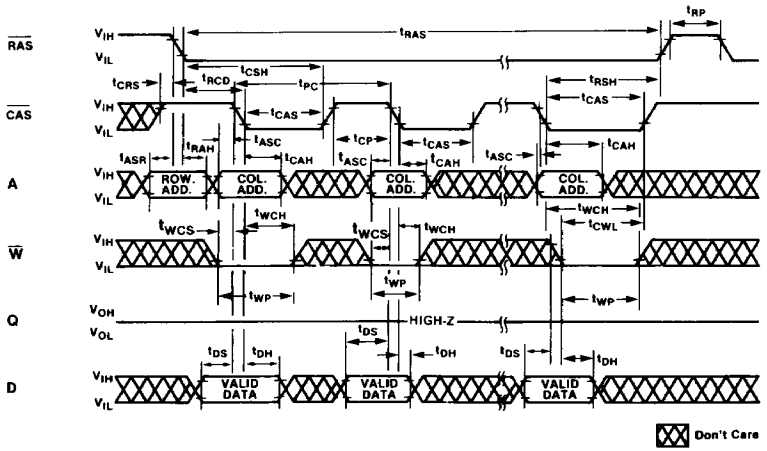


Timing Diagrams
(Continued)

Page Mode Read Cycle

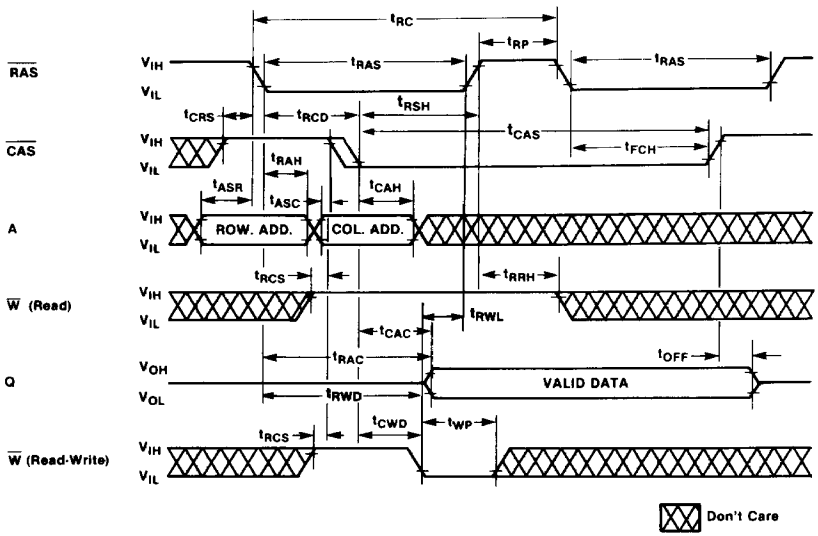


Page Mode Write Cycle

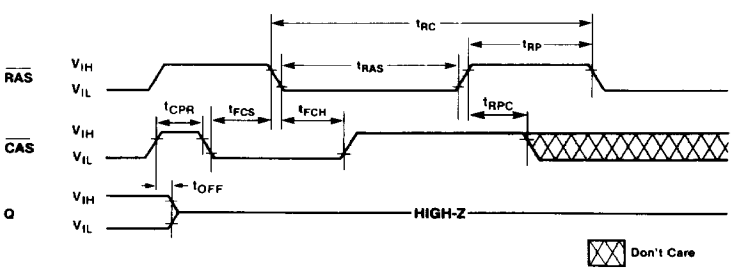


Timing Diagrams
(Continued)

Hidden Refresh Cycle

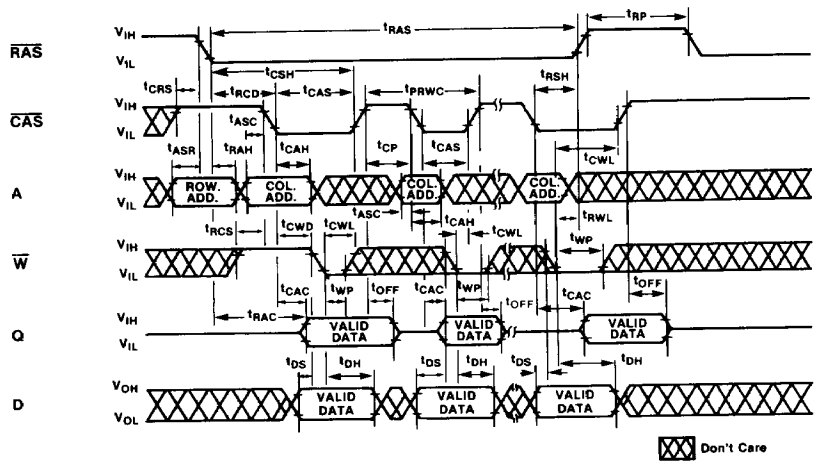


"CAS-Before-RAS" Refresh Cycle
NOTE: A, W, D = Don't Care



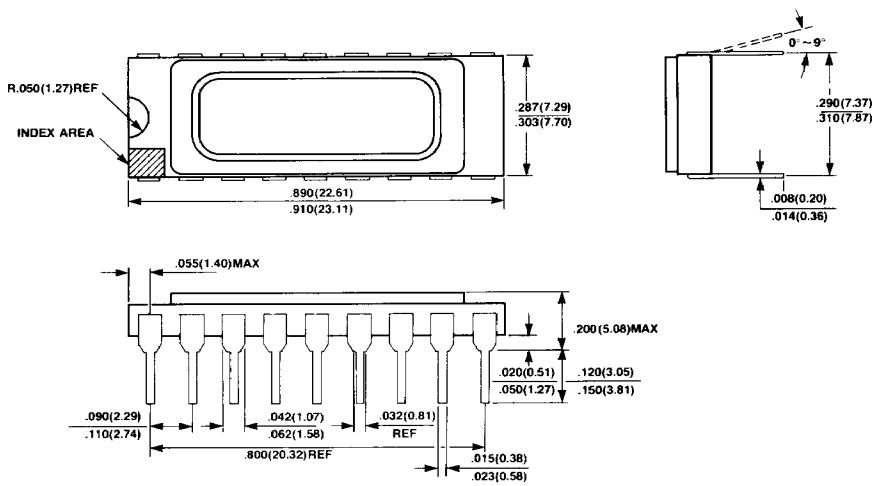
Timing Diagrams
(Continued)

Page Mode Read-Write Cycle

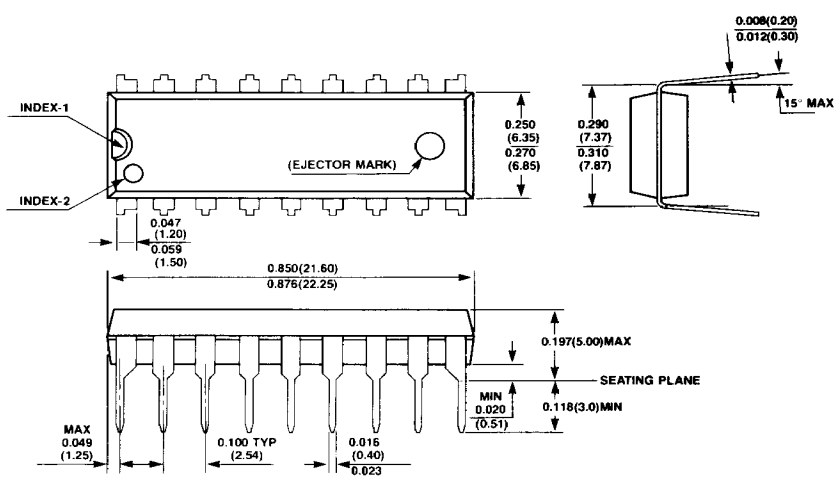


Package Dimensions
Dimensions in inches
(millimeter)

Ceramic Seam Weld Package
(DIP-18C-A01)



18 Lead Plastic Dual-In-Line Package
(DIP-18P-M03)



Package Dimensions
(Continued)
Dimensions in inches
(millimeter)

26 Lead SOJ Package