FUJITSU

CMOS 1,048,576 BIT UV ERASABLE READ ONLY MEMORY (EPROM)

MBM27C1024-15
MBM27C1024-20
MBM27C1024-25

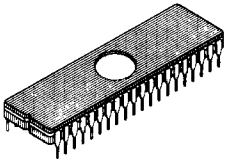
August 1988
Edition 1.0

CMOS 1,048,576 BIT UV ERASABLE READ ONLY MEMORY (EPROM)

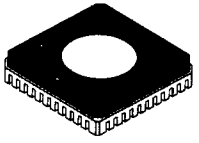
The Fujitsu MBM27C1024 is a high speed read-only static memory that is UV-erasable and reprogrammable. The devices contains 1,048,576 programmable or reprogrammable bits organized in a 65,536-word/16-bits format. The MBM27C1024 is housed in both 40-pin DIP and 44-pad LCC package with a transparent lid; when the lid is properly exposed to an ultraviolet light source, a previously programmed bit pattern is erased in approximately 12 to 21 minutes. A new bit pattern can then be written into memory.

The MBM27C1024 is fabricated using CMOS double poly-silicon gate technology with stacked single-transistor gate cells. The MBM27C1024 is an excellent choice for system development work and in other applications where programmed, the device requires only a single +5V power supply; the current requirements are exceptionally low in both the acitve and standby modes of operation.

- 65,536 words x 16 bit organization, with on chip decoding
- One-word or two-word programming capability with Quick-Pro™ algorithm
- Static operation (no clocks required)
- Easy and simple memory expansion via $\overline{OE}$
- High active bus enables $\overline{PGM}$
- Three-state output for wired-OR capability
- Fast access time:
  150ns max. (MBM27C1024-15)
  200ns max (MBM27C1024-20)
  250ns max. (MBM27C1024-25)
- Single +5V(±10%) power supply with low current drain:
  Active operation = 30mA (max) for 200ns/250ns
  40mA (max) for 150ns
  Standby operation = 0.1mA (max)
- Programming voltage: 12.5V
- JEDEC approved pin assignment
- 40-pin Ceramic(Cerdip) DIP Package: suffix =Z
- 44-pad Frit seal LCC package: Suffix =TV

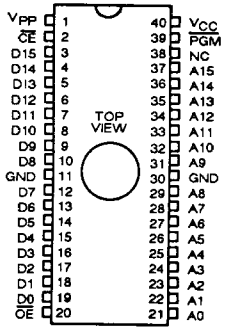


CERAMIC PACKAGE
DIP-40C-C02



CERAMIC PACKAGE
LCC-44C-F01

PIN ASSIGNMENT



LCC : See page 11

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
V_{CC} Supply Voltage with respect to GND	V_{CC}	-0.6 to 7.0	V
V_{PP} Supply Voltage with respect to GND	V_{PP}	-0.6 to 14.0	V
All Input/Output Voltage except for A_9 with respect to ground	$V_{IN\ 1}$	-0.6 to V_{CC} +0.3	V
A9 Voltage with respect to GND	$V_{IN\ 2}$	-0.6 to + 13.5	V
Temperature under Bias	T_{BIAS}	-25 to + 85	°C
Storage Temperature Range	T_{STG}	-65 to + 125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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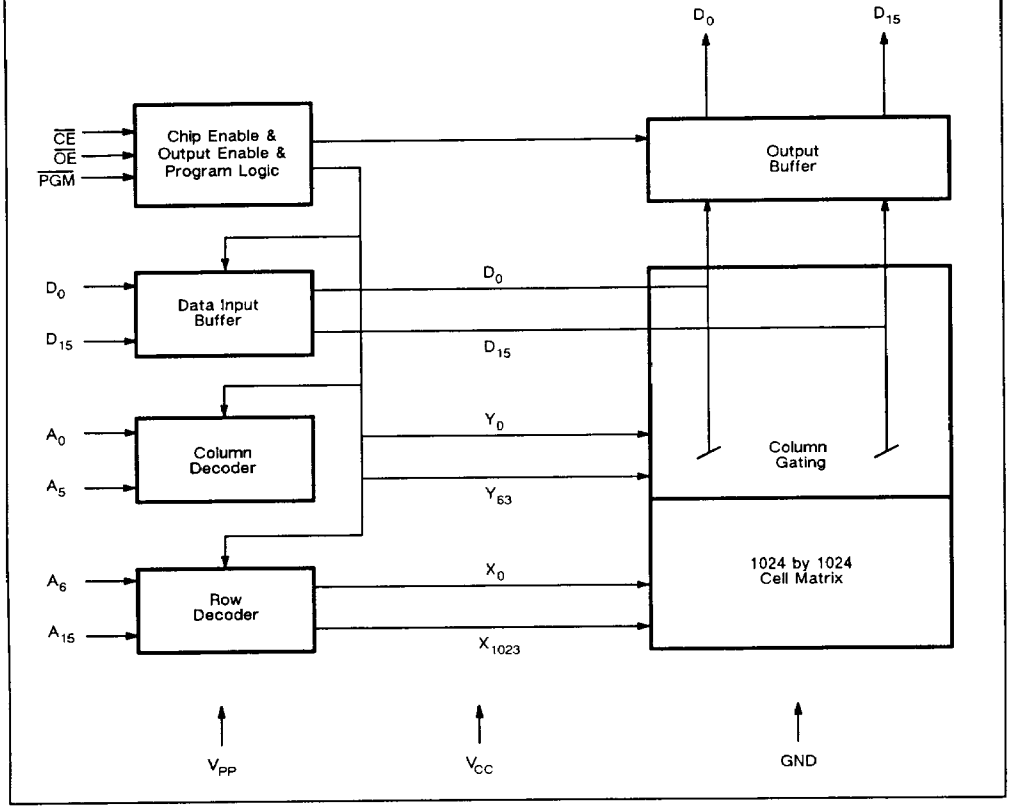
Fig. 1 — BLOCK DIAGRAM



CAPACITANCE (T_A = 25 °C, f = 1MHz)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Input Capacitance (V_{IN} = 0V)	C_{IN}		10	12	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}		10	12	pF

PIN DESCRIPTION

Symbol	Pin No. *	Function
V_{PP}	1	+5V power supply. When +12.5V is applied, the device is enabled for programming operation.
$\overline{CE}$	2	Chip enable. When active Low, the device is enabled for data read and programming operations.
$D_0 - D_{15}$	19-12, 10-3	Three-state output data line.
GND	11,30	Circuit ground.
$\overline{OE}$	20	Output enable. When active Low, all output lines are enabled.
$A_0 - A_{15}$	21-29, 31-37	Address lines.
NC	38	No connection.
$\overline{PGM}$	39	Program.
V_{CC}	40	+5V power supply

*This numbers are applied to DIP package.

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FUNCTIONAL TRUTH TABLE

MODE	A_0-A_8	A_9	A_{10} - A_{15}	Data	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{CC}	V_{PP}	GND
Standby	X	X	X	Hi-Z	V_{IH}	X	X	5V	5V	0V
Read	A_{IN}	A_{IN}	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	5V	5V	0V
Output Disable	A_{IN}	A_{IN}	A_{IN}	Hi-Z	V_{IL}	V_{IH} / X	X / V_{IL}	5V	5V	0V
One-Word Program	A_{IN}	A_{IN}	A_{IN}	D_{IN}	V_{IL}	V_{IH}	V_{IL}	6V	12.5V	0V
One-Word Verify	A_{IN}	A_{IN}	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	6V	12.5V	0V
One-Word Program Inhibit	A_{IN}	A_{IN}	A_{IN}	Hi-Z	V_{IL}	V_{IH}	V_{IH}	6V	12.5V	0V
Two-Word Data Input	A_{IN}*	A_{IN}	A_{IN}	D_{IN}	V_{IH}	V_{IH}	V_{IH}	6V	12.5V	0V
Two-Word Program	A_{IN}*	A_{IN}	A_{IN}	Hi-Z	V_{IH}	V_{IL}	V_{IL}	6V	12.5V	0V
Two-Word Verify	A_{IN}*	A_{IN}	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	6V	12.5V	0V
Two-Word Program Inhibit	A_{IN}	A_{IN}	A_{IN}	Hi-Z	V_{IH}	V_{IL}	V_{IH}	6V	12.5V	0V
Electronic Signature	A_{IN}*	12V	X	CODE	V_{IL}	V_{IL}	V_{IH}	5V	5V	0V

Legend: X = Don't care
A_{IN} = Address input
D_{IN} = Data input
D_{OUT} = Data output

Notes: *. A_0 is toggling address.

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
V_{PP} Supply Voltage	V_{PP}	V_{CC} -0.6	V_{CC}	V_{CC} +0.6	V
Operating Temperature	T_A	0		70	°C

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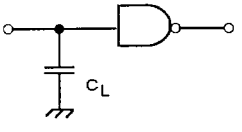
DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Conditions	Symbol	Values			Unit
			Min	Typ	Max	
Input Leakage Current	$V_{IN} = V_{CC} = 5.5V$	I_{LI}	-10		10	µA
Output Leakage Current	$V_{OUT} = V_{CC} = 5.5V$	I_{LO}	-10		10	µA
V_{CC} Standby Current	$\overline{CE}=V_{IH}$	I_{SB_1}			1	mA
V_{CC} Standby Current	$\overline{CE}=V_{CC}\pm0.3V$	I_{SB_2}		1	100	µA
V_{CC} Active Current	$\overline{CE}=V_{IL}$, I_{OUT} =0mA	I_{CC_1}			30	mA
V_{CC} Operation Current 150 ns / 200ns/250ns	$\overline{CE}=V_{IL}$: f=Min, I_{OUT} =0mA	I_{CC_2}			40 / 30	mA
V_{PP} Supply Current	$V_{PP} = V_{CC}\pm0.6V$	I_{PP_1}		1	100	µA
Input High Level		V_{IH}	2.0		V_{CC} +0.3	V
Input Low Level		V_{IL}	-0.1		0.8	V
Output Low Level	I_{OL} =2.1mA	V_{OL}			0.45	V
Output High Level	I_{OH} = -400 µA	V_{OH_1}	2.4			V
Output High Level	I_{OH} = -100 µA	V_{OH_2}	V_{CC}-0.7			V

AC TEST CONDITIONS

Input pulse levels:	0.45V TO 2.4V
Input Rise/Fall Times:	≤20ns
Input Reference Levels:	0.8V TO 2.0V
Output Reference Levels:	0.8V to 2.0V
Output Load:	1 TTL gate and C_L =100pF



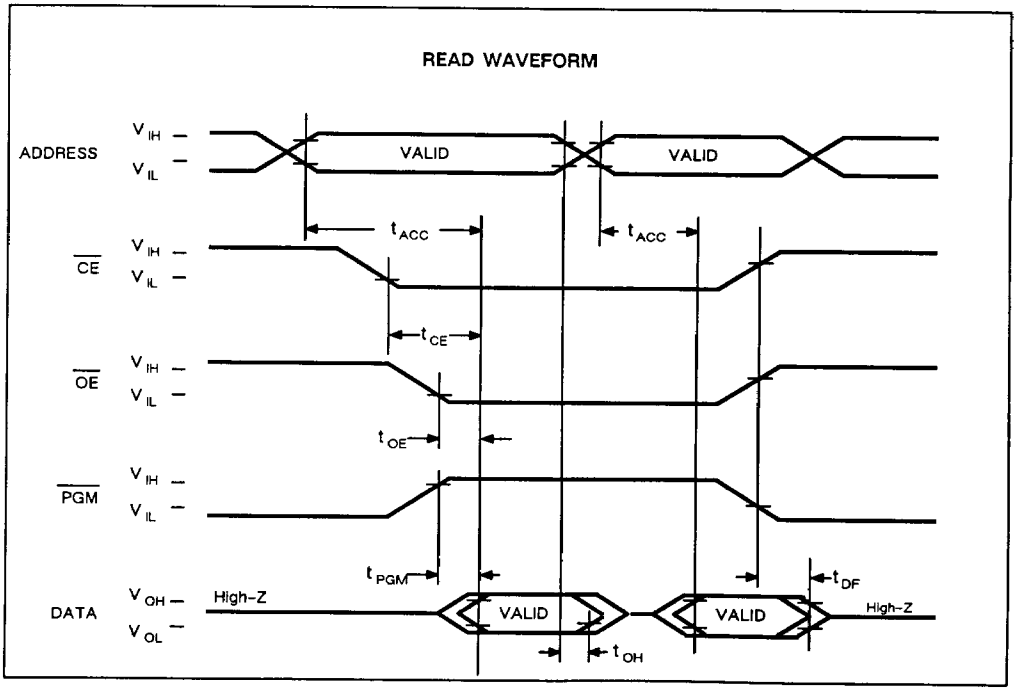
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	MBM27C1024-15 Values		MBM7C1024-20 Values		MBM27C1024-25 Values		Unit
		Min	Max	Min	Max	Min	Max	
Address Access Time	t_{ACC}		150		200		250	ns
$\overline{CE}$ to Output Delay Time	t_{CE}		150		200		250	ns
$\overline{OE}$ to Output Delay Time *1	t_{OE}		70		70		100	ns
$\overline{PGM}$ to Output Delay Time *1	t_{PGM}		70		70		100	ns
$\overline{CE}$, $\overline{OE}$ or $\overline{PGM}$ to Output Float Delay*2	t_{DF}	0	60	0	60	0	60	ns
Address to Output Hold Time	t_{OH}	0		0		0		ns

NOTE: *1: $\overline{OE}$ ($\overline{PGM}$) may be delayed up to tACC-tOE(tPGM) after the falling edge of $\overline{CE}$ without impact on tACC.

*2: tDF is specified from $\overline{CE}$, $\overline{OE}$ or $\overline{PGM}$, whichever occurs first. tDF is defined as the point where data is no longer driven.



PROGRAMMING / ERASING INFORMATION

PROGRAMMING

One-Word Programming. When +12.5V(±0.3V) is applied to V_{PP}, +6V (±0.25V) is applied to V_{CC}, $\overline{CE}$ = VIL, $\overline{PGM}$ and $\overline{OE}$ = VIH, the programming mode is initiated. Next, the proper address is input and the data pattern is applied to the input buffer(Figure 1). When both address and data are stable, a 0.5ms negative pulse is applied to the $\overline{PGM}$. Upon verification of written data read out by $\overline{OE}$ an over pulse (three times the initial pulse width times the number of pulses used to accomplish a write) should be applied to complete the programming of one word. Refer to the PROGRAMMING FLOWCHART that follows for step-by-step programming procedures.

Two-Word Programming. When compared to one-word programming, the two-word programming method reduces the programming time by about 50% one half. Voltages applied to V_{PP} and V_{CC} are the same as those for one-word programming; however, some logic levels differ--refer to "Two Word Programming" in the Truth Table. In conjunction with the $\overline{OE}$ pin, address A0 is used to latch two words of data. When both address and data are stable, a 0.5ms negative pulse is applied to the $\overline{PGM}$. Upon verification of written data read out by $\overline{OE}$ an over pulse (three times the initial pulse width times the number of pulses used to accomplish a write) should be applied to complete the programming of two words. Refer to the PROGRAMMING FLOWCHART that follows for step-by-step programming procedures.

Caution

The width of one programming pulse must not exceed 40ms; thus, a continuous TTL low-level voltage should not be applied to the $\overline{PGM}$ pin. Also, a 0.1µF capacitor must be connected between V_{PP} and ground to prevent excessive voltage transients. Neglecting either of these precautions may cause device failure.

Electronic Signature/Programming Algorithm. When the MBM27C1024 is shipped from the factory, all memory cells (1,048,576 bits) are set to the High state (logic 1). During the programming procedure, affected bit cells are set to the Low state (logic 0).

The MBM27C1024 is programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. Manufacturer and device codes are electronically stored in each device; these codes can be read at the output port (D0 to D15) for the purpose of matching the device with the Quick Pro™ algorithm. The ELECTRONIC SIGNATURE CODE LIST is shown preceding the ELECTRICAL CHARACTERISTICS.

ERASING

In order to clear all memory cells of programmed contents, the MBM27C1024 must be exposed to an ultraviolet light source. To completely erase the memory (restore all cells to a logic 1 state), a dosage of 15Wsec/cm^2 is required. The required exposure can be obtained by using a UV-lamp with a wavelength of 253.7nm with an intensity of 12mW/cm^2. Remove all filters from the lamp and clean the transparent lid of the MBM27C1024 with a non-abrasive cleaner. Hold the MBM27C1024 approximately one inch from the light source for 15-to-21 minutes. (Note. The MBM27C1024 and other similar devices can be erased by light sources with longer wavelengths: however, the erasing time is much greater. Nonetheless, exposure to fluorescents or sunlight will severely degrade and eventually erase the memory. When used in a lighted environment, it is recommended that the transparent window be covered with an opaque label.)

ELECTRONIC SIGNATURE CODE LIST

Definition	A0	A1 TO A5	A6 to A15	O0	O1	O2	O3	O4	O5	O6	O7	D8 to D15	HEX
Manufacture	VIL	VIL	Don't Care	0	0	1	0	0	0	0	0	0	#04
Device	VIH	VIL	Don't Care	0	0	1	0	0	1	1	0	0	#64

Note: A9=12V±0.5V

DC CHARACTERISTICS *(DURING PROGRAMMING)*

(T_A= 25 °C ± 5°C, V_{CC}*1 = 6V ± 0.25V, V_{PP}*2 = 12.5V ± 0.3V)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Input High Level	V_{IH}	2.0		V_{CC}+0.3	V
Input Low Level	V_{IL}	-0.1		0.8	V
Input Load Current	I_{LI}	-10		10	μA
V_{CC} Supply Current	I_{CC}			30	mA
V_{PP} Supply Current ($\overline{CE}$=$\overline{PGM}$=V_{IL} ; $\overline{OE}$=V_{IH})	I_{PP21}			50	mA
V_{PP} Supply Current ($\overline{CE}$=V_{IH} ; $\overline{OE}$=$\overline{PGM}$=V_{IL})	I_{PP22}			100	mA
V_{PP} Supply Current ($\overline{PGM}$=V_{IH})	I_{PP3}			5	mA
Output Low Level (IOL=2.1mA)	V_{OL}			0.45	V
Output High Level (IOH=-400 μA)	V_{OH}	2.4			V

NOTE *1 V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.

*2 V_{PP} must not be greater than 13V including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 12.5 volts. Also, during $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from V_{CC} to V_{PP} volts or vice versa.

AC CHARACTERISTICS *(AT ONE WORD PROGRAMMING)*

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
V_{PP} Setup Time	t_{VPS}	2			μS
Address Setup Time	t_{AS}	2			μS
Data Setup Time	t_{DS}	2			μS
$\overline{CE}$ Setup Time	t_{CES}	2			μS
$\overline{OE}$ Setup time	t_{OES}	2			μS
Address Hold Time	t_{AH}	0			μS
Data Hold Time	t_{DH}	2			μS
$\overline{OE}$ to Output Valid	t_{OEV}			500	ns
$\overline{OE}$ to Output Float	t_{DFV}			150	ns
Programming Pulse Width	t_{PW}	0.475	0.50	0.525	ms
Programming Pulse Number	N	1		25	times
Over Programming Pulse Width	t_{OPW}	1.4	1.5*	39.4	ms

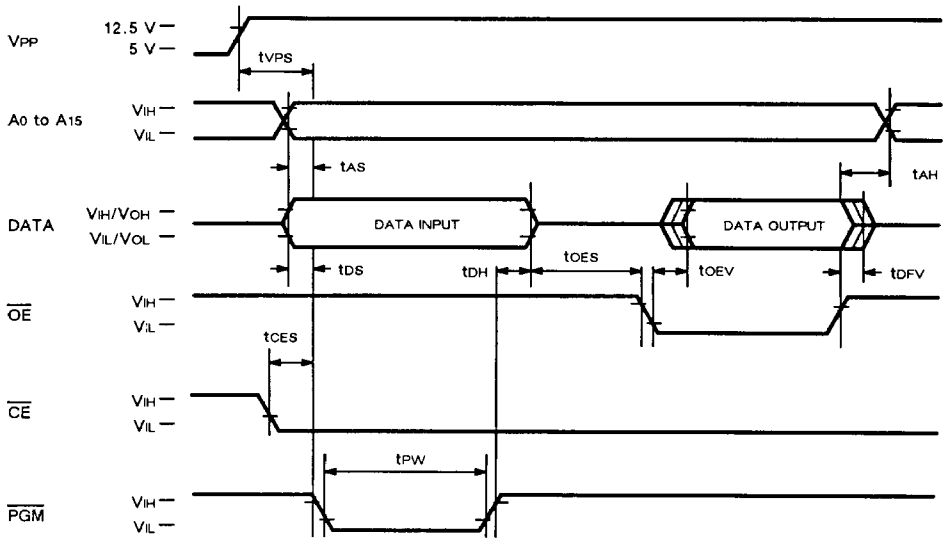
NOTE: t_{OPW} = 1.5 x Nms ± 5%

AC CHARACTERISTICS *(AT TWO WORD PROGRAMMING)*

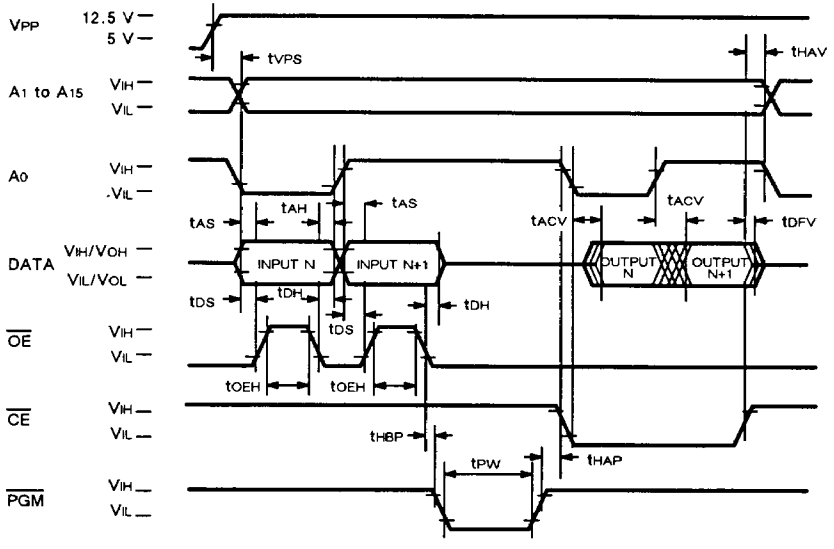
Parameter	Symbol	Values			Unit
		Min	Typ	Max	
V_{PP} Setup Time	t_{VPS}	2			μS
Address Setup Time	t_{AS}	2			μS
Data Setup Time	t_{DS}	2			μS
Address Hold Time	t_{AH}	2			μS
Data Hold Time	t_{DH}	2			μS
$\overline{OE}$ High Hold Time	t_{OEH}	2			μS
Hold Time Before Programming	t_{HBP}	2			μS
Hold Time After Program	t_{HAP}	2			μS
Hold Time After Verify	t_{HAV}	0			μS
Address Access Time at Verify	t_{ACV}			500	ns
$\overline{CE}$ to Output Float at Verify	t_{DFV}			150	ns
Programming Pulse Width	t_{PW}	0.475	0.50	0.525	ms
Programming Pulse Number	N	1		25	times
Over Programming Pulse Width (Note)	t_{OPW}	1.4	1.5*	39.4	ms

NOTE: $t_{OPW} = 1.5 \times Nms \pm 5\%$

ONE-WORD PROGRAMMING WAVEFORM



TWO-WORD PROGRAMMING WAVEFORM



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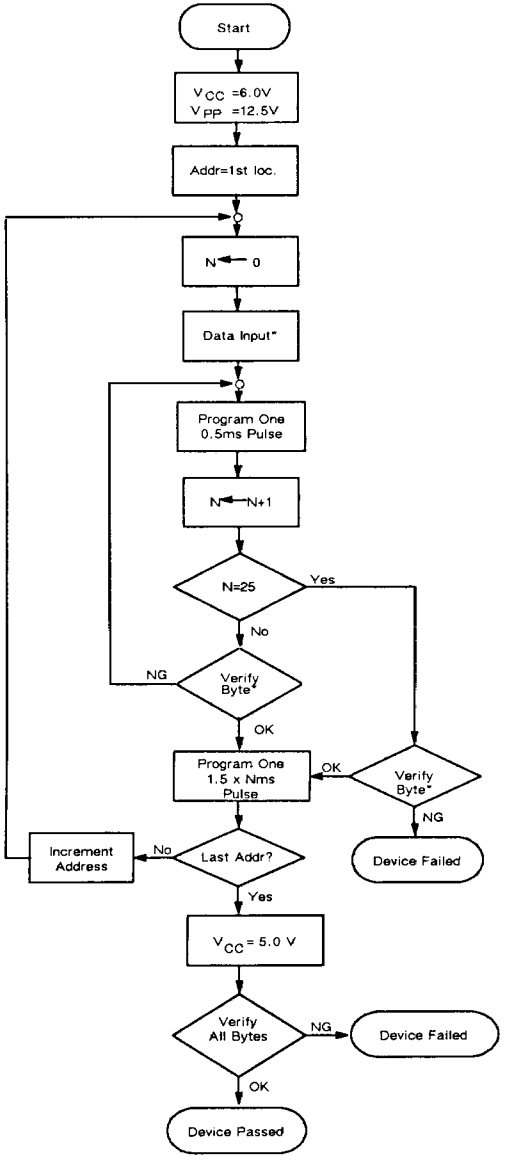
PROGRAMMING FLOWCHART

V_{CC} =6V ±0.25V
V_{PP} =12.5 ± 0.3V
t_{PW} =0.5ms ± 5%
t_{OPW} =1.5 x Nms ±5%



*: 1 word or 2 words

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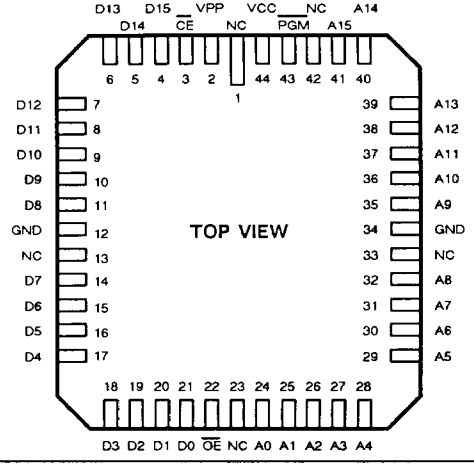
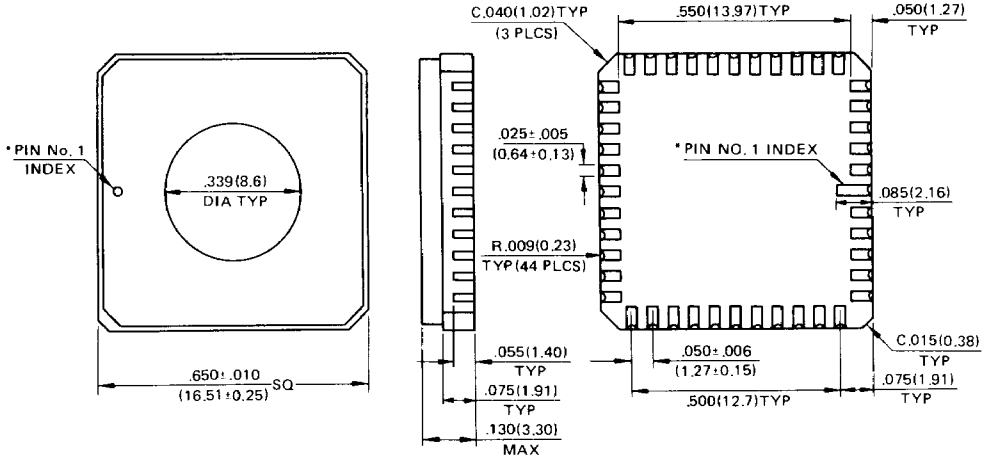
PACKAGE DIMENSIONS



44-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIR
(CASE No.: LCC-44C-F01)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

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Dimension in
inches (millimeters)

Dimensions in
Inches (millimeters)

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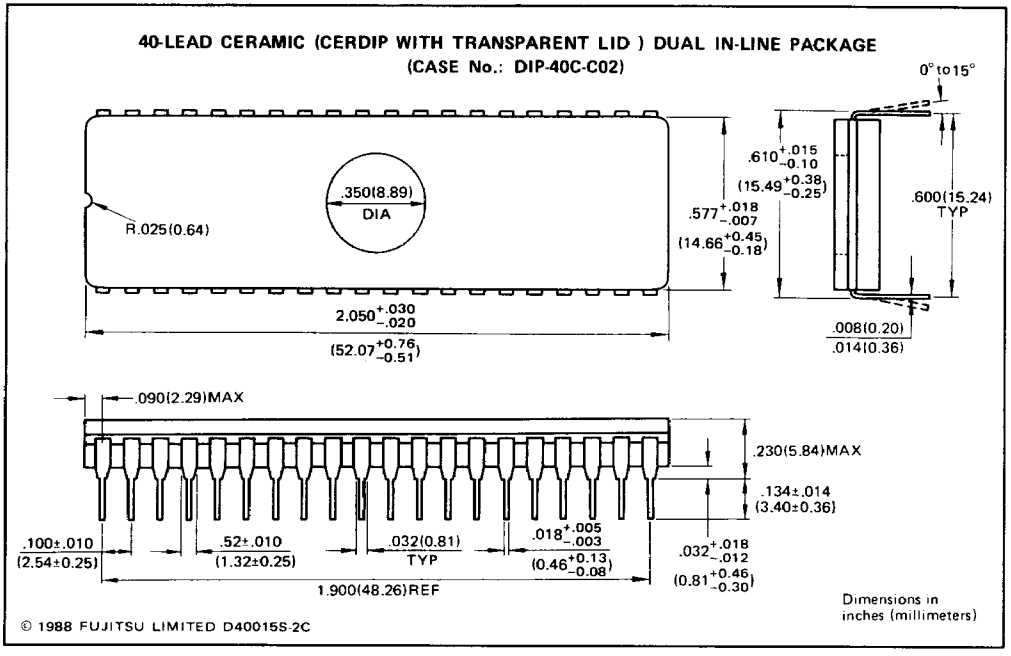
PACKAGE DIMENSIONS