Integrated Device Technology, Inc.

BiCMOS StaticRAM 240K (16K x 15-BIT) CACHE-TAG RAM For PowerPC™ and RISC Processors

IDT71216

FEATURES:

- 16K x 15 Configuration
  - 12 TAG Bits
  - 3 Separate I/O Status Bits (Valid, Dirty, Write Through)
- Match output uses Valid bit to qualify MATCH output
- High-Speed Address-to-Match comparison times
  - 8/9/10/12ns over commercial temperature range
- $\overline{TA}$ circuitry included inside the Cache-Tag for highest speed operation
- Asynchronous Read/Match operation with Synchronous Write and Reset operation
- Separate $\overline{WE}$ for the TAG bits and the Status bits
- Separate $\overline{OE}$ for the TAG bits, the Status bits, and $\overline{TA}$
- Synchronous $\overline{RESET}$ pin for invalidation of all Tag entries
- Dual Chip selects for easy depth expansion with no performance degredation
- I/O pins both 5V TTL and 3.3V LVTTL compatible with V_{CCQ} pins
- $\overline{PWRDN}$ pin to place device in low-power mode
- Packaged in a 80-pin Thin Plastic Quad Flat Pack (TQFP)

DESCRIPTION:

The IDT71216 is a 245,760-bit Cache Tag StaticRAM, organized 16K x 15 and designed to support PowerPC and other RISC processors at bus speeds up to 66MHz. There are twelve common I/O TAG bits, with the remaining three bits used as status bits. A 12-bit comparator is on-chip to allow fast comparison of the twelve stored TAG bits and the current Tag input data. An active HIGH MATCH output is generated when these two groups of data are the same for a given address. This high-speed MATCH signal, with t_{ADM} as fast as 8ns, provides the fastest possible enabling of secondary cache accesses.

The three separate I/O status bits (VLD, DTY, and WT) can be configured for either dedicated or generic functionality, depending on the SFUNC input pin. With SFUNC LOW, the status bits are defined and used internally by the device, allowing easier determination of the validity and use of the given Tag data. SFUNC HIGH releases the defined internal status bit usage and control, allowing the user to configure the status bit information to fit his system needs. A synchronous $\overline{RESET}$ pin, when held LOW at a rising clock edge, will reset all status bits in the array for easy invalidation of all Tag addresses.

The IDT71216 also provides the option for Transfer Acknowledge ($\overline{TA}$) generation within the cache tag itself, based upon MATCH, VLD bit, WT bit, and external inputs provided by the user. This can significantly simplify cache controller logic and minimize cache decision time. Match and Read operations are both asynchronous in order to provide the fastest access times possible, while Write operations are synchronous for ease of system timing.

The IDT71216 uses a 5V power supply on Vcc, with separate V_{CCQ} pins provided for the outputs to offer compliance with both 5.0V TTL and 3.3V LVTTL Logic levels. The $\overline{PWRDN}$ pin offers a low-power standby mode to reduce power consumption by 90%, providing significant system power savings.

The IDT71216 is fabricated using IDT's high-performance, high-reliability BiCMOS technology and is offered in a space-saving 80-pin Thin Plastic Quad Flat Pack (TQFP) package.

PIN DESCRIPTIONS

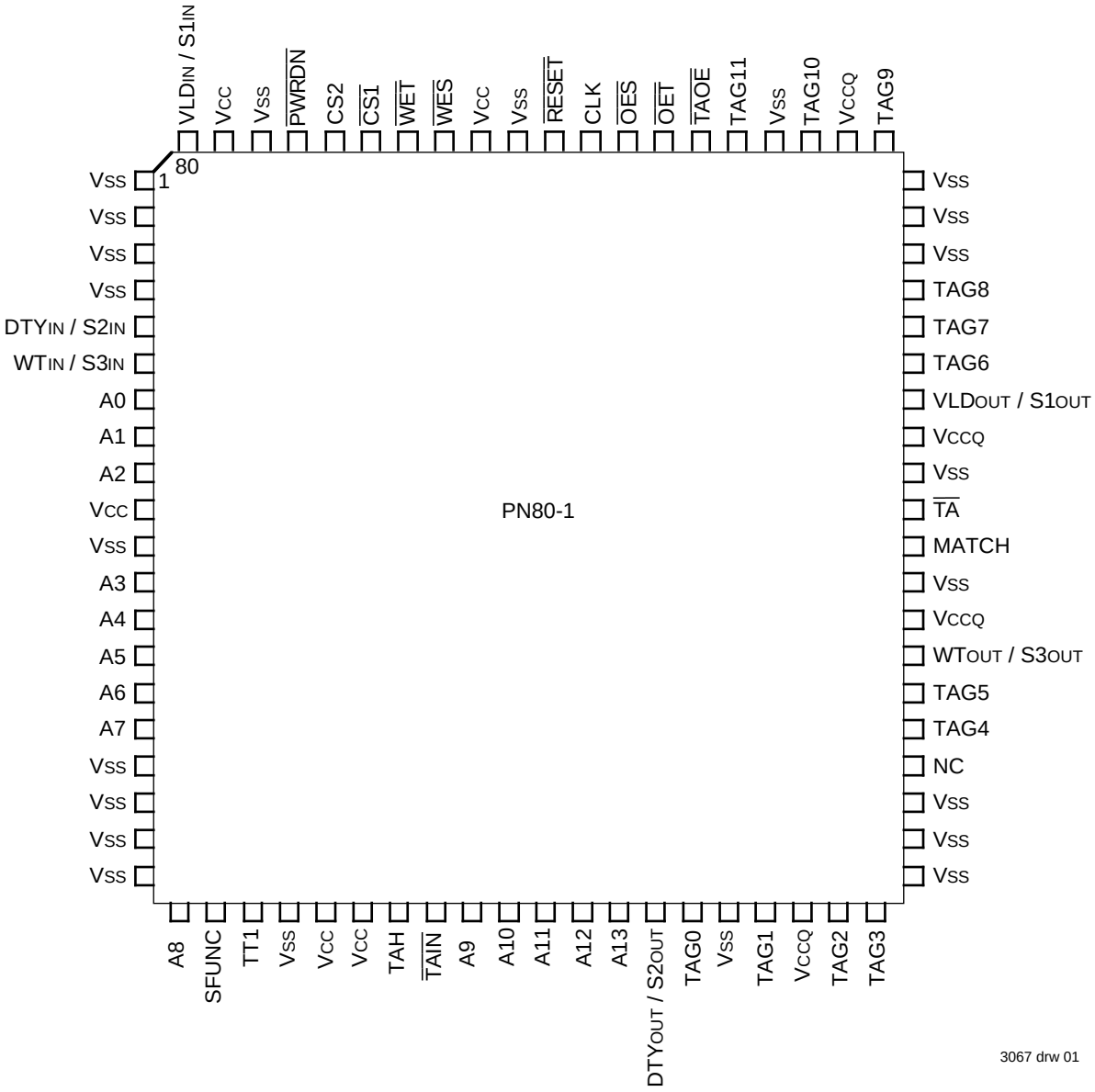
$A_0 – A_{13}$	Address Inputs	Input
$\overline{CS1}$, CS2	Chip Selects	Input
$\overline{WET}$	Write Enable - Tag Bits	Input
$\overline{WES}$	Write Enable - Status Bits	Input
$\overline{OET}$	Output Enable - Tag Bits	Input
$\overline{OES}$	Output Enable - Status Bits	Input
$\overline{RESET}$	Status Bit Reset	Input
$\overline{PWRDN}$	Powerdown Mode Control Pin	Input
SFUNC	Status Bit Function Control Pin	Input
TT1	Read/Write Input from Processor	Input
VLD_{IN} / S_{1IN}	Valid Bit / S_1 Bit Input	Input
DTY_{IN} / S_{2IN}	Dirty Bit / S_2 Bit Input	Input
WT_{IN} / S_{3IN}	Write Through Bit / S_3 Bit Input	Input

CLK	System Clock	Input
TAH	$\overline{TA}$ Force High	Input
$\overline{TAOE}$	$\overline{TA}$ Output Enable	Input
$\overline{TAIN}$	Additional $\overline{TA}$ Input	Input
$\overline{TA}$	Transfer Acknowledge	Output
$TAG_0 – TAG_{11}$	Tag Data Input/Outputs	I/O
VLD_{OUT} / S_{1OUT}	Valid Bit / S_1 Bit Output	Output
DTY_{OUT} / S_{2OUT}	Dirty Bit / S_2 Bit Output	Output
WT_{OUT} / S_{3OUT}	Write Through Bit / S_3 Bit Output	Output
MATCH	Match	Output
V_{CC}	+5V Power	Pwr
V_{CCQ}	Output Buffer Power	QPwr
V_{SS}	Ground	Gnd

3067 tbl 01

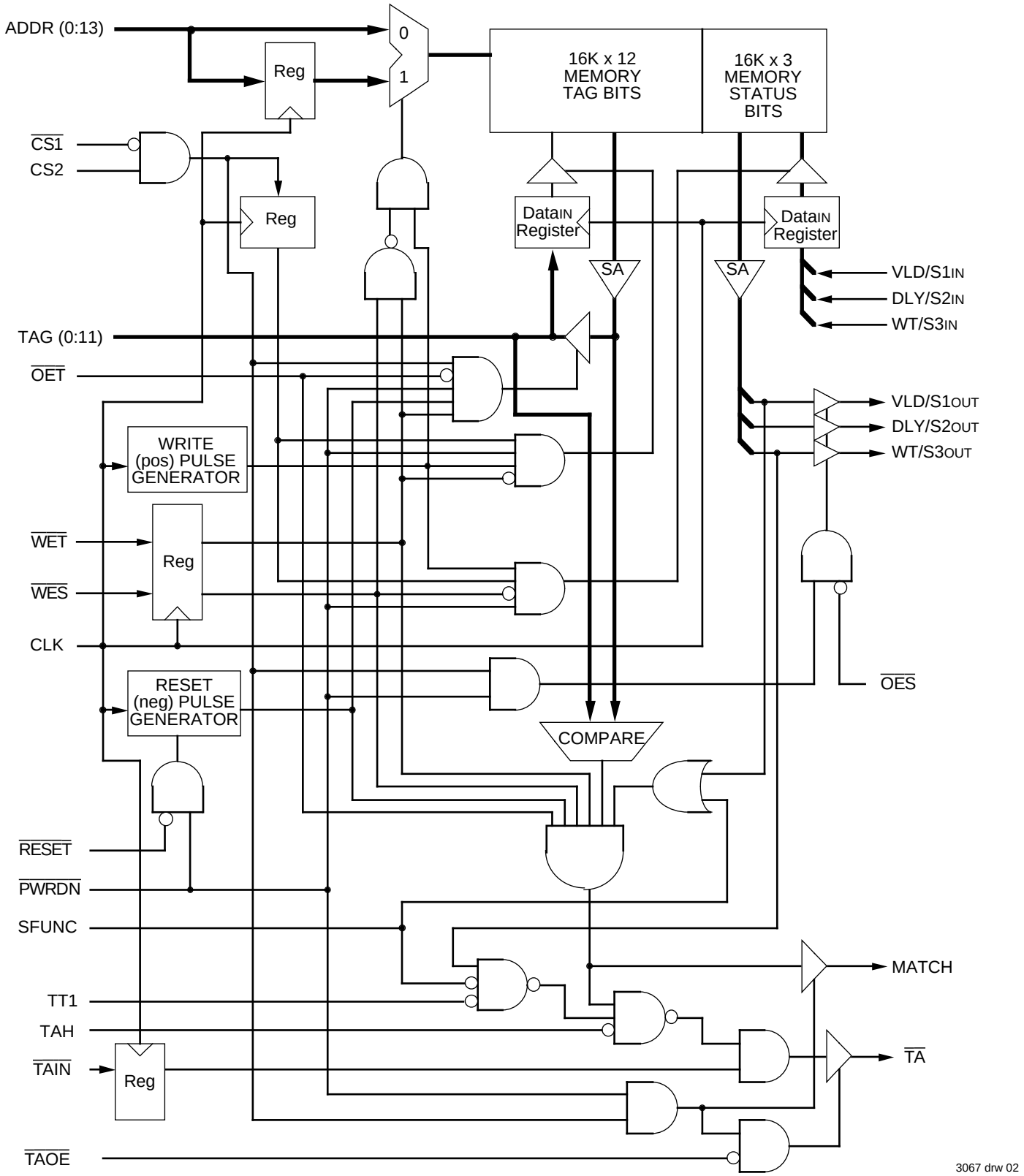
The IDT logo is a registered trademark and CacheRAM is a trademark of Integrated Device Technology, Inc.
PowerPC is a trademark of International Business Machines, Inc.

PIN CONFIGURATION



TQFP
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLES

CHIP SELECT, RESET, AND POWER-DOWN FUNCTIONS(1, 2)

$\overline{CS1}$	CS2	$\overline{RESET}$	$\overline{PWRDN}$	CLK	$\overline{WET}$	$\overline{WES}$	$\overline{TAOE}$		TAG	VLD_{OUT}	DTY_{OUT}	WT_{OUT}	MATCH	$\overline{TA}$	OPERATION	POWER
CHIP SELECT FUNCTION																
H	X	X	H	X	X	X	X		Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Deselected	Active
X	L	X	H	X	X	X	X		Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Deselected	Active
L	H	X	H	X	X	X	X		–	–	–	–	–	–	Selected	Active
RESET FUNCTION																
L	H	L	H	↑	H	H	L		Hi-Z	L(3)	L(3)	L(3)	L(3)	H	Reset Status	Active
L	H	L	H	↑	H	H	H		Hi-Z	L(3)	L(3)	L(3)	L(3)	Hi-Z	Reset Status	Active
H	X	L	H	↑	H	H	X		Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Reset Status	Active
X	L	L	H	↑	H	H	X		Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Reset Status	Active
X	X	L	H	↑	L	X	X		–	–	–	–	–	–	Not Allowed	–
X	X	L	H	↑	X	L	X		–	–	–	–	–	–	Not Allowed	–
POWER-DOWN FUNCTION																
X	X	X	L	X	H	H	X		Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Power-down	Standby

NOTES: 3067 tbl 02

1. "H" = V_{IH}, "L" = V_{IL}, "X" = don't care, "–" = unrelated.
2. $\overline{OET}$, $\overline{OES}$, TT1, TAH, $\overline{TAIN}$ and SFUNC are "X" for this table.
3. $\overline{OES}$ is LOW.

READ AND WRITE FUNCTIONS(1, 2)

$\overline{OET}$	$\overline{OES}$	$\overline{WET}$	$\overline{WES}$	CLK	TT1		TAG	VLD_{IN}	DTY_{IN}	WT_{IN}	VLD_{OUT}	DTY_{OUT}	WT_{OUT}	MATCH	OPERATION
READ FUNCTION															
L	X	H	X	X	X		D_{OUT}	–	–	–	–	–	–	D_{OUT}	Read TAG I/O
X	L	X	X	X	X		–	–	–	–	D_{OUT}	D_{OUT}	D_{OUT}	D_{OUT}	Read Status Bits
H	X	X	X	X	X		Hi-Z	–	–	–	–	–	–	D_{OUT}	TAG I/O Disable
X	H	X	X	X	X		–	–	–	–	Hi-Z	Hi-Z	Hi-Z	D_{OUT}	Status Disabled
WRITE FUNCTION															
H	X	L	X	↑	X		D_{IN}	–	–	–	D_{OUT}	D_{OUT}	D_{OUT}	L	Write TAG I/O
L	X	L	X	↑	X		–	–	–	–	–	–	–	–	Not Allowed
X	L	X	L	↑	X		–	D_{IN}	D_{IN}	D_{IN}	D_{OUT}(3)	D_{OUT}(3)	D_{OUT}(3)	L	Write Status Bits
X	H	X	L	↑	X		–	D_{IN}	D_{IN}	D_{IN}	Hi-Z	Hi-Z	Hi-Z	L	Write Status Bits

NOTES: 3067 tbl 03

1. "H" = V_{IH}, "L" = V_{IL}, "X" = don't care, "–" = unrelated.
2. This table applies when $\overline{CS1}$ is LOW and CS2, $\overline{RESET}$, and $\overline{PWRDN}$ are HIGH. $\overline{TAOE}$, TAH, $\overline{TAIN}$ and SFUNC are "X" for this table.
3. D_{OUT} in this case is the same as DIN; that is, the input data is written through to the outputs during the write operation.

TRUTH TABLES (CONT.)

MATCH FUNCTION(1, 2, 3)

$\overline{CS1}$	CS2	SFUNC	$\overline{OET}$	$\overline{WET}$	$\overline{WES}$	TAG	VLD(4)	DTY(4)	WT(4)	MATCH	OPERATION
H	X	X	X	X	X	Hi-Z	–	–	–	Hi-Z	Deselected
X	L	X	X	X	X	Hi-Z	–	–	–	Hi-Z	Deselected
L	H	X	X	X	X	–	–	–	–	DOUT	Selected
L	H	X	L	H	X	DOUT	–	–	–	L	Read Tag I/O
L	H	X	H	L	X	DIN	–	–	–	L	Write Tag I/O
L	H	X	X	X	L	–	DIN	DIN	DIN	L	Write Status Bits
L	H	L	H	H	H	TAGIN	L	–	–	L	Invalid Data - Dedicated Status Bits
L	H	L	H	H	H	TAGIN	H	–	–	M	Match - Dedicated Status Bits
L	H	H	H	H	H	TAGIN	X	–	–	M	Match - Generic Status Bits

NOTES:
3067 tbl 04

1. "H" = V_{IH}, "L" = V_{IL}, "X" = don't care, "–" = unrelated.
2. M = HIGH if TAGIN equals the memory contents at that address; M = LOW if TAGIN does not equal the memory contents at that address.
3. $\overline{PWRDN}$ and $\overline{RESET}$ are HIGH for this table. TT1, TAH, $\overline{TAOE}$, $\overline{TAIN}$, $\overline{OES}$, and CLK are "X".
4. This column represents the stored memory cell data for the given Status bit at the selected address.

$\overline{TA}$ FUNCTION(1, 2, 3, 5)

$\overline{TAOE}$	$\overline{TAIN}$(6)	$\overline{OET}$	$\overline{WET}$	$\overline{WES}$	TAH	TT1	SFUNC	VLD(4)	DTY(4)	WT(4)	TAG	MATCH	$\overline{TA}$	OPERATION
H	X	X	X	X	X	X	X	X	–	X	–	–	Hi-Z	$\overline{TA}$ Disabled
L	L	X	X	X	X	X	X	X	–	X	–	X	L	External $\overline{TA}$ Input (7)
L	H	L	X	X	X	X	X	X	–	X	DOUT	L	H	Read TAG
L	H	X	L	X	X	X	X	X	–	X	DIN	L	H	Write TAG
L	H	X	X	L	X	X	X	DIN	DIN	DIN	–	L	H	Write Status
L	H	X	X	X	H	X	X	X	–	X	–	X	H	Force $\overline{TA}$ HIGH
L	H	X	X	X	X	X	L	L	–	X	–	L	H	Invalid TAG
L	H	X	X	X	X	L	L	X	–	H	–	X	H	Write Through
L	H	H	H	H	L	X	L	H	–	L	TAGIN	M	$\overline{M}$	Compare
L	H	H	H	H	L	H	L	H	–	X	TAGIN	M	$\overline{M}$	Compare
L	H	H	H	H	L	X	L	H	–	X	TAGIN	M	$\overline{M}$	Compare
L	H	H	H	H	L	X	H	X	–	X	TAGIN	M	$\overline{M}$	Compare

NOTES:
3067 tbl 05

1. "H" = V_{IH}, "L" = V_{IL}, "X" = don't care, "–" = unrelated.
2. M = HIGH if TAGIN equals the memory contents at that address; M = LOW if TAGIN does not equal the memory contents at that address.
3. $\overline{PWRDN}$ and $\overline{RESET}$ are HIGH for this table. CLK and $\overline{OES}$ are "X".
4. This column represents the stored memory cell data for the given Status bit at the selected address.
5. $\overline{CS1}$ is LOW, CS2 is HIGH for this table.
6. $\overline{TAIN}$ is a synchronous input; thus the inputs noted in the table must be applied during a rising CLK edge.
7. $\overline{TAIN}$ will be a factor in determining the $\overline{TA}$ output in all cases except when TAH is HIGH and there is a valid MATCH. In that case, $\overline{TA}$ will be LOW(Valid).

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
V_{CCQ}	5V Output Buffers	4.75	5.0	5.25	V
V_{CCQ}	3.3V Output Buffers	3.0	3.3	3.6	V
V_{SS}	Supply Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.0	VCC+0.3	V
V_{IHQ}	I/O High Voltage	2.2	3.0	VCCQ+0.3	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 3067 tbl 06

1. V_{IL} (min.) = –1.5V for pulse width of less than 10ns, once per cycle.

CAPACITANCE

(T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{TAG}	TAG Input/Output Capacitance	$V_{I/O}$ = 0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 3067 tbl 07

1. This parameter is determined by device characterization but is not production tested.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0(2)	V
T_A	Operating Temperature	–0 to +70	°C
T_{BIAS}	Temperature Under Bias	–65 to +135	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.7	W
I_{OUT}	DC Output Current	20	mA

NOTES: 3067 tbl 08

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.
2. V_{IN} should not exceed Vcc+0.5V. All pins should not exceed 7.0V. V_{CCQ} should never exceed V_{CC}, and V_{CC} should never exceed V_{CCQ} + 4.0V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

(V_{CC} = 5.0V ± 5%, V_{CCQ} = 5.0V ± 5% OR 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0V to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS1} \geq V_{IH}$, CS2 ≤ V_{IL}, $\overline{OE} \geq V_{IH}$, V_{CC} = Max. V_{OUT} = 0V to V_{CCQ}, V_{CCQ} = Max.	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

3067 tbl 09

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1, 2) (V_{CC} = 5.0V ± 5%)

Symbol	Parameter	Test Condition	71216S8		71216S9		71216S10		71216S12		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Operating Power Supply Current	$\overline{PWRDN} \geq V_{IH}$ Outputs Open, V_{CC} = Max., f = f_{MAX}(3)	330	—	300	—	290	—	280	—	mA
I_{SB}	Standby Power Supply Current	$\overline{PWRDN} \leq V_{IL}$, $V_{IN} \geq V_{IH}$ or ≤ V_{IL} V_{CC} = Max., f = f_{MAX}(3)	30	—	30	—	30	—	30	—	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{PWRDN} \leq V_{IL}$, $V_{IN} \geq V_{HC}$ or ≤ V_{LC}(4) V_{CC} = Max., f = 0(3)	25	—	25	—	25	—	25	—	mA

NOTES: 3067 tbl 10

1. All values are maximum guaranteed values.
2. $\overline{CS1} \leq V_{IL}$, CS2 ≥ V_{IH}.
3. f_{MAX} =1/t_{CYC} (all address inputs are cycling at f_{MAX}). f = 0 means no address input lines are changing.
4. V_{HC} = V_{CC} - 0.2V, V_{LC} = 0.2V

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, V_{CCQ} = 5.0V ± 5% OR 3.3V ± 0.3V, T_A = 0 to 70°C)

Symbol	Parameter	IDT71216S8		IDT71216S9		IDT71216S10		IDT71216S12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{AAT}	Address Access Time Tag Bits	—	10	—	11	—	12	—	14	ns
t_{ACST}	Chip Select Access Time Tag Bits	—	8	—	9	—	10	—	12	ns
t_{CLZ}(1)	Chip Select to Tag and Status Bits in Low-Z	1	—	1	—	1	—	1	—	ns
t_{CHZ}(1)	Chip Select to Tag and Status Bits in High-Z	1	5	1	6	1	6	1	7	ns
t_{OET}	Output Enable to Tag Bits Valid	—	5	—	6	—	6	—	7	ns
t_{OTLZ}(1)	Output Enable to Tag Bits in Low-Z	0	—	0	—	0	—	0	—	ns
t_{OTHZ}(1)	Output Enable to Tag Bits in High-Z	1	5	1	6	1	6	1	7	ns
t_{TOH}	Tag Bit Hold from Address Change	2	—	2	—	2	—	2	—	ns
t_{OES}	Output Enable to Status Bits Valid	—	5	—	6	—	6	—	7	ns
t_{OSLZ}(1)	Output Enable to Status Bits in Low-Z	0	—	0	—	0	—	0	—	ns
t_{OSHZ}(1)	Output Enable to Status Bits in High-Z	1	5	1	6	1	6	1	7	ns
t_{AAS}	Address Access Time Status Bits	—	8	—	9	—	10	—	12	ns
t_{ACSS}	Chip Select Access Time Status Bits	—	6	—	7	—	8	—	10	ns
t_{SOH}	Status Bit Hold from Address Change	2	—	2	—	2	—	2	—	ns

NOTE:
1. This parameter is guaranteed with the AC Load (Figure 3) by device characterization, but is not production tested.

3067 tbl 11

AC ELECTRICAL CHARACTERISTICS (1)

(V_{CC} = 5.0V ± 5%, V_{CCQ} = 5.0V ± 5% OR 3.3V ± 0.3V, T_A = 0 to 70°C)

Symbol	Parameter	IDT71216S8		IDT71216S9		IDT71216S10		IDT71216S12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Reset and Power Down Cycles										
t_{SR}	$\overline{RESET}$ Set-up Time	4	—	4	—	4	—	4	—	ns
t_{HR}	$\overline{RESET}$ Hold Time	1	—	1	—	1	—	1	—	ns
t_{SRST}	Status Bit Reset Time	—	50	—	60	—	60	—	70	ns
t_{SHRS}	Status Bit Hold from $\overline{RESET}$ LOW	2	—	2	—	2	—	2	—	ns
t_{RSMI}	$\overline{RESET}$ LOW to MATCH and $\overline{TA}$ Invalid	—	9	—	10	—	10	—	12	ns
t_{RSMV}	$\overline{RESET}$ HIGH to MATCH and $\overline{TA}$ Valid	—	110	—	120	—	120	—	130	ns
t_{RSHZ}(2)	$\overline{RESET}$ LOW to TAG High-Z	—	9	—	10	—	10	—	12	ns
t_{RSLZ}(2)	$\overline{RESET}$ HIGH to TAG Low-Z	—	90	—	100	—	100	—	110	ns
t_{PDSR}	$\overline{PWRDN}$ Set-up to $\overline{RESET}$ LOW	30	—	30	—	30	—	30	—	ns
t_{RHPL}	$\overline{RESET}$ HIGH to $\overline{PWDRN}$ LOW	1	—	1	—	1	—	1	—	CLK
t_{RHWL}	$\overline{RESET}$ HIGH to $\overline{WET}$ and $\overline{WES}$ LOW	90	—	95	—	95	—	105	—	ns
t_{PD}(2)	$\overline{PWRDN}$ LOW to Low Power Mode	—	50	—	50	—	50	—	50	ns
t_{PU}(2)	$\overline{PWRDN}$ HIGH to Active Power Mode	0	—	0	—	0	—	0	—	ns
t_{PDHZ}(2)	$\overline{PWRDN}$ LOW to Outputs in High-Z	—	9	—	10	—	10	—	12	ns
t_{PDLZ}(2)	$\overline{PWRDN}$ HIGH to Outputs in Low-Z	0	—	0	—	0	—	0	—	ns
t_{PUV}	$\overline{PWRDN}$ HIGH to Outputs Valid	—	50	—	50	—	50	—	50	ns
t_{WHPL}(2)	$\overline{WET}$ and $\overline{WES}$ HIGH to $\overline{PWRDN}$ LOW	5	—	5	—	5	—	5	—	ns
t_{PUWL}	$\overline{PWRDN}$ HIGH to $\overline{WET}$ and $\overline{WES}$ Active	50	—	50	—	50	—	50	—	ns

NOTES:
1. Power-down mode is intended to be used during extended time periods of device inactivity.
2. This parameter is guaranteed with the AC Load (Figure 3) by device characterization, but is not production tested.

3067 tbl 12

AC ELECTRICAL CHARACTERISTICS (1)

(V_{CC} = 5.0V ± 5%, V_{CCQ} = 5.0V ± 5% OR 3.3V ± 0.3V, T_A = 0 to 70°C)

Symbol	Parameter	IDT71216S8		IDT71216S9		IDT71216S10		IDT71216S12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle and Clock Parameters										
t_{CYC}	Clock Cycle Time	15	—	15	—	15	—	16.6	—	ns
t_{CH}(2, 3)	Clock Pulse HIGH	4.5	—	4.5	—	4.5	—	5	—	ns
t_{CL}(2, 3)	Clock Pulse LOW	4.5	—	4.5	—	4.5	—	5	—	ns
t_S	$\overline{WET}$, $\overline{WES}$, Chip Select, and Input Data Set-up Time	3	—	3	—	3	—	3	—	ns
t_H	$\overline{WET}$, $\overline{WES}$, Chip Select, and Input Data Hold Time	1	—	1	—	1	—	1	—	ns
t_{SA}	Address Set-up Time	3	—	3	—	3	—	3	—	ns
t_{HA}	Address Hold Time	1	—	1	—	1	—	1	—	ns
t_{WMI}	CLK HIGH Write to MATCH and $\overline{TA}$ Invalid	—	6	—	7	—	7	—	8	ns
t_{CKLZ}(3)	CLK HIGH Read to Outputs in Low-Z	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{CTV}(4)	CLK HIGH Read to Tag Bits Valid	—	9	—	10	—	10	—	12	ns
t_{CSV}(4)	CLK HIGH Write to Status Outputs Valid	—	8	—	9	—	9	—	10	ns
t_{CSH}(3)	Status Output Hold from CLK HIGH Write	0	—	0	—	0	—	0	—	ns
t_{WHPL}	$\overline{WET}$ and $\overline{WES}$ HIGH to $\overline{PWRDN}$ LOW	5	—	5	—	5	—	5	—	ns
t_{PUWL}	PWRDN HIGH to WET and WES Active	50	—	50	—	50	—	50	—	ns

NOTES: 3067 tbl 14

1. All Write cycles are synchronous and referenced from rising CLK.
2. This parameter is measured as a HIGH time above 2.0V and a LOW time below 0.8V.
3. This parameter is guaranteed with the AC Load (Figure 3) by device characterization, but is not production tested.
4. Addresses are stable prior to CLK transition HIGH.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, V_{CCQ} = 5.0V ± 5% OR 3.3V ± 0.3V, T_A = 0 to 70°C)

Symbol	Parameter	IDT71216S8		IDT71216S9		IDT71216S10		IDT71216S12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
MATCH and $\overline{TA}$ Cycles										
t_{ADM}	Address to MATCH Valid	—	8	—	9	—	10	—	12	ns
t_{DAM}	Data Input to MATCH Valid	—	8	—	9	—	10	—	12	ns
t_{CSM}	Chip Select to MATCH Valid	—	8	—	9	—	10	—	12	ns
t_{CMLZ}(1)	Chip Select to MATCH in Low-Z	1	—	1	—	1	—	1	—	ns
t_{CMHZ}(1)	Chip Select to MATCH in High-Z	1	5	1	6	1	6	1	7	ns
t_{MHA}	MATCH Valid Hold from Address	2	—	2	—	2	—	2	—	ns
t_{MHD}	MATCH Valid Hold from Data	2	—	2	—	2	—	2	—	ns
t_{BHA}	$\overline{TA}$ Valid Hold from Address	2	—	2	—	2	—	2	—	ns
t_{BHD}	$\overline{TA}$ Valid Hold from Data	2	—	2	—	2	—	2	—	ns
t_{ADB}	Address to $\overline{TA}$ Valid	—	9	—	10	—	11	—	13	ns
t_{DAB}	Data Input to $\overline{TA}$ Valid	—	9	—	10	—	11	—	13	ns
t_{CSB}	Chip Select LOW to $\overline{TA}$ Valid	—	9	—	10	—	11	—	13	ns
t_{OEBV}	$\overline{TAOE}$ LOW to $\overline{TA}$ Valid	—	6	—	6	—	7	—	8	ns
t_{OBLZ}(1)	$\overline{TAOE}$ LOW to $\overline{TA}$ in Low-Z	0	—	0	—	0	—	0	—	ns
t_{OBHZ}(1)	$\overline{TAOE}$ HIGH to $\overline{TA}$ in High-Z	1	5	1	6	1	6	1	7	ns
t_{BYFH}	TAH HIGH to Force $\overline{TA}$ HIGH	—	5	—	5	—	5	—	6	ns
t_{BYHV}	TAH LOW to $\overline{TA}$ Valid	—	5	—	5	—	5	—	6	ns
t_{SB}	$\overline{TAIN}$ Set-up Time	4	—	4	—	4	—	4	—	ns
t_{HB}	$\overline{TAIN}$ Hold Time	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{BIBL}	CLK HIGH $\overline{TAIN}$ LOW to $\overline{TA}$ LOW	—	6	—	6	—	7	—	8	ns
t_{BIBV}	CLK HIGH $\overline{TAIN}$ HIGH to $\overline{TA}$ Valid	—	6	—	6	—	7	—	8	ns
t_{OEMI}	$\overline{OET}$ LOW to MATCH and $\overline{TA}$ Invalid	—	6	—	7	—	7	—	8	ns
t_{OEMV}	$\overline{OET}$ HIGH to MATCH and $\overline{TA}$ Valid	—	7	—	8	—	8	—	10	ns
t_{WRBH}(2)	W/$\overline{R}$ HIGH to $\overline{TA}$ HIGH	—	6	—	7	—	7	—	8	ns
t_{WRBV}(2)	W/$\overline{R}$ LOW to $\overline{TA}$ Valid	—	6	—	7	—	7	—	8	ns
t_{WMI}	CLK HIGH Write to MATCH and $\overline{TA}$ Invalid	—	7	—	7	—	7	—	8	ns
t_{WMV}(3)	CLK HIGH Read to MATCH and $\overline{TA}$ Valid	—	8	—	9	—	10	—	12	ns

NOTES:

3067 tbl 15

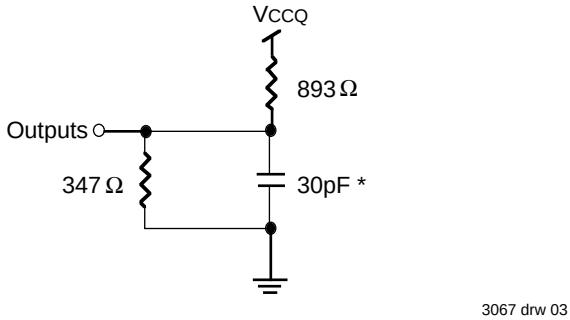
1. This parameter is guaranteed with the AC Load (Figure 3) by device characterization, but is not production tested.
2. These parameters only apply when SFUNC is LOW and the internal WT bit is HIGH.
3. t_{ADM}, t_{DAM}, t_{CSM} and t_{ADB}, t_{DAB}, t_{CSB} must also be satisfied.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
AC Test Load	See Figs. 1, 2, 3, & 4

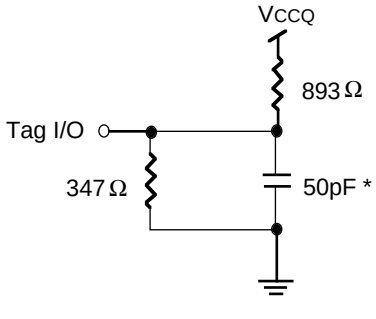
3067 tbl 16

AC TEST LOADS



3067 drw 03

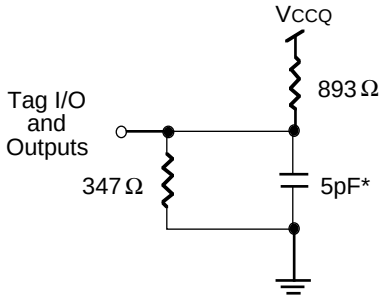
Figure 1. AC Test Load



3067 drw 04

Figure 2. Tag I/O AC Test Load

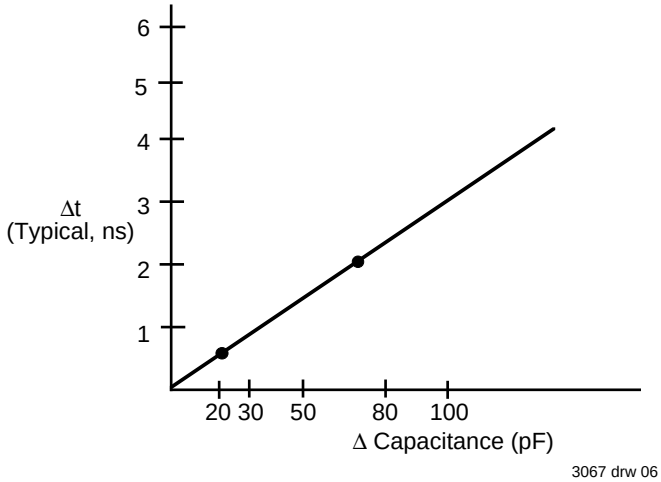
*** Including scope and jig capacitance**



3067 drw 05

Figure 3. AC Test Load
(for t_{HZ} and t_{LZ} parameters)

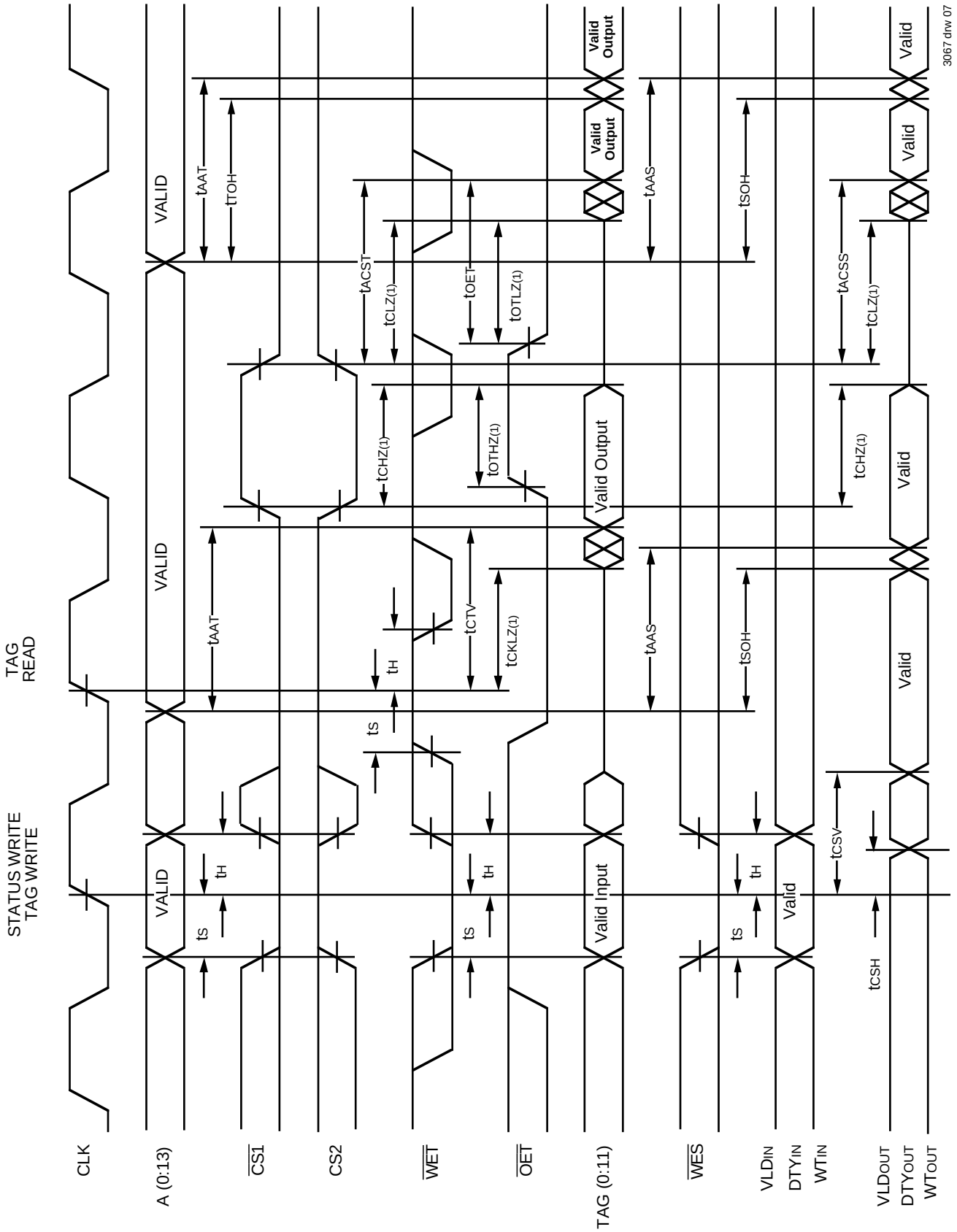
*** Including scope and jig capacitance**



3067 drw 06

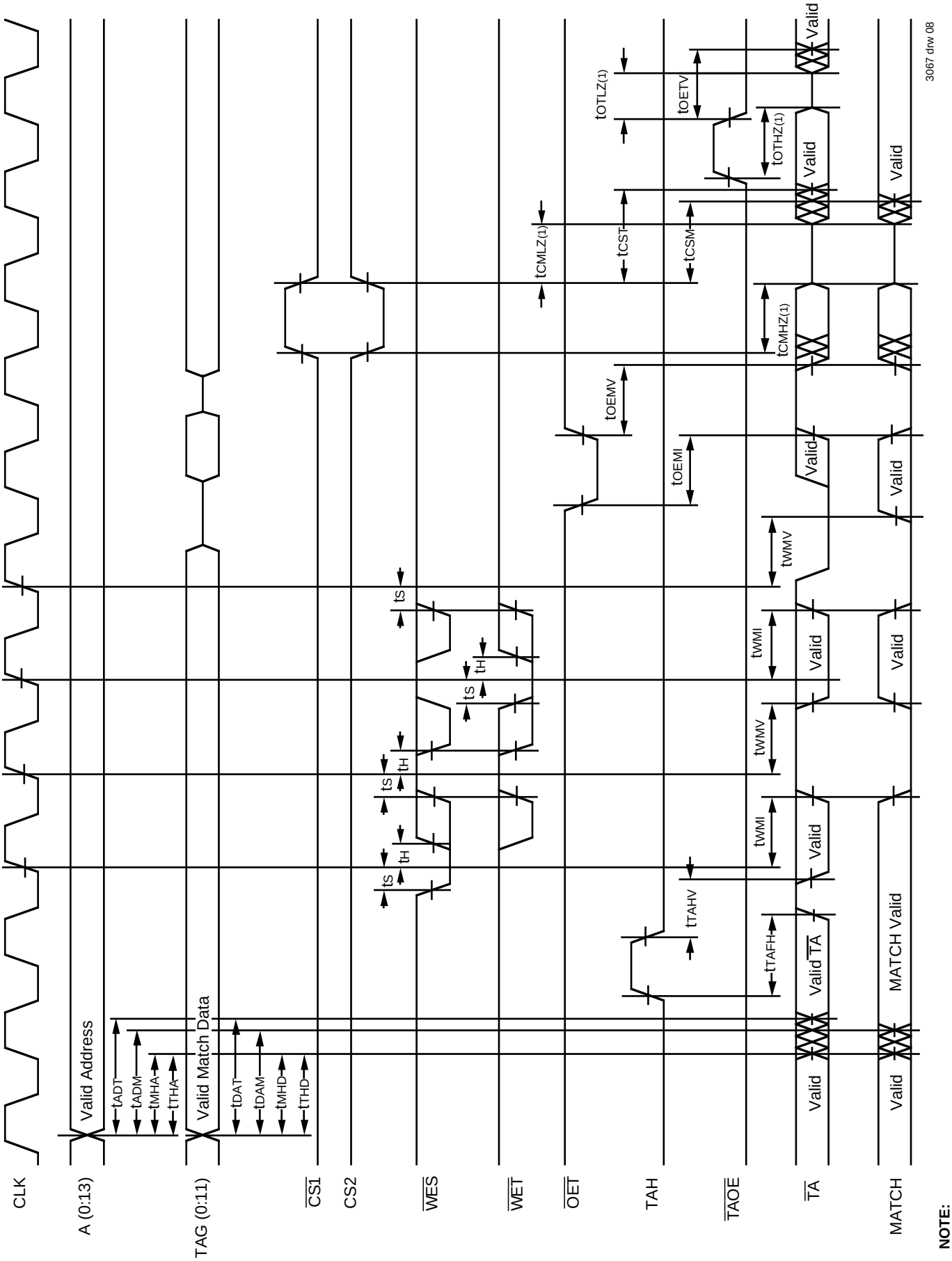
Figure 4. Lumped Capacitance Load, Typical Derating

TIMING WAVEFORMS OF WRITE AND READ CYCLES



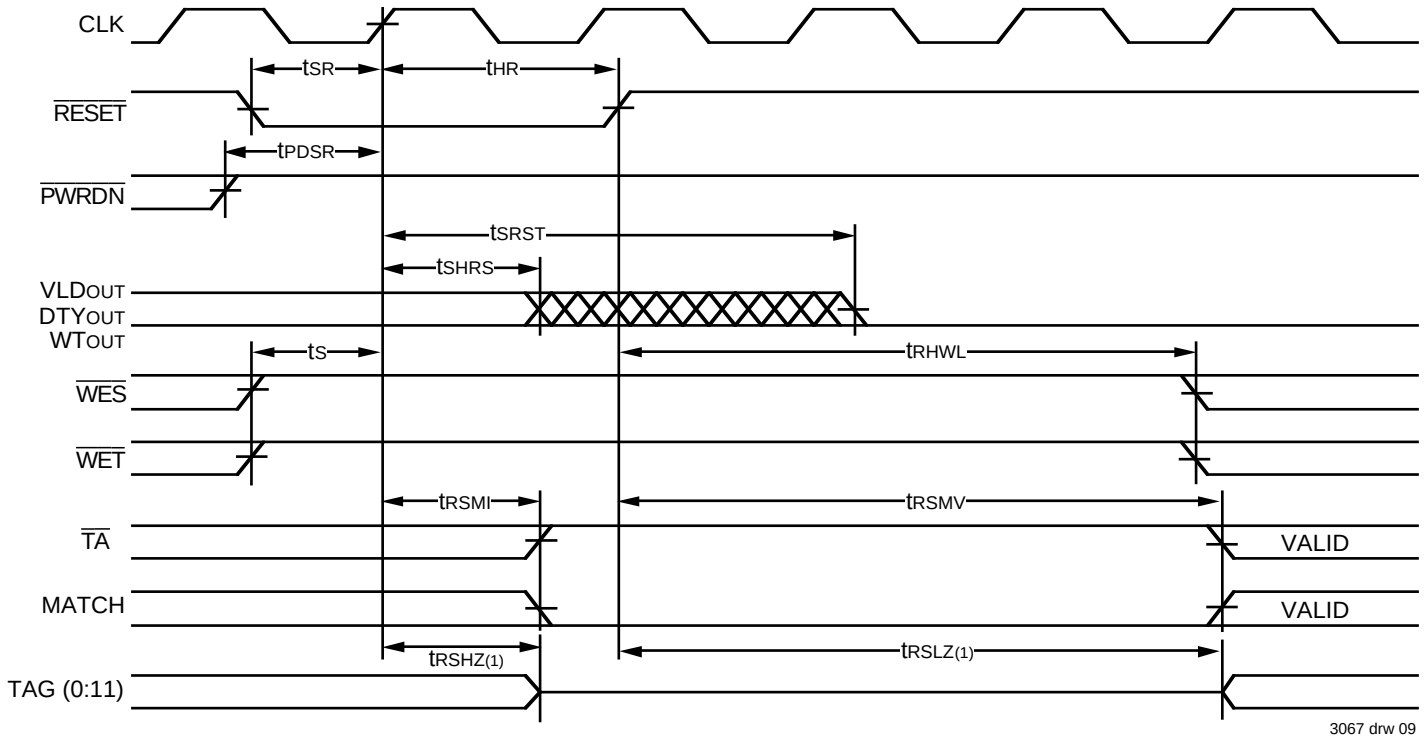
NOTE:
1. Transition is measured ±200mV from steady state.

TIMING WAVEFORMS OF MATCH AND $\overline{TA}$ FUNCTIONS



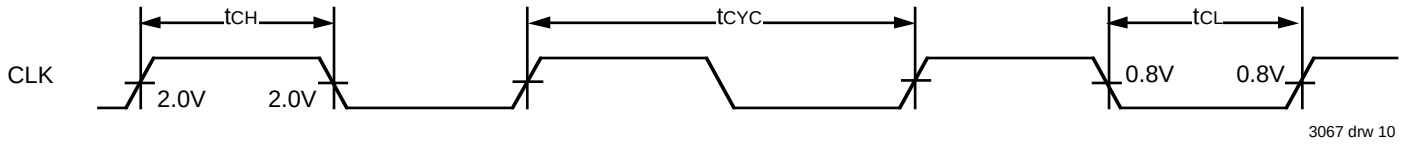
NOTE:
1. Transition is measured ±200mV from steady state.

TIMING WAVEFORMS OF $\overline{\text{RESET}}$ FUNCTION



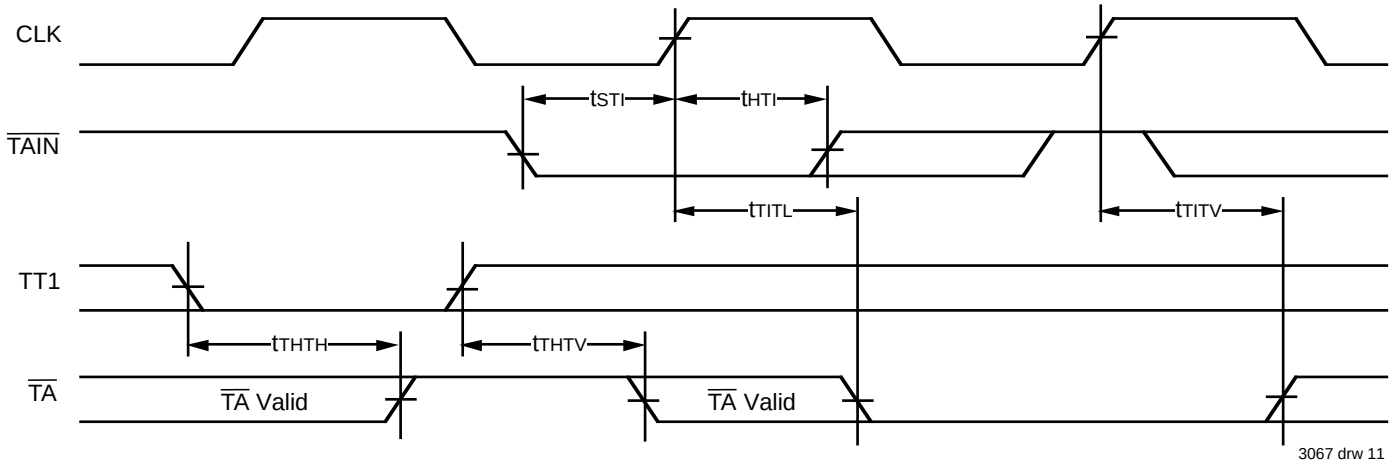
NOTE:
1. Transition is measured ±200mV from steady state.

CLOCK TIMING WAVEFORM

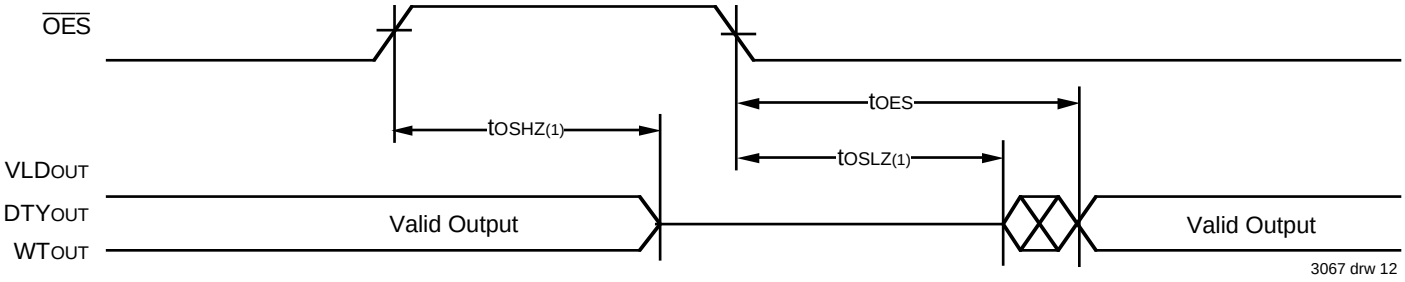


TIMING WAVEFORMS OF $\overline{\text{TA}}$ AND TT1 SIGNAL

Applies when SFUNC is LOW, and the internal WT bit is HIGH

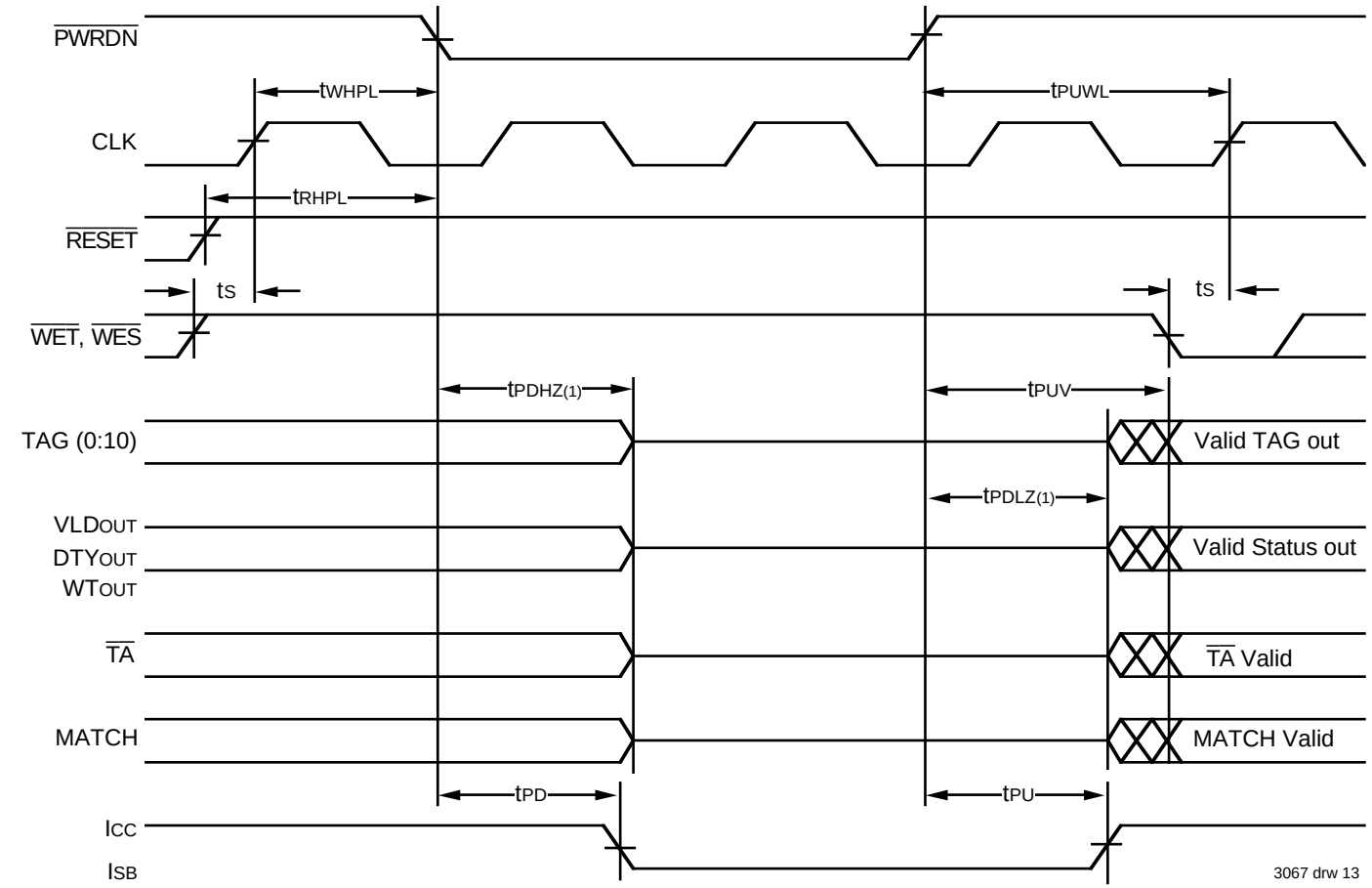


TIMING WAVEFORMS OF $\overline{OES}$ FUNCTION



NOTE:
1. Transition is measured ±200mV from steady state.

TIMING WAVEFORMS OF POWER DOWN FUNCTION



NOTE:
1. Transition is measured ±200mV from steady state.

ORDERING INFORMATION