Integrated Device Technology, Inc.

CMOS STATIC RAMs 64K (16K x 4-BIT)

Separate Data Inputs and Outputs

IDT71981S/L
IDT71982S/L

FEATURES:

- Separate data inputs and outputs
- IDT71981S/L: outputs track inputs during write mode
- IDT71982S/L: high impedance outputs during write mode
- High speed (equal access and cycle time)
  - — Military: 20/25/35/45/55/70/85ns (max.)
  - — Commercial: 15/20/25/35ns (max.)
- Low power consumption
- Battery backup operation—2V data retention (L version only)
- High-density 28-pin hermetic and plastic DIP, 28-pin leadless chip carrier, and 28-pin SOJ
- Produced with advanced CMOS high-performance technology
- Inputs and outputs directly TTL-compatible
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71981/IDT71982 are 65,536-bit high-speed static RAMs organized as 16K x 4. They are fabricated using IDT's high-performance, high-reliability technology—CMOS.

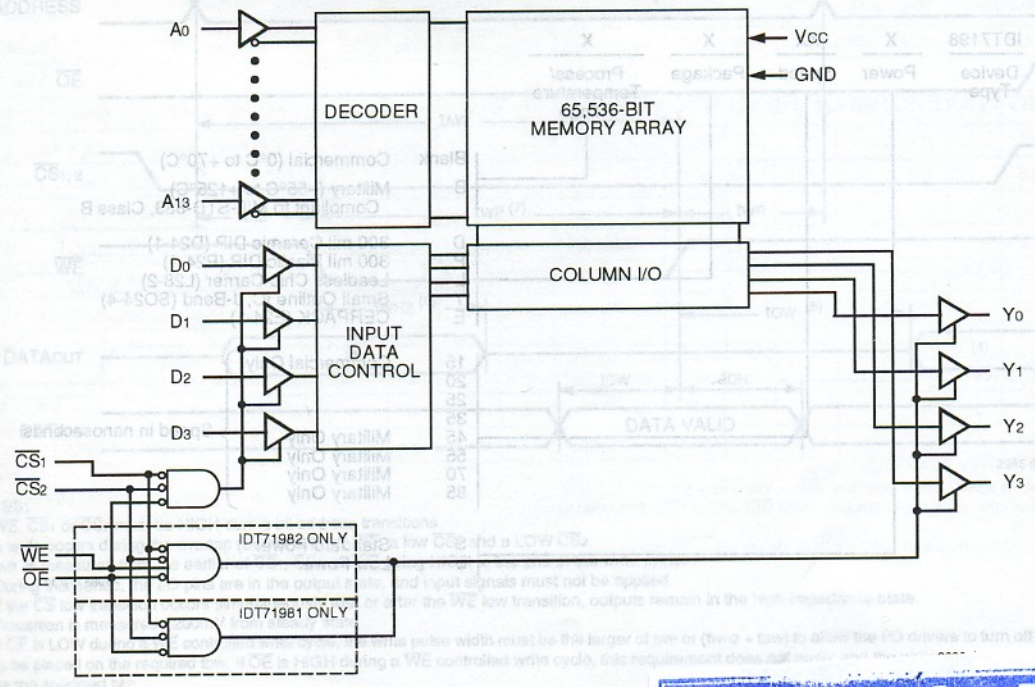
Access times as fast as 15ns are available. These circuits also offer a reduced power standby mode (I_{SB}). When $\overline{CS_1}$ or $\overline{CS_2}$ goes high, the circuit will automatically go to, and remain in, this standby mode. In the ultra-low-power standby mode (I_{SB1}), the devices consume less than 2.5mW, typically. This capability provides significant system-level power and cooling savings. The low-power (L) versions also offer a battery backup data retention capability where the circuit typically consumes only 30µW operating off a 2V battery.

All inputs and outputs of the IDT71981/IDT71982 are TTL-compatible and operate from a single 5V supply.

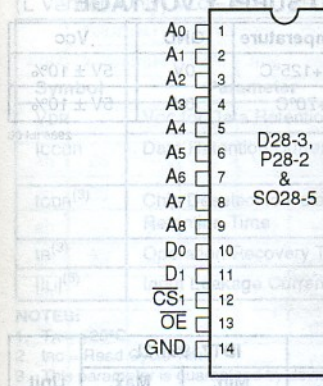
The IDT71981/IDT71982 are packaged in either a 28-pin, 300 mil hermetic DIP, 28-pin 300 mil plastic DIP, 28-pin SOJ,or 28-pin leadless chip carrier.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

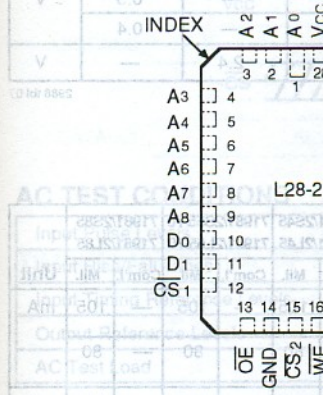
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP/SOJ
TOP VIEW



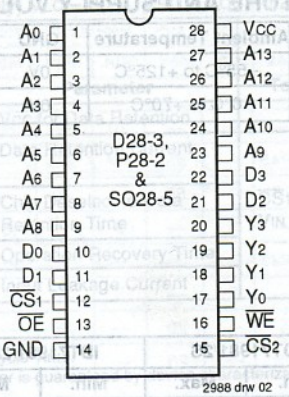
LCC
TOP VIEW

CAPACITANCE (T_A = +25°C,

Symbol	Parameter[1]
C_{IN}	Input Capacitance
C_{OUT}	Output Capacitance

NOTE:
1. This parameter is determined by dev production tested.

PIN CONFIGURATIONS



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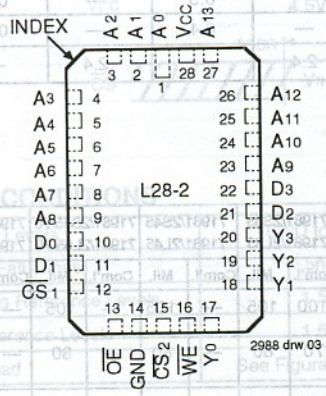
DIP/SOJ
TOP VIEW



2988 drw 03

LCC
TOP VIEW

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

2988 tbl 04

NOTE:
1. This parameter is determined by device characterization, but is not production tested.

PIN DESCRIPTIONS

Name	Description
A0–A13	Address Inputs
$\overline{CS_1}$, $\overline{CS_2}$	Chip Selects
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
D0–D3	$DATA_{IN}$
Y0–Y3	$DATA_{OUT}$
V_{CC}	Power
GND	Ground

2988 tbl 01

TRUTH TABLE[3]

Mode	$\overline{CS_1}$	$\overline{CS_2}$	$\overline{WE}$	$\overline{OE}$	Output	Power
Standby	H	X	X	X	High Z	Standby
Standby	X	H	X	X	High Z	Standby
Read	L	L	H	L	D_{OUT}	Active
Write[1]	L	L	L	L	D_{IN}	Active
Write[1]	L	L	L	H	High Z	Active
Write[2]	L	L	L	X	High Z	Active
Read	L	L	H	H	High Z	Active

2988 tbl 02

NOTES:
1. For IDT71981 only.
2. For IDT71982 only.
3. H = V_{IH}, L = V_{IL}, X = don't care.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

2988 tbl 03

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

2988 tbl 05

NOTE:
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns, once per cycle.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

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DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT71981/2S Min.	IDT71981/2S Max.	IDT71981/2L Min.	IDT71981/2L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	—	10	—	5	µA
			COM'L.	—	5	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}_{1,2}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	—	10	—	5	µA
			COM'L.	—	5	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		—	0.5	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.		2.4	—	2.4	—	V

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DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	71981/2S15 71981/2L15 Com'l.	71981/2S15 71981/2L15 Mil.	71981/2S20 71981/2L20 Com'l.	71981/2S20 71981/2L20 Mil.	71981/2S25 71981/2L25 Com'l.	71981/2S25 71981/2L25 Mil.	71981/2S35 71981/2L35 Com'l.	71981/2S35 71981/2L35 Mil.	71981/2S45 71981/2L45 Com'l.	71981/2S45 71981/2L45 Mil.	71981/2S55/70 71981/2L55/70 Com'l.	71981/2S55/70 71981/2L55/70 Mil.	71981/2S85 71981/2L85 Com'l.	71981/2S85 71981/2L85 Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS}_{1,2}$ = V_{IL}, Outputs Open V_{CC} = Max., f = 0(2)	S	100	—	100	105	100	105	100	105	—	105	—	105	—	105	mA
		L	75	—	70	80	70	80	70	80	—	80	—	80	—	80	
I_{CC2}	Dynamic Operating Current $\overline{CS}_{1,2}$ = V_{IL}, Outputs Open V_{CC} = Max., f = f_{MAX}(2)	S	135	—	130	160	125	155	125	140	—	140	—	140	—	140	mA
		L	125	—	115	130	105	125	105	115	—	110	—	110	—	105	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}_{1,2} \geq V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}(2)	S	60	—	55	70	50	60	45	50	—	50	—	50	—	50	mA
		L	45	—	40	50	35	50	30	40	—	35	—	35	—	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}_{1,2} \geq V_{HC}$, V_{CC}= Max., $V_{IN} \geq V_{HC}$ or $V_{IN} \leq V_{LC}$, f = 0(2)	S	20	—	15	25	15	20	15	20	—	20	—	20	—	20	mA
		L	1.5	—	0.5	1.5	0.5	1.5	0.5	1.5	—	1.5	—	1.5	—	1.5	

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NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

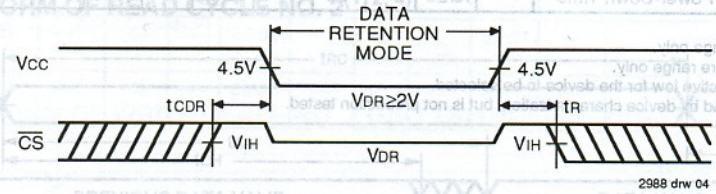
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.(1) Vcc @ 2.0v	Typ.(1) Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current		MIL.	—	10	15	600	900	µA
			COM'L.	—	10	15	150	225	
t_{CDR}(3)	Chip Deselect to Data Retention Time	$\overline{CS1}$ or $\overline{CS2} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$		0	—	—	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	—	—	ns
$\|I_{LI}\|$(3)	Input Leakage Current			—	—	—	2	2	µA

2988 tbl 09

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization, but is not production tested.

LOW Vcc DATA RETENTION WAVEFORM

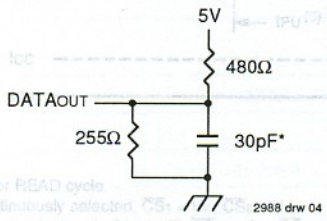


2988 drw 04

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2988 tbl 10



2988 drw 04

Figure 1. AC Test Load

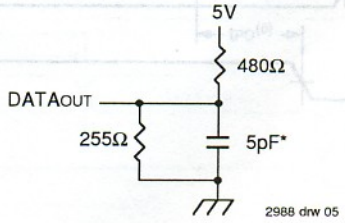


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Figure 2. AC Test Load
(for $t_{CLZ1, 2}$, t_{OLZ}, $t_{CHZ1, 2}$, t_{OHZ}, t_{OW} and t_{WHZ})

*Includes scope and jig capacitances

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71981/2S15[1]/20 71981/2L15[1]/20 Min.	Max.	71981/2S25 71981/2L25 Min.	Max.	71981/2S35/45[2] 71981/2L35/45[2] Min.	Max.	71981/2S55[2] 71981/2L55[2] Min.	Max.	71981/2S70[2] 71981/2L70[2] Min.	Max.	71981/2S85[2] 71981/2L85[2] Min.	Max.	Unit
Read Cycle														
tRC	Read Cycle Time	15/20	—	25	—	35/45	—	55	—	70	—	85	—	ns
tAA	Address Access Time	—	15/19	—	25	—	35/45	—	55	—	70	—	85	ns
tACS1,2	Chip Select-1,2 Access Time[3]	—	15/20	—	25	—	35/45	—	55	—	70	—	85	ns
tCLZ1,2	Chip Select-1,2 to Output in Low-Z[4]	5	—	5	—	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	8/9	—	11	—	20/25	—	35	—	45	—	55	ns
tOLZ	Output Enable to Output in Low-Z[4]	5	—	5	—	5	—	5	—	5	—	5	—	ns
tCHZ1,2	Chip Select1,2 to Output in High-Z[4]	—	7/8	—	10	—	4	—	20	—	25	—	30	ns
tOHZ	Output Disable to Output in High-Z[4]	—	7/8	—	9	—	15	—	20	—	25	—	30	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
tPU	Chip Select to Power-Up Time[4]	0	—	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Deselect to Power-Down Time[4]	—	15/20	—	25	—	35/45	—	55	—	70	—	85	ns

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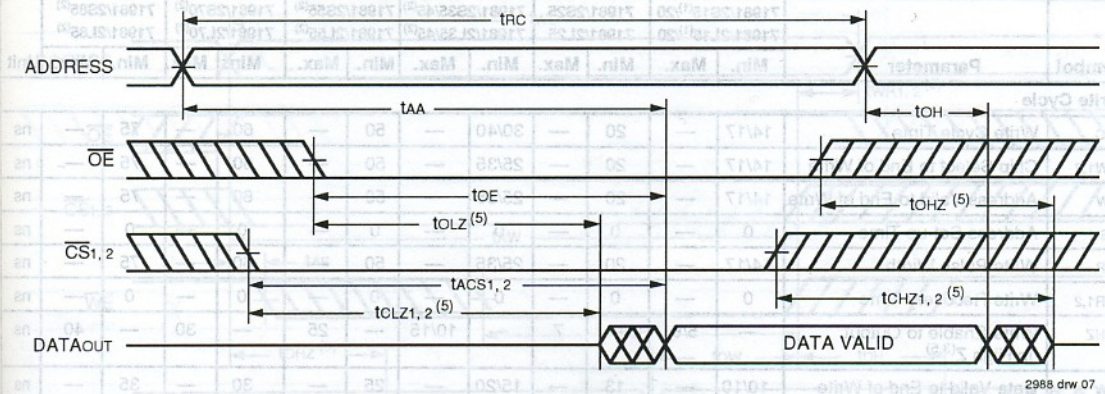
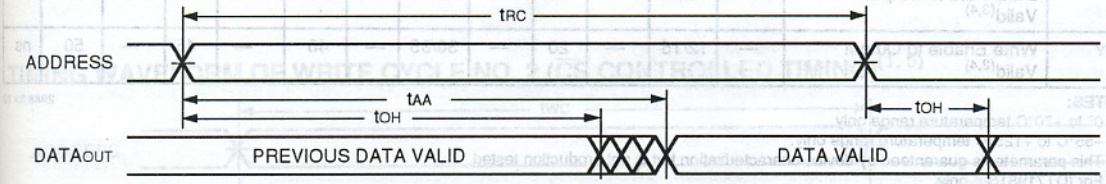
NOTES:
1. 0° to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. Both chip selects must be active low for the device to be selected.
4. This parameter is guaranteed by device characterization, but is not production tested.

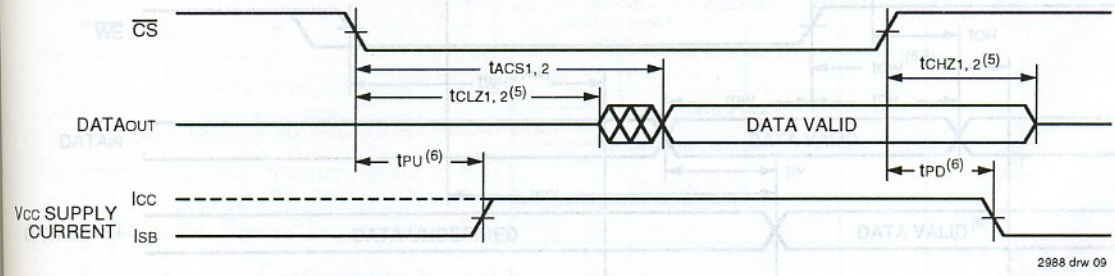
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



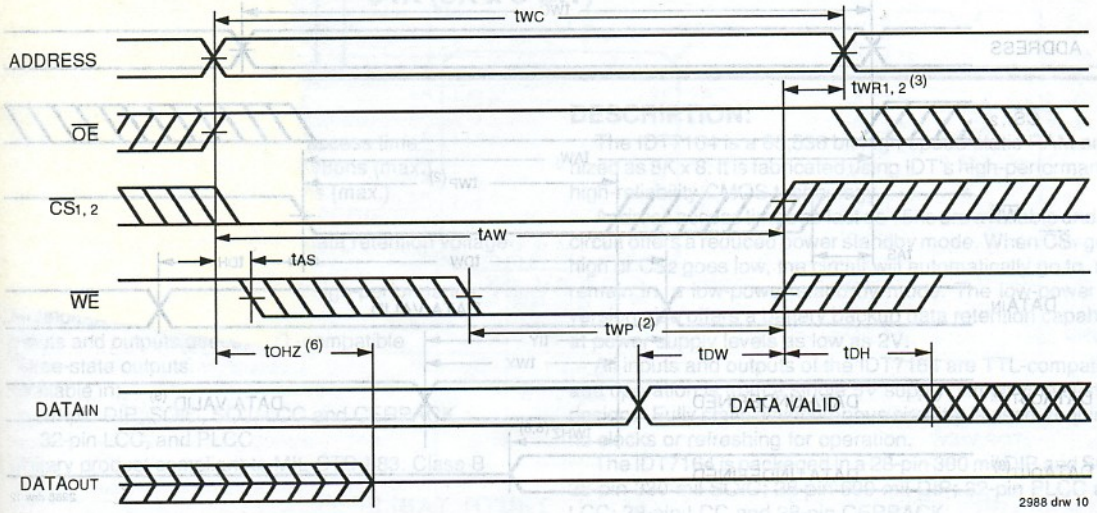
NOTES:
1. WE is HIGH for READ cycle.
2. Device is continuously selected, CS1 = VIL, CS2 = VIL.
3. Address valid prior to or coincident with CS1 and or CS2 transition low.
4. OE = VIL.
5. Transition is measured ±200mV from steady state voltage.
6. This parameter is guaranteed by device characterization but is not production tested.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71981/2S15[1]/20 71981/2L15[1]/20 Min.	Max.	71981/2S25 71981/2L25 Min.	Max.	71981/2S35/45[2] 71981/2L35/45[2] Min.	Max.	71981/2S55[2] 71981/2L55[2] Min.	Max.	71981/2S70[2] 71981/2L70[2] Min.	Max.	71981/2S85[2] 71981/2L85[2] Min.	Max.	Un
Write Cycle														
tWC	Write Cycle Time	14/17	—	20	—	30/40	—	50	—	60	—	75	—	n
tCW1,2	Chip Select to End of Write	14/17	—	20	—	25/35	—	50	—	60	—	75	—	n
tAW	Address Valid to End of Write	14/17	—	20	—	25/35	—	50	—	60	—	75	—	n
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	n
tWP	Write Pulse Width	14/17	—	20	—	25/35	—	50	—	60	—	75	—	n
tWR1,2	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	n
tWHZ	Write Enable to Output in High Z[3,5]	—	5/6	—	7	—	10/15	—	25	—	30	—	40	n
tDW	Data Valid to End of Write	10/10	—	13	—	15/20	—	25	—	30	—	35	—	n
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	n
tOW	Output Active from End of Write[3,5]	5	—	5	—	5	—	5	—	5	—	5	—	n
tIY	Data Valid to Output Valid[3,4]	—	12/15	—	20	—	30/35	—	40	—	45	—	50	n
tWY	Write Enable to Output Valid[3,4]	—	12/15	—	20	—	30/35	—	40	—	45	—	50	n

NOTES:
1. 0° to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. This parameter is guaranteed by device characterization but is not production tested.
4. For IDT71981S/L only.
5. For IDT71982S/L only.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1)



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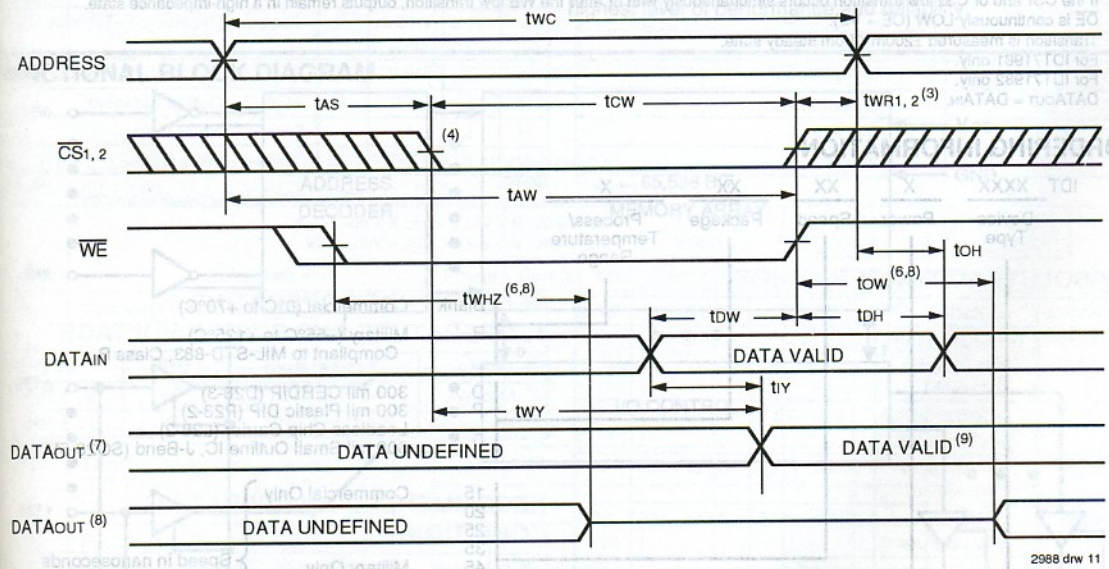
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 5)



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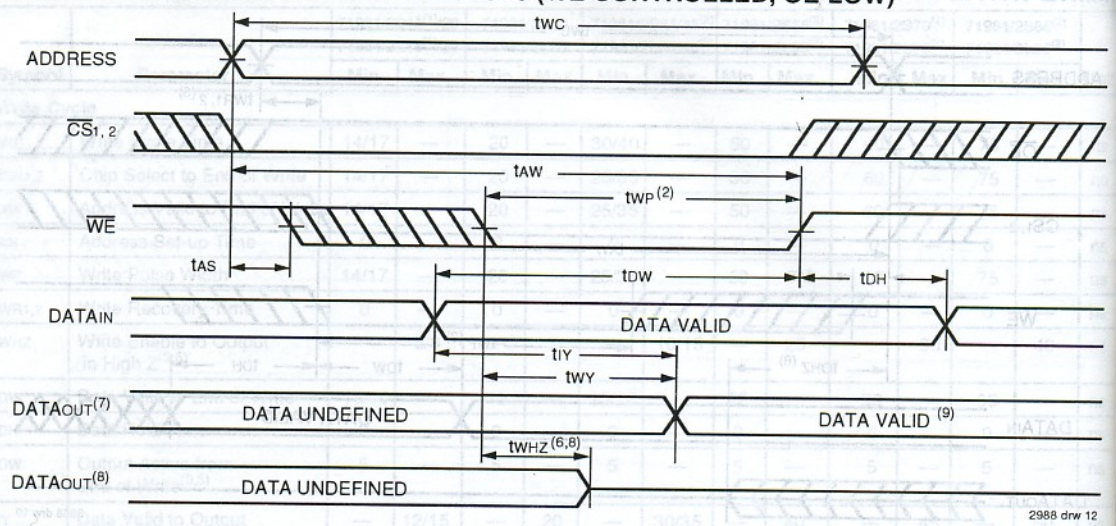
NOTES:
1. $\overline{WE}$ or $\overline{CS_1}$ or $\overline{CS_2}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a LOW $\overline{WE}$, a LOW $\overline{CS_1}$ and a low $\overline{CS_2}$.
3. t_{WR} is measured from the earlier of $\overline{CS_1}$, $\overline{CS_2}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. If the $\overline{CS_1}$ and or $\overline{CS_2}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, outputs remain in a high-impedance state.
5. $\overline{OE}$ is continuously LOW ($\overline{OE}$ = V_{IL}).
6. Transition is measured ±200mV from steady state.
7. For IDT71981 only.
8. For IDT71982 only.
9. $DATA_{OUT}$ = $DATA_{IN}$.

TIMING WAVEFORM OF WRITE CYCLE NO. 3 ($\overline{WE}$ CONTROLLED, $\overline{OE}$ LOW)(1, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}_1$ or $\overline{CS}_2$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a LOW $\overline{WE}$, a low $\overline{CS}_1$ and a LOW $\overline{CS}_2$.
3. t_{WR} is measured from the earlier of $\overline{CS}_1$, $\overline{CS}_2$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. If the $\overline{CS}_1$ and or $\overline{CS}_2$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, outputs remain in a high-impedance state.
5. $\overline{OE}$ is continuously LOW ($\overline{OE}$ = V_{IL}).
6. Transition is measured ±200mV from steady state.
7. For IDT71981 only.
8. For IDT71982 only.
9. $DATA_{OUT}$ = $DATA_{IN}$.

ORDERING INFORMATION