



FAST CMOS OCTAL BIDIRECTIONAL TRANSCEIVER

IDT74FCT645T/AT/CT/DT

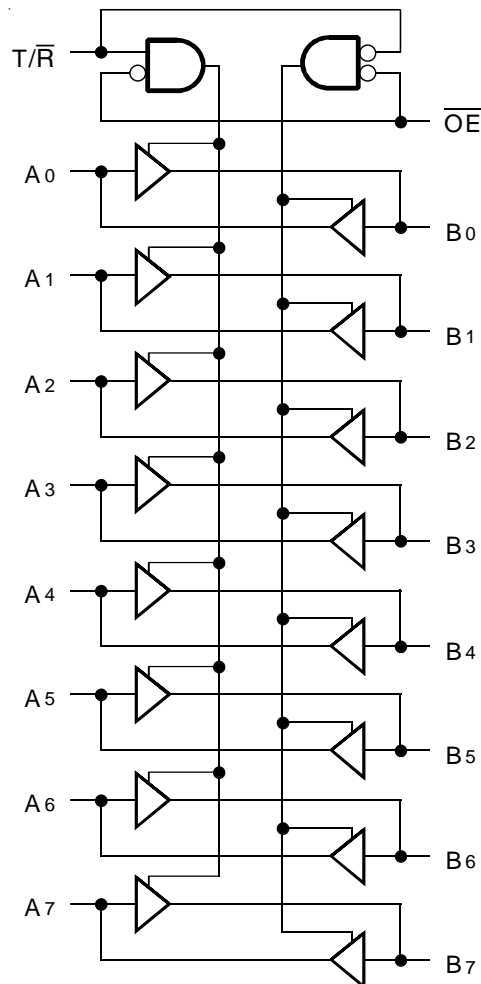
FEATURES:

- Std., A, C, and D grades
- Low input and output leakage $\leq 1\mu\text{A}$ (max.)
- CMOS power levels
- True TTL input and output compatibility:
 - $V_{OH} = 3.3V$ (typ.)
 - $V_{OL} = 0.3V$ (typ.)
- High Drive outputs (-15mA I_{OH} , 64mA I_{OL})
- Meets or exceeds JEDEC standard 18 specifications
- Available in SOIC and QSOP packages

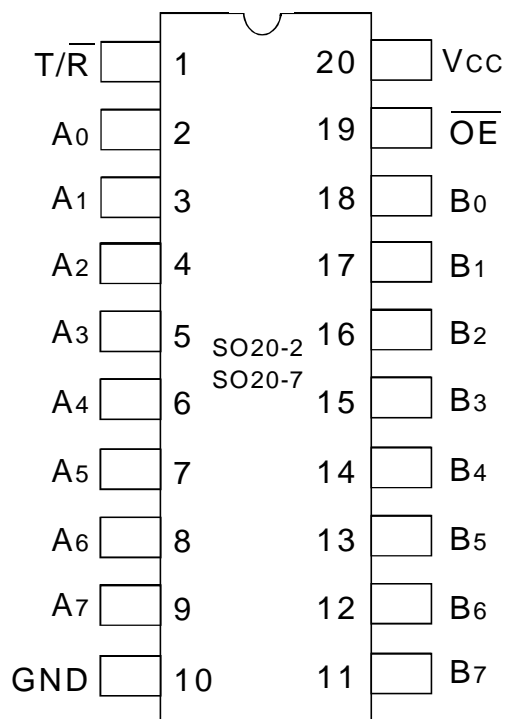
DESCRIPTION:

The IDT octal bidirectional transceivers are built using an advanced dual metal CMOS technology. The FCT645T is designed for asynchronous two-way communication between data buses. The transmit/receive (T/\bar{R}) input determines the direction of data flow through the bidirectional transceiver. Transmit (active high) enables data from A ports to B ports, and receive (active low) from B ports to A ports. The output enable (\overline{OE}) input, when high, disables both A and B ports by placing them in high Z condition.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SOIC/ SSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC} +0.5	V
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-60 to +120	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
- Inputs and V_{CC} terminals only.
- Output and I/O terminals only.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
\overline{OE}	Output Enable Input (Active LOW)
$\overline{T/R}$	Transmit/Receive Input
A ₀ - A ₇	Side A Inputs or 3-State Outputs
B ₀ - B ₇	Side B Inputs or 3-State Outputs

FUNCTION TABLE⁽¹⁾

Inputs		Outputs
\overline{OE}	$\overline{T/R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

NOTE:

- H = HIGH Voltage Level
X = Don't Care
L = LOW Voltage Level

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_I = 2.7\text{V}$	—	—	± 1	μA
I_{IL}	Input LOW Current ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_I = 0.5\text{V}$	—	—	± 1	μA
I_{OZH}	High Impedance Output Current (3-State Output Pins) ⁽⁴⁾	$V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$	$V_I = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}			$V_I = 0.5\text{V}$	—	—	± 1	
I_I	Input HIGH Current	$V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$		—	—	± 1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND or } V_{CC}$		—	0.01	1	mA

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -8\text{mA}$	2.4	3.3	—	V
			$I_{OH} = -15\text{mA}$	2	3	—	
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 64\text{mA}$	—	0.3	0.55	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-60	-120	-225	mA

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0\text{V}$, $+25^\circ\text{C}$ ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^\circ\text{C}$.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{OE} = T/\overline{R} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{OE} = T/\overline{R} = \text{GND}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	1.5	3.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	1.8	4.5	
		$V_{CC} = \text{Max.}$ Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{OE} = T/\overline{R} = \text{GND}$ Four Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3	6 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	5	14 ⁽⁵⁾	

NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of ΔI_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_{HT} + I_{CCD} (f_i N_i)$
 $I_{CC} = \text{Quiescent Current}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $f_i = \text{Output Frequency}$
 $N_i = \text{Number of Outputs at } f_i$

All currents are in milliamps and all frequencies are in megahertz.

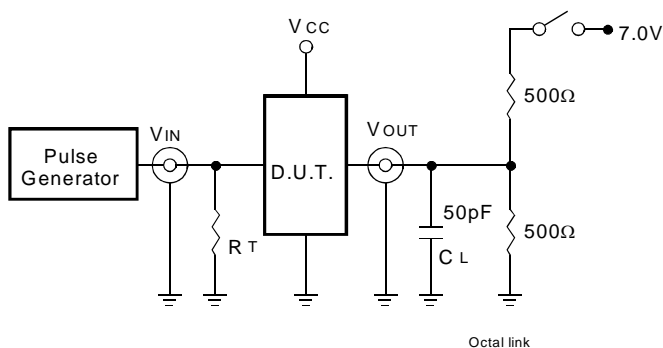
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	IDT74FCT645T		IDT74FCT645AT		IDT74FCT645CT		IDT74FCT645DT		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t_{PLH}	Propagation Delay	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	9.5	1.5	4.6	1.5	4.1	1.5	3.8	ns
t_{PHL}	A to B, B to A										
t_{PZH}	Output Enable Time		1.5	11	1.5	6.2	1.5	5.8	1.5	5	
t_{PZL}	\overline{OE} to A or B										
t_{PHZ}	Output Disable Time		1.5	12	1.5	5	1.5	4.8	1.5	4.3	
t_{PLZ}	\overline{OE} to A or B										
t_{PZH}	Output Enable Time	T/\overline{R} to A or B ⁽³⁾	1.5	11	1.5	6.2	1.5	5.8	1.5	5	ns
t_{PZL}	T/\overline{R} to A or B ⁽³⁾										
t_{PHZ}	Output Disable Time	T/\overline{R} to A or B ⁽³⁾	1.5	12	1.5	5	1.5	4.8	1.5	4.3	ns
t_{PLZ}	T/\overline{R} to A or B ⁽³⁾										

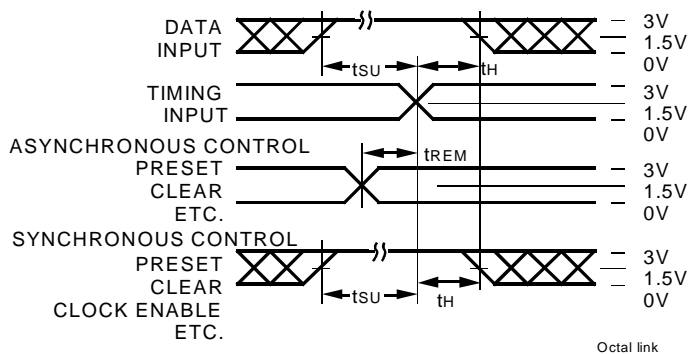
NOTES:

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter is guaranteed but not tested.

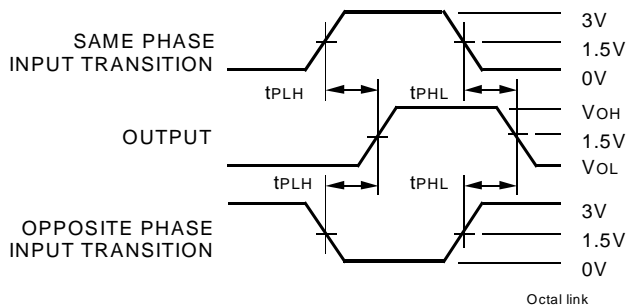
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-Up, Hold, and Release Times



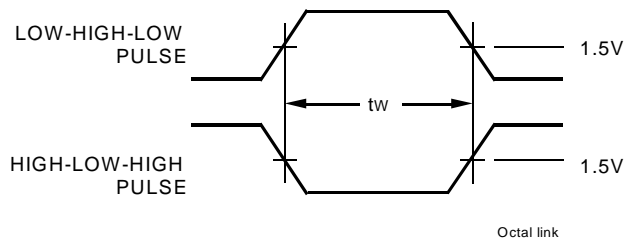
Propagation Delay

SWITCH POSITION

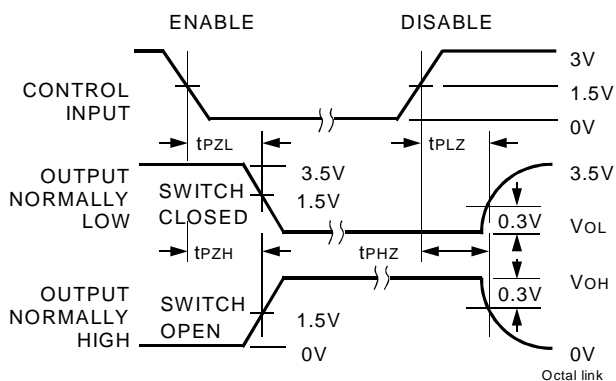
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

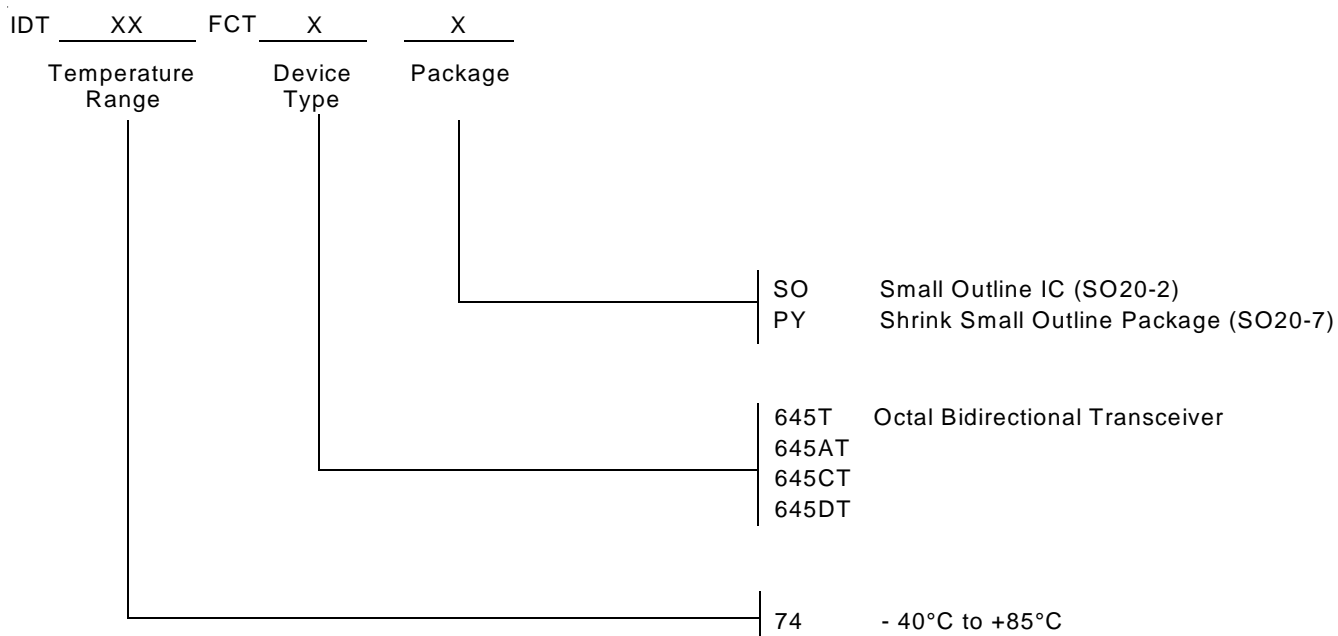


Enable and Disable Times

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$.

ORDERING INFORMATION



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