HIGH-PERFORMANCE CMOS BUS INTERFACE LATCH

IDT74FCT841A/B

FEATURES:

- **Equivalent to AMD's Am29841 bipolar registers in pinout/ function, speed, and output drive over full temperature and voltage supply extremes**
- **IDT74FCT841A equivalent to FAST™ speed**
- **IDT74FCT841B 25% faster than FAST**
- **Buffered common latch enable, clear and present inputs**
- **I_{OL} = 48mA**
- **Clamp diodes on all inputs for ringing suppression**
- **CMOS power levels (1mW typ. static)**
- **TTL input and output level compatible**
- **CMOS output level compatible**
- **Substantially lower input current levels than AMD's bilopar Am29800 series (5µA max.)**
- **Available in SOIC package**

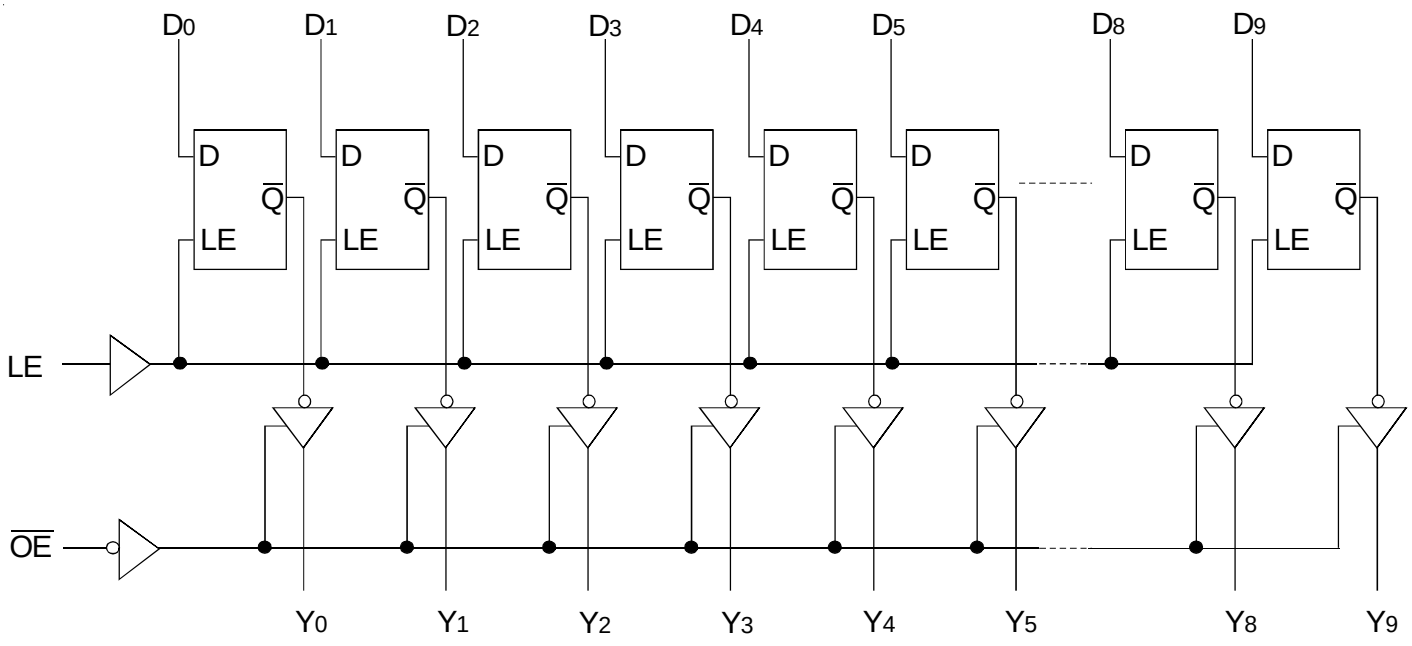
DESCRIPTION:

The IDT74FCT800 series is built using an advanced dual metal CMOS technology.

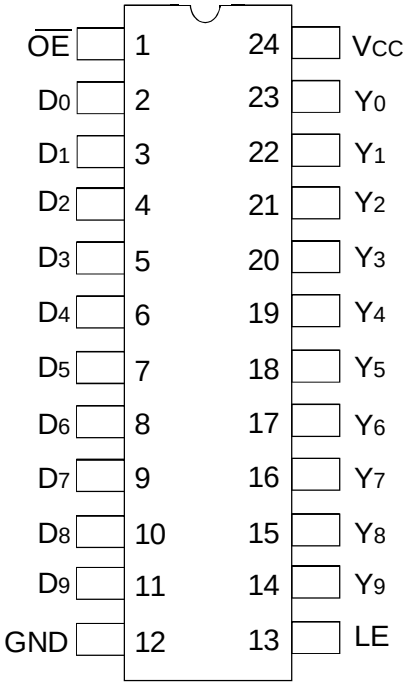
The IDT74FCT840 series bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The IDT74FCT841 is a buffered, 10-bit wide version of the popular '373 function.

All of the IDT74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high-impedance state.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SOIC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature under BIAS	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	120	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Output and I/O terminals only.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	I/O	Description
Dx	I	Latch Data Inputs
LE	I	Latch Enable Input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Yx	O	3-State Latch Outputs
$\overline{OE}$	I	Output Enable Control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs Yx are in high-impedance (off) state.

FUNCTION TABLE(1)

Inputs			Internal	Output	
$\overline{OE}$	LE	Dx	Qx	Yx	Function
H	X	X	X	Z	High Z
H	H	L	L	Z	High Z
H	H	H	H	Z	High Z
H	L	X	NC	Z	Latched (High Z)
L	H	L	L	L	Transparent
L	H	H	H	H	Transparent
L	L	X	NC	NC	Latched
H	L	X	L	Z	Latched (High Z)
H	L	X	H	Z	Latched (High Z)

NOTE:
1. H = HIGH Voltage Level
   X = Don't Care
   L = LOW Voltage Level
   Z = High-Impedance
   NC = No Change

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5[4]	
			V_I = GND	—	—	–5	
I_{OZH}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	10	µA
			V_O = 2.7V	—	—	10[4]	
I_{OZL}			V_O = 0.5V	—	—	–10[4]	
			V_O = GND	—	—	–10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–75	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –24mA	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min	I_{OL} = 300µA	—	GND	V_{LC}[4]	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA	—	0.3	0.5	

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not ttested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4	mA
		50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	2	5	
		V_{CC} = Max. Outputs Open fi = 2.5MHz	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.2	6.5[5]	
		50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	5.2	14.5[5]	

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of ΔI_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for register devices (zero for non-register devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

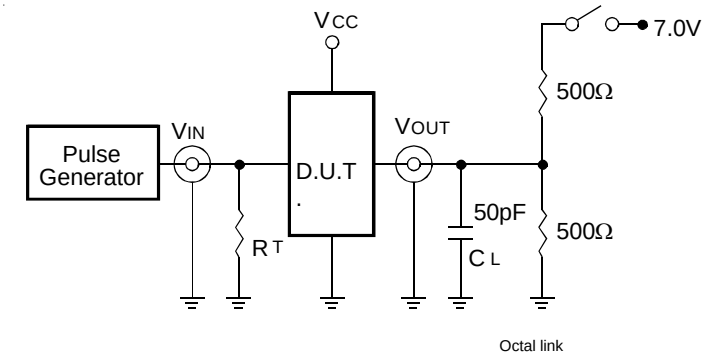
All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

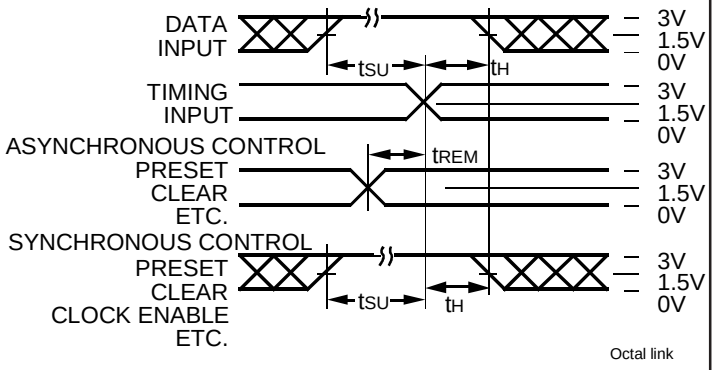
Symbol	Parameter	Condition[1]	74FCT841A		74FCT841B		Unit
			Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay Dx to Yx (LE = HIGH)	C_L = 50pF R_L = 500Ω	1.5	9	1.5	6.5	ns
		C_L = 300pF[4] R_L = 500Ω	1.5	13	1.5	13	
t_{PLH} t_{PHL}	Propagation Delay LE to Yx	C_L = 50pF R_L = 500Ω	1.5	12	1.5	8	ns
		C_L = 300pF[4] R_L = 500Ω	1.5	16	1.5	15.5	
t_{PZH} t_{PZL}	Output Enable Time, $\overline{OE}$ to Yx	C_L = 50pF R_L = 500Ω	1.5	11.5	1.5	8	ns
		C_L = 300pF[4] R_L = 500Ω	1.5	23	1.5	14	
t_{PHZ} t_{PLZ}	Output Disable Time, $\overline{OE}$ to Yx	C_L = 5pF[4] R_L = 500Ω	1.5	7	1.5	6	ns
		C_L = 50pF R_L = 500Ω	1.5	18	1.5	7	
t_{SU}	Data to LE Set-up Time	C_L = 50pF R_L = 500Ω	2.5	—	2.5	—	ns
t_H	Data to LE Hold Time		2.5	—	2.5	—	ns
t_W	LE Pulse Width HIGH[3]		4	—	4	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.
4. This condition is guaranteed but not tested.

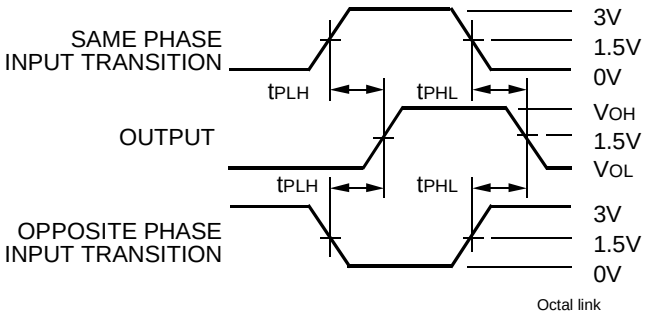
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-Up, Hold, and Release Times



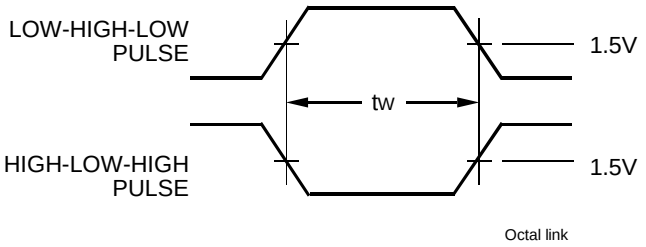
Propagation Delay

SWITCH POSITION

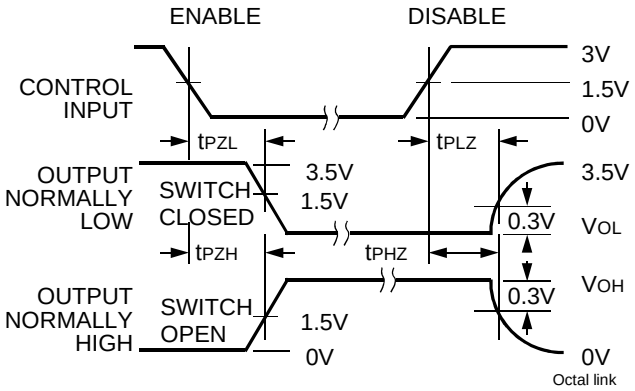
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.



Pulse Width

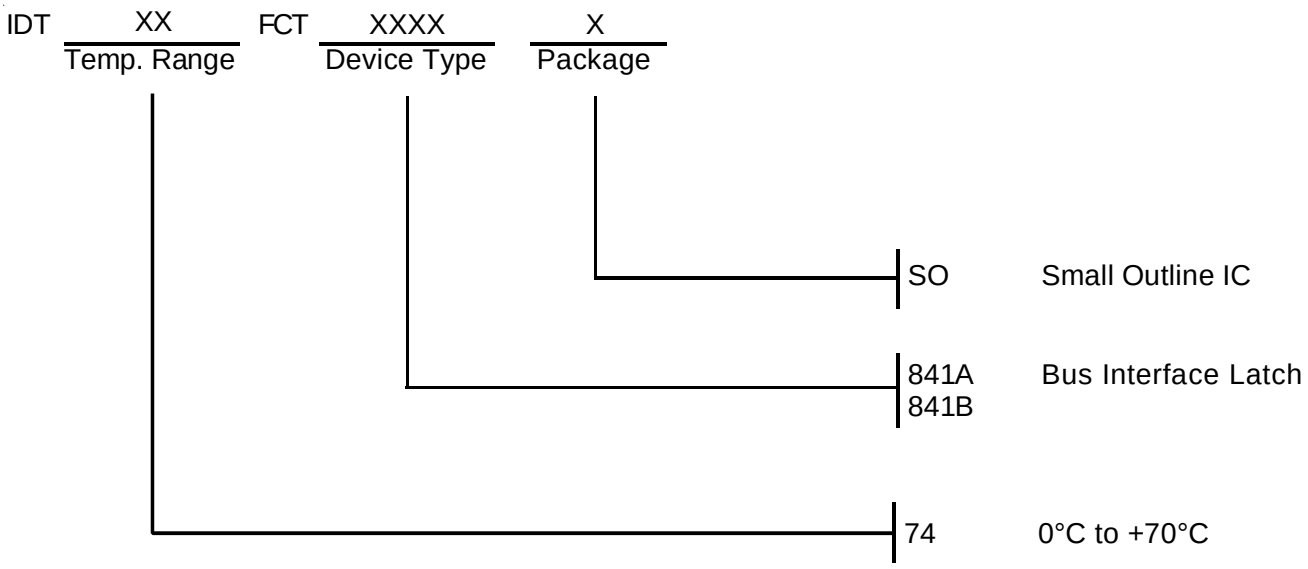


Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_O ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



DATA SHEET DOCUMENT HISTORY

6/27/2002 Updated according to PDNs Logic-00-07 and Logic-01-04

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