# 82C284

## Clock Generator and Ready Interface for 80C286 Processors

March 1997

### Features

- **Generates System Clock for 80C286 Processors**
- **Generates System Reset Output from Schmitt Trigger Input**
  - **Improved Hysteresis**
- **Uses Crystal or External Signal for Frequency Source**
- **Dynamically Switchable between Two Input Frequencies**
- **Provides Local $\overline{\text{READY}}$ and MULTIBUS® $\overline{\text{READY}}$ Synchronization**
- **Static CMOS Technology**
- **Single +5V Power Supply**
- **Available in 18 Lead CerDIP Package**

### Description

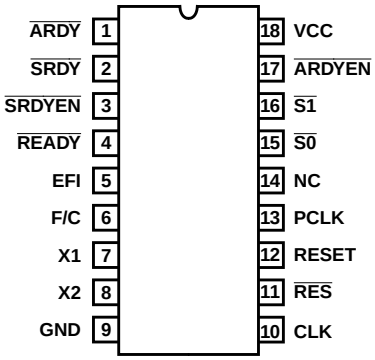
The Intersil 82C284 is a clock generator/driver which provides clock signals for 80C286 processors and support components. It also contains logic to supply $\overline{\text{READY}}$ to the CPU from either asynchronous or synchronous sources and synchronous RESET from an asynchronous input with hysteresis.

### Ordering Information

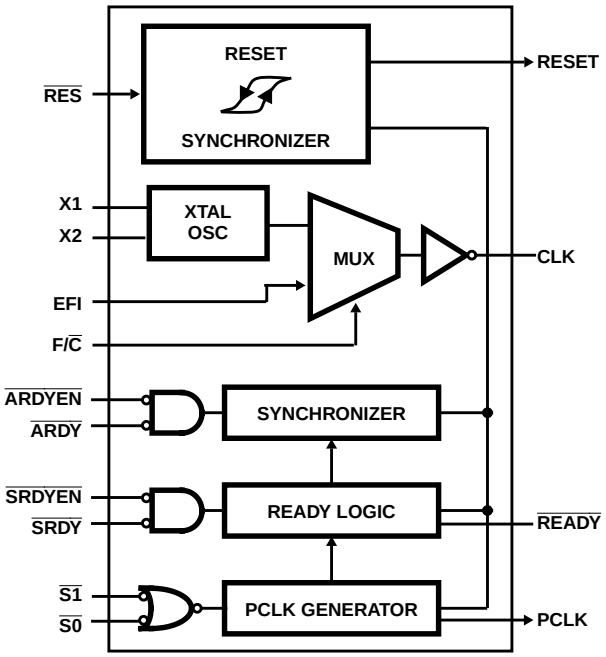
| PART NUMBER | TEMP. RANGE | PACKAGE | PKG. NO. |
|---|---|---|---|
| CD82C284-12 | $0^oC$ to $+70^oC$ | 18 Ld CERDIP | F18.3 |
| ID82C284-10 | $-40^oC$ to $+85^oC$ | 18 Ld CERDIP | F18.3 |
| ID82C284-12 | $-40^oC$ to $+85^oC$ | 18 Ld CERDIP | F18.3 |

### Pinout

**82C284 (CERDIP)**
TOP VIEW




### Functional Diagram



## Pin Description

The following pin function descriptions are for the 82C284 clock generator.

| PIN SYMBOL | NUMBER | TYPE | DESCRIPTION |
|---|---|---|---|
| CLK | 10 | O | SYSTEM CLOCK: the signal used by the processor and support devices which must be synchronous with the processor. The frequency of the CLK output has twice the desired internal processor clock frequency. CLK can drive both TTL and CMOS level inputs. |
| F/$\overline{C}$ | 6 | I | FREQUENCY/CRYSTAL SELECT: this pin selects the source for the CLK output. When there is a LOW level on this input, the internal crystal oscillator drives CLK. When there is a HIGH level on F/$\overline{C}$, the EFI input drives the CLK input. This pin can be dynamically switched, which allows changing the processor CLK frequency while running for low-power operation, etc. |
| X1, X2 | 7, 8 | I | CRYSTAL IN: the pin stop which parallel resonant, fundamental mode crystal is attached for the internal oscillator. When F/$\overline{C}$ is LOW, the internal oscillator will drive the CLK output at the crystal frequency. The crystal frequency must be twice the desired internal processor clock frequency. |
| EFI | 5 | I | EXTERNAL FREQUENCY IN: drives CLK when the F/$\overline{C}$ input is HIGH. The EFI input frequency must be twice the desired internal processor clock frequency. |
| PCLK | 13 | O | PERIPHERAL CLOCK: the output which provides a 50% duty cycle clock with one-half the frequency of CLK. PCLK will be in phase with the internal processor clock following the first bus cycle after the processor has been reset. |
| $\overline{ARDYEN}$ | 17 | I | ASYNCHRONOUS READY ENABLE: an active LOW input which qualifies the $\overline{ARDY}$ input. $\overline{ARDYEN}$ selects $\overline{ARDY}$ as the source of $\overline{READY}$ for the current bus cycle. Inputs to $\overline{ARDYEN}$ may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous outputs. |
| $\overline{ARDY}$ | 1 | I | ASYNCHRONOUS READY: an active LOW input used to terminate the current bus cycle. The $\overline{ARDY}$ input is qualified by $\overline{ARDYEN}$. Inputs to $\overline{ARDY}$ may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous outputs. |
| $\overline{SRDYEN}$ | 3 | I | SYNCHRONOUS READY ENABLE: an active LOW input which qualifies $\overline{SRDY}$. $\overline{SRDYEN}$ selects $\overline{SRDY}$ as the source for $\overline{READY}$ to the CPU for the current bus cycle. Setup and hold time must be satisfied for proper operation. |
| $\overline{SRDY}$ | 2 | I | SYNCHRONOUS READY: an active LOW input used to terminate the current bus cycle. The $\overline{SRDY}$ input is qualified by the $\overline{SRDYEN}$ input. Setup and hold time must be satisfied for proper operation. |
| $\overline{READY}$ | 4 | O | READY: an active LOW output which signals to the processor that the current bus cycle is to be completed. The $\overline{SRDY}$ $\overline{SRDYEN}$, $\overline{ARDY}$, $\overline{ARDYEN}$, $\overline{S1}$, $\overline{S0}$, and $\overline{RES}$ inputs control $\overline{READY}$ as explained later in the $\overline{READY}$ generator section. $\overline{READY}$ is an open drain output requiring an external pull-up resistor. |
| $\overline{S0}$, $\overline{S1}$ | 15,16 | I | STATUS: these inputs prepare the 82C284 for a subsequent bus cycle. $\overline{S0}$ and $\overline{S1}$ synchronize PCLK to the internal processor clock and control READY. Setup and hold times must be satisfied for proper operation |
| RESET | 12 | O | RESET: an active HIGH output which is derived from the $\overline{RES}$ input RESET is used to force the system into an initial state. When RESET is active, $\overline{READY}$ will be active (LOW). |
| $\overline{RES}$ | 11 | I | RESET IN: an active LOW input which generates the system reset signal (RESET). Signals to $\overline{RES}$ may be applied asynchronously to CLK. A Schmitt trigger input is provided on $\overline{RES}$, so that an RC circuit can be used to provide a time delay. Setup and hold times are given to assure a guaranteed response to synchronous inputs. |
| $V_{CC}$ | 18 | | SYSTEM POWER: The +5V Power Supply Pin. A 0.1µF capacitor between $V_{CC}$ and GND is recommended for decoupling. |
| GND | 9 | | SYSTEM GROUND: 0V |

## Functional Description

### Introduction

The 82C284 generates the clock, ready, and reset signals required for 80C286 processors and support components. The 82C284 is packaged in an 18-pin DIP and contains a crystal controlled oscillator, clock generator, peripheral clock generator, MULTIBUS® ready synchronization logic, and system reset generation logic.

### Clock Generator

The CLK output provides the basic timing control for an 80C286 system. CLK has output characteristics sufficient to drive CMOS devices. CLK is generated by either an internal crystal oscillator, or an external source as selected by the F/$\overline{C}$ input pin. When F/$\overline{C}$ is LOW, the crystal oscillator drives the CLK output. When F/$\overline{C}$ is HIGH, the EFI input drives the CLK output.

The F/$\overline{C}$ pin on the Intersil 82C284 is dynamically switchable. This allows the CLK frequency to the processor to be changed from one frequency to another in a running system. With this feature, a system can be designed which operates at maximum speed when needed, and then dynamically switched to a lower frequency to implement a low-power mode. The lower frequency can be anything down to, but excluding, DC. The following 3 conditions apply when dynamically switching the F/$\overline{C}$ pin (see Figure 1):

1) The CLK is stretched in the low portion of the $\phi$2 phase of its cycle during transition from one CLK frequency to the other (see Waveforms).

2) When switching CLK frequency sources, there is a maximum transition latency of 2.5 clock cycles of the frequency being switched to, from the time CLK freezes low, until CLK restarts at the new frequency (see Waveforms).

3) The maximum latency from the time F/C is dynamically switched, to the time CLK freezes low, is 4 CLK cycles (see Waveforms).

The following steps describe the sequence of events that transpire when F/C is dynamically switched:

A) F/$\overline{C}$ switched from high (using EFI input) to low (using the crystal input X1 - see Figure 1A).

   1) The state of F/$\overline{C}$ is sampled when both CLK and PCLK are high until a change is detected.

   2) On the second following falling edge of PCLK, CLK is frozen low.

   3) CLK restarts at the crystal frequency on the rising edge of Xl, after the second falling edge of X1.

B) F/$\overline{C}$ switched from low (using the crystal input Xl) to high (using the EFI input - see Figure 1B).

   1) The state of F/C is sampled when both CLK and PCLK are high until a change is detected.

   2) On the second following falling edge of PCLK, CLK is frozen low.

   3) CLK restarts at the EFI input frequency on the falling edge of EFl after the second rising edge of EFI.

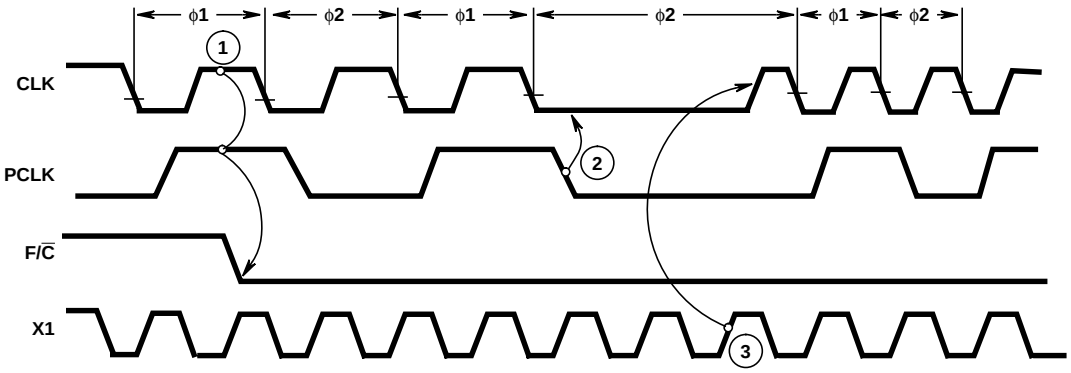



**FIGURE 1A. F/$\overline{C}$ SWITCHED FROM HIGH (USING EFI INPUT) TO LOW (USING THE CRYSTAL INPUT X1)**

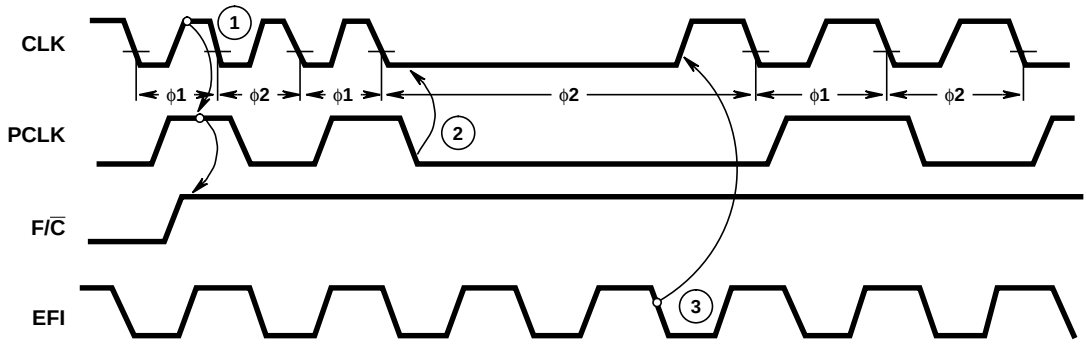



**FIGURE 1B. F/C SWITCHED FROM LOW (USING THE CRYSTAL INPUT X1) TO HIGH (USING THE EFI INPUT)**
**FIGURE 1. DYNAMICALLY SWITCHING THE F/$\overline{C}$ PIN**

The 82C284 provides a second clock output, PCLK, for peripheral devices. PCLK is CLK divided by two. PCLK has a duty cycle of 50% and CMOS output drive characteristics. PCLK is normally synchronized to the internal processor clock.

After reset, the PCLK signal may be out of phase with the internal processor clock. The $\overline{S1}$ and $\overline{S0}$ signals of the first bus cycle are used to synchronize PCLK to the internal processor clock. The phase of the PCLK output changes by extending its HIGH time beyond one system clock (see waveforms). PCLK is forced HIGH whenever either $\overline{S0}$ or $\overline{S1}$ were active (LOW) for the two previous CLK cycles. PCLK continues to oscillate when both $\overline{S0}$ and $\overline{S1}$ are HIGH.

Since the phase of the internal processor clock will not change except during reset, the phase of PCLK will not change except during the first bus cycle after reset.

### Oscillator

The oscillator circuit of the 82C284 is a linear Pierce oscillator which requires an external parallel resonant, fundamental mode, crystal. The output of the oscillator is internally buffered. The crystal frequency chosen should be twice the required internal processor clock frequency. The crystal should have a typical load capacitance of 32pF.

X1 and X2 are the oscillator crystal connections. For stable operation of the oscillator, two loading capacitors are recommended, as shown in Table 1. The sum of the board capacitance and loading capacitance should equal the values shown. It is advisable to limit stray board capacitances (not including the effect of the loading capacitors or crystal capacitance) to less than 10pF between the X1 and X2 pins. Decouple $V_{CC}$ and GND as close to the 82C284 as possible with a 0.1µF polycarbonate capacitor.

**TABLE 1. 82C284 CRYSTAL LOADING CAPACITANCE VALUES**

| CRYSTAL FREQUENCY | CI CAPACITANCE (PIN 7) | C2 CAPACITANCE (PIN 8) |
|---|---|---|
| 1MHz to 8MHz | 60pF | 40pF |
| 8MHz to 20MHz | 25pF | 15pF |
| 20MHz to 25MHz | 15pF | 15pF |

### CLK Termination

Due to the CLK output having a very fast rise and fall time, it is recommended to properly terminate the CLK line at frequencies above 10MHz to avoid signal reflections and ringing. Termination is accomplished by inserting a small resistor (typically 10-74Ω) in series with the output, as shown in Figure 2. This is known as series termination. The resistor value plus the circuit output impedance (approximately 25Ω) should be made equal to the impedance of the transmission line.

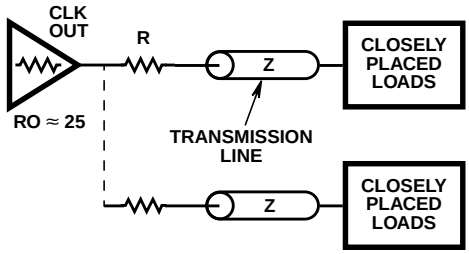



**FIGURE 2. SERIES TERMINATION**

### Reset Operation

The reset logic provides the RESET output to force the system into a known, initial state. When the $\overline{RES}$ input is active (LOW), the RESET output becomes active (HIGH), $\overline{RES}$ is synchronized internally at the falling edge of CLK before generating the RESET output (see waveforms). Synchronization of the $\overline{RES}$ input introduces a one or two CLK delay before affecting the RESET Output.

At power up, a system does not have a stable $V_{CC}$ and CLK. To prevent spurious activity, $\overline{RES}$ should be asserted until $V_{CC}$ and CLK stabilize at their operating values. 80C286 processors and support components also require their RESET inputs be HIGH a minimum of 16 CLK cycles. An RC network, as shown in Figure 3, will keep $\overline{RES}$ LOW long enough to satisfy both needs.

A Schmitt trigger input with hysteresis on $\overline{RES}$ assures a single transition of RESET with an RC circuit on $\overline{RES}$. The hysteresis separates the input voltage level at which the circuit output switches from HIGH to LOW from the input voltage level at which the circuit output switches from LOW to HIGH. The $\overline{RES}$ HIGH to LOW input transition voltage is lower than the $\overline{RES}$

LOW to HIGH input transition voltage. As long as the slope of the $\overline{RES}$ input voltage remains in the same direction (increasing or decreasing) around the $\overline{RES}$ input transition voltage, the RESET output will make a single transition.

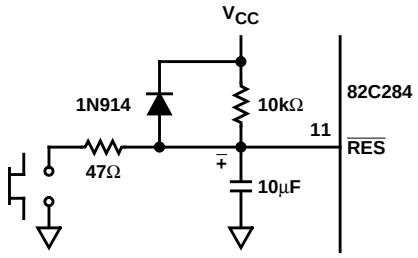



**FIGURE 3. TYPICAL RC $\overline{RES}$ TIMING CIRCUIT**

### Ready Operation

The 82C284 accepts two ready sources for the system ready signal which terminates the current bus cycle. Either a synchronous ($\overline{SRDY}$) or asynchronous ready ($\overline{ARDY}$) source may be used. Each ready input has an enable ($\overline{SRDYEN}$ and $\overline{ARDYEN}$) for selecting the type of ready source required to terminate the current bus cycle. An address decoder would normally select one of the enable inputs.

$\overline{READY}$ is enabled (LOW), if either $\overline{SRDY}$ + $\overline{SRDYEN}$ = 0 or $\overline{ARDY}$ + $\overline{ARDYEN}$ = 0 when sampled by the 82C284 $\overline{READY}$ generation logic. $\overline{READY}$ will remain active for at least two CLK cycles.

The $\overline{READY}$ output has an open-drain driver allowing other ready circuits to be wired with it, as shown in Figure 4. The $\overline{READY}$ signal of an 80C286 system requires an external pull-up resistor. To force the $\overline{READY}$ signal inactive (HIGH) at the start of a bus cycle, the $\overline{READY}$ output floats when either $\overline{S1}$ or $\overline{S0}$ are sampled LOW at the falling edge of CLK. Two system clock periods are allowed for the pull-up resistor to pull the $\overline{READY}$ signal to $V_{IH}$. When RESET is active, $\overline{READY}$ is forced active one CLK later (see Waveforms).

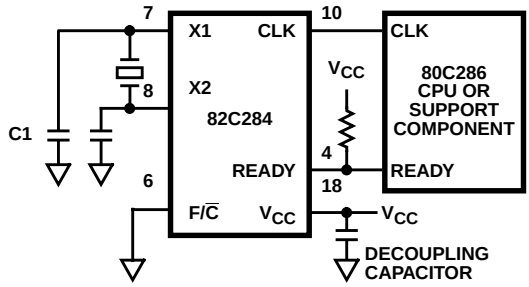



**FIGURE 4. RECOMMENDED CRYSTAL AND $\overline{READY}$ CONDITIONS**

Figure 5 illustrates the operation of $\overline{SRDY}$ and $\overline{SRDYEN}$. These inputs are sampled on the falling edge of CLK when $\overline{S1}$ and $\overline{S0}$ are inactive and PCLK is HIGH. $\overline{READY}$ is forced active when both $\overline{SRDY}$ and $\overline{SRDYEN}$ are sampled as LOW.

Figure 6 shows the operation of $\overline{ARDY}$ and $\overline{ARDYEN}$ These inputs are sampled by an internal synchronizer at each falling edge of CLK. The output of the synchronizer is then sampled when PCLK is HIGH. If the synchronizer resolved both the $\overline{ARDY}$ and $\overline{ARDYEN}$ as active, the $\overline{SRDY}$ and $\overline{SRDYEN}$ inputs are ignored. Either $\overline{ARDY}$ or $\overline{ARDYEN}$ must be HIGH at the end of $T_S$, therefore, at least one wait state is required when using the $\overline{ARDY}$ and $\overline{ARDYEN}$ inputs as a basis for generating $\overline{READY}$.

$\overline{READY}$ remains active until either $\overline{S1}$ or $\overline{S0}$ are sampled LOW, or the ready inputs are sampled as inactive.

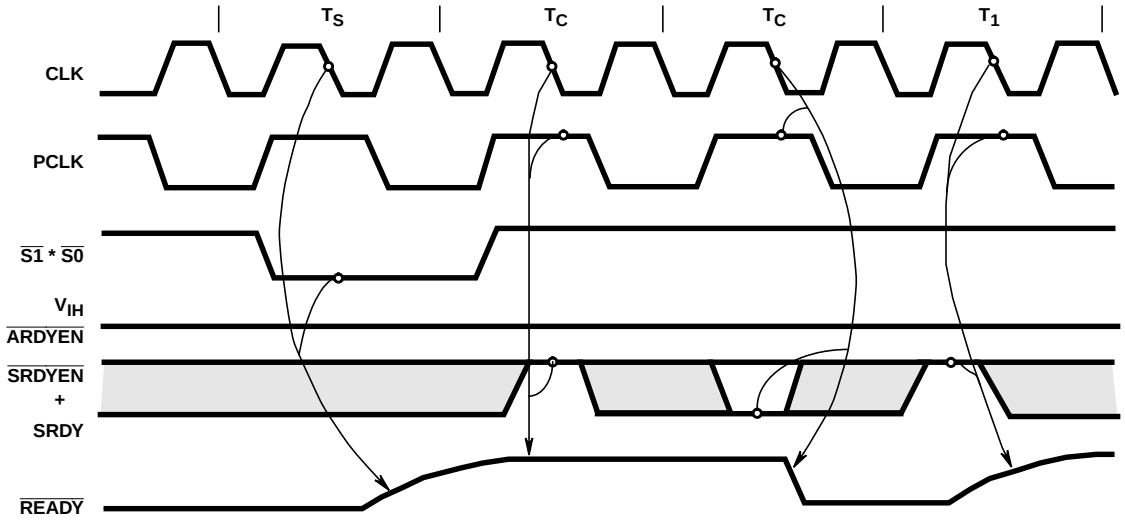



FIGURE 5. SYNCHRONOUS READY OPERATION

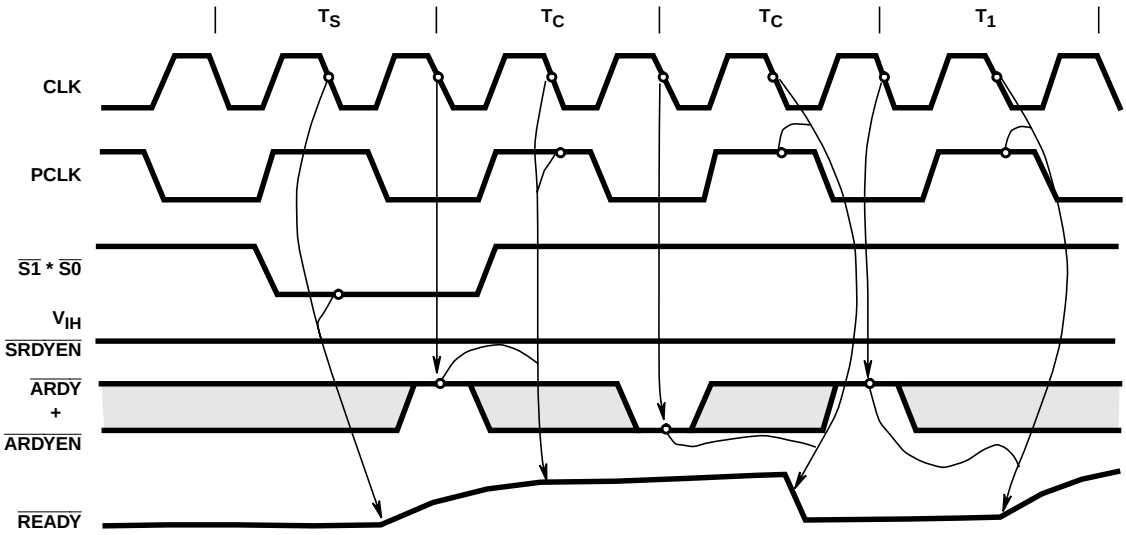



FIGURE 6. ASYNCHRONOUS READY OPERATION

## Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage Applied . . . . . GND -0.5V to $V_{CC}$ +0.5V
Storage Temperature Range . . . . . $-65^oC$ to $+150^oC$

## Thermal Information

| Thermal Resistance | $\theta_{JA}$ ($^oC/W$) | $\theta_{JC}$ ($^oC/W$) |
|---|---|---|
| CERDIP Package | 80 | 20 |

Gate Count . . . . . 200 Gates
Junction Temperature . . . . . $+175^oC$
Lead Temperature (Soldering, 10s) . . . . . $+300^oC$
ESD Classification . . . . . Class 2

## Operating Conditions

Operating Temperature Range
C82C284 . . . . . $0^oC$ to $+70^oC$
I82C284 . . . . . $-40^oC$ to $+85^oC$

Operating Supply Voltage . . . . . +4.5V to +5.5V
EFI Rise Time (from 0.8V to 3.2V) . . . . . 8ns (Max)
EFI Fall Time (from 3.2 to 0.8V) . . . . . 8ns (Max)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

## DC Electrical Specifications

$T_A = 0^oC$ to $+70^oC$ (CD82C284); $V_{CC} = 5V \pm 10\%$
$T_A = -40^oC$ to $+85^oC$ (ID82C284)

| SYMBOL | PARAMETER | MIN | MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|
| $V_{IL}$ | Input LOW Voltage | - | 0.8 | V | $V_{CC}$ = 4.5V |
| $V_{IH}$ | Input HIGH Voltage | 2.2 | - | V | $V_{CC}$ = 5.5V |
| $V_{IHC}$ | EFI, F/$\overline{C}$ Input HIGH Voltage | 3.2 | - | V | $V_{CC}$ = 5.5V |
| $V_{IHR}$ | $\overline{RES}$ HIGH Voltage | $V_{CC}$-0.8 | - | V | $V_{CC}$ = 5.5V |
| $V_{HYS}$ | $\overline{RES}$ Input Hysteresis | 0.5 | - | V | $V_{CC}$ = 5.5V |
| $V_{OL}$ | RESET, PCLK Output LOW Voltage | - | 0.4 | V | $I_{OL}$ = 5mA, $V_{CC}$ = 4.5V, Note 2 |
| $V_{OH}$ | RESET, PCLK Output HIGH Voltage | $V_{CC}$-0.4 | - | V | $I_{OH}$ = -1mA, $V_{CC}$ = 4.5V, Note 2 |
| $V_{OLR}$ | $\overline{READY}$ Output LOW Voltage | - | 0.4 | V | $I_{OL}$ = 10mA, $V_{CC}$ = 4.5V, Note 2 |
| $V_{OLC}$ | CLK Output LOW Voltage | - | 0.4 | V | $I_{OL}$ = 5mA, $V_{CC}$ = 4.5V, Note 2 |
| $V_{OHC}$ | CLK Output HIGH Voltage | $V_{CC}$-0.4 | - | V | $I_{OH}$ = -5mA, $V_{CC}$ = 4.5V, Note 2 |
| $I_{IL}$ | Input Leakage Current | -10 | 10 | µA | $V_{IN}$ = $V_{CC}$ or GND, $V_{CC}$ = 5.5V |
| $I_{CCOP}$ | Active Power Supply Current | - | 60 | mA | 82C284-12 (Note 1) |
| | | - | 48 | mA | 82C284-10 (Note 1) |

NOTES:

1. $I_{CCOP}$ measured at 10MHz for 82C284-10 and at 12.5MHz for the 82C284-12. $V_{IN}$ = GND or $V_{CC}$, $V_{CC}$ = 5.5V outputs unloaded.
2. Interchanging of force and sense conditions is permitted.

## AC Electrical Specifications

$T_A = 0^oC$ to $+70^oC$ (CD82C284); $V_{CC} = 5V \pm 10\%$
$T_A = -40^oC$ to $+85^oC$ (ID82C284)
AC Timings are Referenced to 0.8V and 2.0V Points of the Signals as Illustrated in Waveforms, Unless Otherwise Noted.

| SYMBOL | PARAMETER | 10MHz | | 12.5MHz | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | | |
| t1 | EFI LOW Time | 20 | - | 16 | - | ns | At $V_{CC}$/2 (Note 8) |
| t2 | EFI HIGH Time | 20 | - | 20 | - | ns | At $V_{CC}$/2 (Note 8) |
| 5A | Status Setup Time for Status Going Active | 20 | - | 18 | - | ns | |
| 5B | Status Setup Time for Status Going Inactive | 20 | - | 16 | - | ns | |

## AC Electrical Specifications

$T_A = 0^oC$ to $+70^oC$ (CD82C284); $V_{CC} = 5V \pm 10\%$ **(Continued)**
$T_A = -40^oC$ to $+85^oC$ (ID82C284)
AC Timings are Referenced to 0.8V and 2.0V Points of the Signals as Illustrated in Waveforms, Unless Otherwise Noted.

| SYMBOL | PARAMETER | 10MHz | | 12.5MHz | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | | |
| t6 | Status Hold Time | 1 | - | 1 | - | ns | |
| t7 | F/$\overline{C}$ Setup Time | 15 | - | 15 | - | | |
| t8 | F/$\overline{C}$ Hold Time | 15 | - | 15 | - | | |
| t9 | $\overline{SRDY}$ or $\overline{SRDYEN}$ Setup Time | 15 | - | 15 | - | ns | |
| t10 | $\overline{SRDY}$ or $\overline{SRDYEN}$ Hold Time | 2 | - | 2 | - | ns | |
| t11 | $\overline{ARDY}$ or $\overline{ARDYEN}$ Setup Time | 5 | - | 5 | - | ns | (Note 3) |
| t12 | $\overline{ARDY}$ or $\overline{ARDYEN}$ Hold Time | 30 | - | 25 | - | ns | (Note 3) |
| t13 | $\overline{RES}$ Setup Time | 20 | - | 18 | - | ns | (Notes 3, 7) |
| t14 | RES Hold Time | 10 | - | 8 | - | ns | (Notes 3, 7) |
| t16 | CLK Period | 50 | - | 40 | - | | |
| t17 | CLK LOW Time | 12 | - | 11 | - | ns | (Notes 2, 6) |
| t18 | CLK HIGH Time | 16 | - | 13 | - | ns | (Notes 2, 6) |
| t21 | $\overline{READY}$ Inactive Delay | 5 | - | 5 | - | ns | At 0.8V (Note 4), Test Condition 2 |
| t22 | $\overline{READY}$ Active Delay | - | 24 | - | 18 | ns | At 0.8V (Note 4) |
| t23 | PCLK Delay | - | 20 | - | 16 | ns | $C_L$ = 75pF, Test Condition 1 |
| t24 | RESET Delay | - | 27 | - | 26 | ns | $C_L$ = 75pF, Test Condition 3 |
| t25 | PCLK LOW Time | t16 -10 | - | t16 -10 | - | na | $C_L$ = 75pF (Note 5) |
| t26 | PCLK HIGH Time | t16 -10 | - | t16 -10 | - | ns | $C_L$= 75pF (Note 5) |

NOTES:

1. $V_{CC}$ = 4.5V and 5.5V unless otherwise specified. CLK loading: $C_L$ = 100pF.
2. With the internal crystal oscillator using recommended crystal and capacitive loading; or with the EFI input meeting specifications $t_1$ and $t_2$. The recommended crystal loading for CLK frequencies of 8MHz to 20MHz are 25pF from pin X1 to ground, and 15pF from pin X2 to ground; for CLK frequencies from 20MHz to 25MHz the recommended loading is 15pF from pin X1 to GND. These recommended values are +5pF and include all stray capacitance. Decouple $V_{CC}$ and GND as close to the 82C284 as possible.
3. This is an asynchronous input. This specification is given for testing purposes only, to assure recognition at a specific CLK edge.
4. The pull-up resistor value for the $\overline{READY}$ pin is 620Ω with the rated 150pF load.
5. $t_{16}$ refers to any allowable CLK period.
6. When using a crystal with the recommended capacitive loading, CLK output HIGH and LOW times are guaranteed to meet 80C286 requirements.
7. Measured from 1.0V on the CLK to 0.8V on the $\overline{RES}$ waveform for $\overline{RES}$ waveform for $\overline{RES}$ active and to 4.2V on the $\overline{RES}$ waveform for $\overline{RES}$ inactive.
8. Input test waveform characteristics: $V_{IL}$ = 0V, $V_{IH}$ = 4.5V.

**UNTESTED SPECIFICATIONS**

| SYMBOL | PARAMETER | 10MHz | | 12.5MHz | | UNITS | **CONDITIONS** (NOTE 1) |
|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | | |
| $C_{IN}$ | Input Capacitance | - | 10 | - | 10 | pF | FREQ = 1MHz, All measurements are referenced to device GND, $T_A = +25^oC$ |
| t15A | EFI HIGH to CLK LOW Delay | - | 30 | - | 25 | ns | (Note 2) |
| t15B | EFI LOW to CLK HIGH Delay | - | 35 | - | 30 | ns | (Note 3) |

**UNTESTED SPECIFICATIONS (Continued)**

| SYMBOL | PARAMETER | 10MHz | | 12.5MHz | | UNITS | CONDITIONS (NOTE 1) |
|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | | |
| t19 | CLK Rise Time | - | 8 | - | 8 | ns | 1.0V to 3.6V, $C_L$ = 100pF |
| t20 | CLK Fall Time | - | 8 | - | 8 | ns | 3.6V to 1.0V, $C_L$ = 100pF |
| t27 | X1 HIGH to CLK | - | 35 | - | 30 | ns | (Note 4) |

NOTES:

1. The parameters listed in this table are controlled via design or, process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
2. Measured from 3.2V on the EFI waveform to 1.0V on the CLK.
3. Measured from 0.8V on the EFI waveform to 3.6V on the CLK.
4. Measured from 3.6V on the X1 input to 3.6V on the CLK.

## AC Specifications

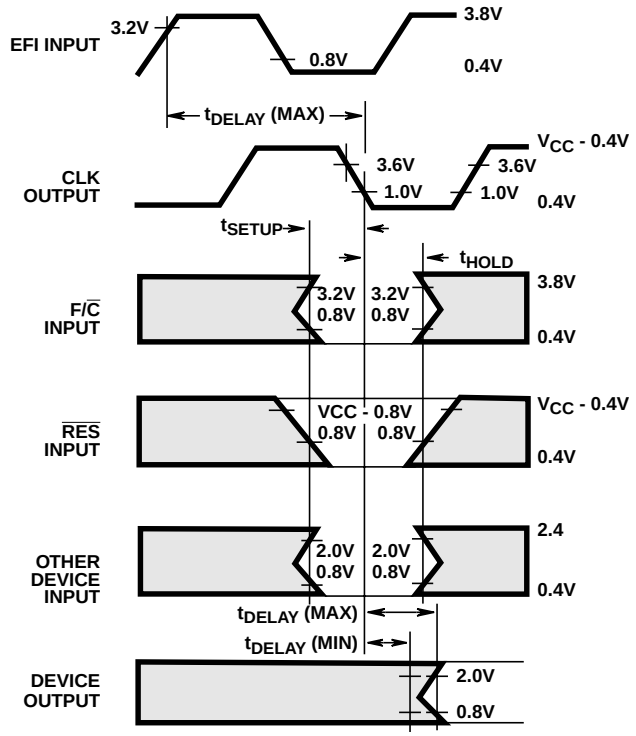



**FIGURE 7. A.C. DRIVE, SETUP, HOLD AND DELAY TIME MEASUREMENT POINTS**

## AC Test Condition

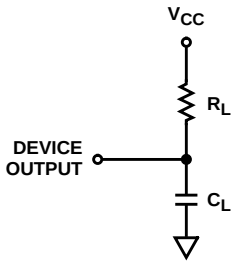
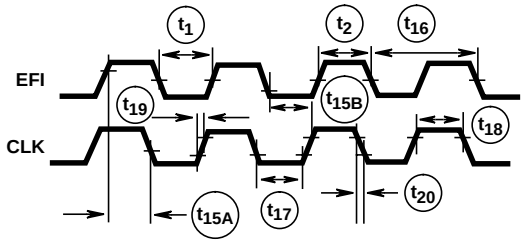



**FIGURE 8.**

| TEST CONDITION | $R_L$ | $C_L$ |
|---|---|---|
| 1 | 750Ω | 75pF |
| 2 | 620Ω | 150pF |
| 3 | ∞ | 75pF |

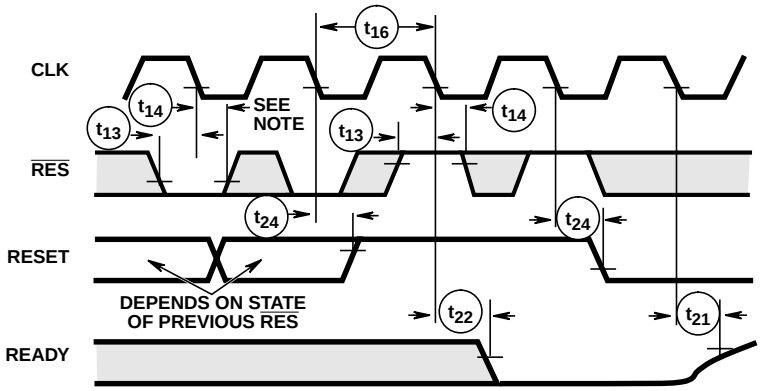
## Waveforms




NOTE:

1. The EFI input LOW and HIGH times as shown are required to guarantee the CLK LOW and HIGH times shown.

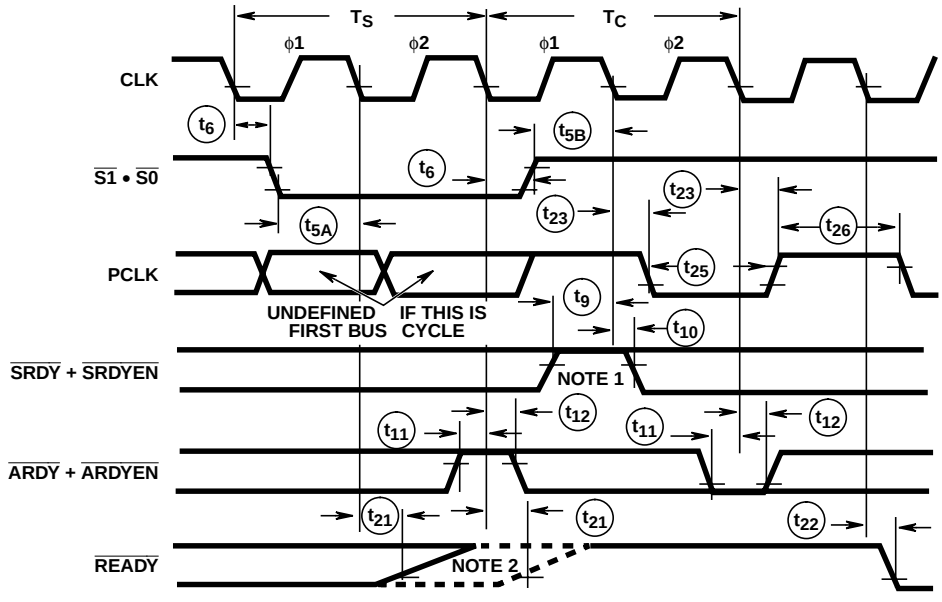
**FIGURE 9. CLK AS A FUNCTION OF EFI**




NOTE:

1. This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.

**FIGURE 10. RESET AND $\overline{\text{READY}}$ TIMING AS A FUNCTION OF RES WITH $\overline{\text{S1}}$, $\overline{\text{S0}}$, $\overline{\text{ARDY}}$ + $\overline{\text{ARDYEN}}$, AND $\overline{\text{SRDY}}$ + $\overline{\text{SRDYEN}}$ HIGH**

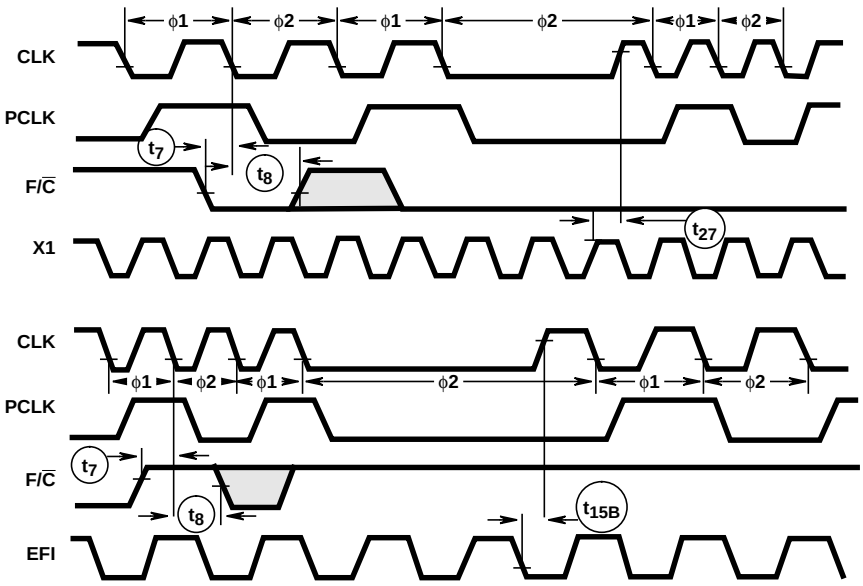



NOTES:

1. This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.
2. If $\overline{\text{SRDY}}$ + $\overline{\text{SRDYEN}}$ or $\overline{\text{ARDYEN}}$ are active before and/or during the first bus cycle after RESET, $\overline{\text{READY}}$ may not be deasserted until the falling edge of $\phi 2$ of $T_S$.

**FIGURE 11. $\overline{\text{READY}}$ AND PCLK TIMING WITH $\overline{\text{RES}}$ HIGH**

## Waveforms (Continued)




NOTE:

1. This is an asynchronous input. The setup and hold times are required to guarantee the response shown.

**FIGURE 12. CLK AS A FUNCTION OF F/$\overline{C}$, PCLK, X1, AND EFI DURING DYNAMIC FREQUENCY SWITCHING**



## Sales Office Headquarters

**NORTH AMERICA**
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

**EUROPE**
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

**ASIA**
Intersil (Taiwan) Ltd.
Taiwan Limited
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029