

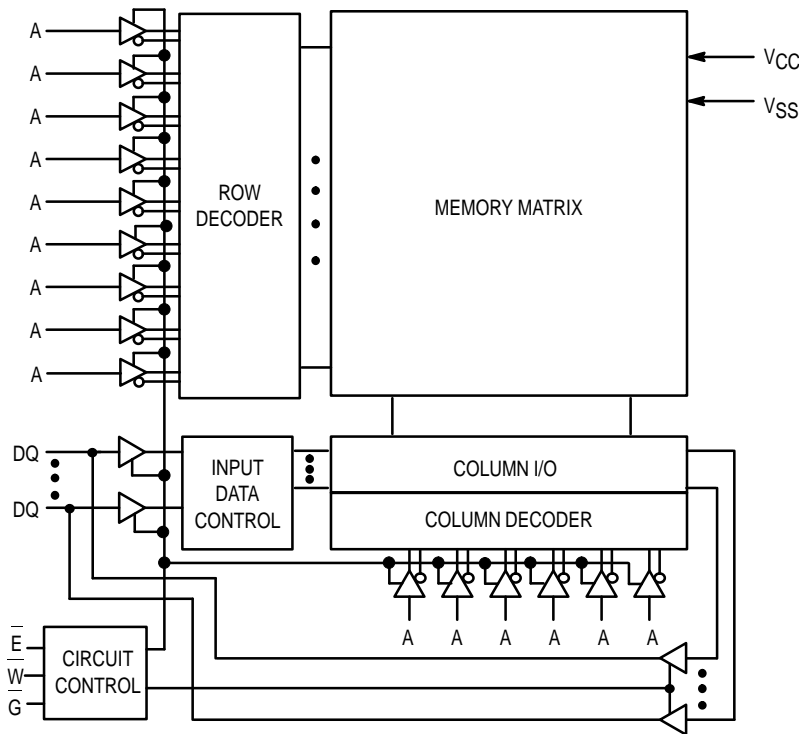
# 32K x 8 Bit Fast Static RAM

The MCM6206BA is a 262,144 bit static random access memory organized as 32,768 words of 8 bits. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

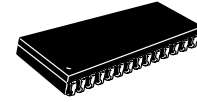
This device meets JEDEC standards for functionality and pinout, and is available in plastic small-outline J-leaded packages.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strokes Necessary
- Fast Access Times: 12/15/20/25 ns
- Equal Address and Chip Enable Access Times
- Output Enable (G) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems
- Low Power Operation: 125 – 140 mA Maximum AC
- Fully TTL Compatible — Three State Output

## BLOCK DIAGRAM



## MCM6206BA



**J PACKAGE**  
**300 MIL SOJ**  
**CASE**  
**810B-03**

## PIN ASSIGNMENT

A	1	28	V <sub>CC</sub>
A	2	27	$\overline{W}$
A	3	26	A
A	4	25	A
A	5	24	A
A	6	23	$\overline{A}$
A	7	22	$\overline{G}$
A	8	21	A
A	9	20	$\overline{E}$
A	10	19	DQ
DQ	11	18	DQ
DQ	12	17	DQ
DQ	13	16	DQ
V <sub>SS</sub>	14	15	DQ

## PIN NAMES

A	.....	Address Input
DQ	.....	Data Input/Data Output
$\overline{W}$	.....	Write Enable
$\overline{G}$	.....	Output Enable
$\overline{E}$	.....	Chip Enable
V <sub>CC</sub>	.....	Power Supply (+ 5 V)
V <sub>SS</sub>	.....	Ground

**TRUTH TABLE** (X = Don't Care)

E	G	W	Mode	V <sub>CC</sub> Current	Output	Cycle
H	X	X	Not Selected	I <sub>SB1</sub> , I <sub>SB2</sub>	High-Z	–
L	H	H	Output Disabled	I <sub>CCA</sub>	High-Z	–
L	L	H	Read	I <sub>CCA</sub>	D <sub>out</sub>	Read Cycle
L	X	L	Write	I <sub>CCA</sub>	High-Z	Write Cycle

**ABSOLUTE MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Power Supply Voltage	V <sub>CC</sub>	– 0.5 to + 7.0	V
Voltage Relative to V <sub>SS</sub> For Any Pin Except V <sub>CC</sub>	V <sub>in</sub> , V <sub>out</sub>	– 0.5 to V <sub>CC</sub> + 0.5	V
Output Current	I <sub>out</sub>	± 20	mA
Power Dissipation	P <sub>D</sub>	1.0	W
Temperature Under Bias	T <sub>bias</sub>	– 10 to + 85	°C
Operating Temperature	T <sub>A</sub>	0 to + 70	°C
Storage Temperature—Plastic	T <sub>stg</sub>	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

**DC OPERATING CONDITIONS AND CHARACTERISTICS**

(V<sub>CC</sub> = 5.0 V ±10%, T<sub>A</sub> = 0 to 70°C, Unless Otherwise Noted)

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V <sub>CC</sub>	4.5	5.0	5.5	V
Input High Voltage	V <sub>IH</sub>	2.2	—	V <sub>CC</sub> + 0.3**	V
Input Low Voltage	V <sub>IL</sub>	– 0.5*	—	0.8	V

\* V<sub>IL</sub> (min) = – 0.5 V dc; V<sub>IL</sub> (min) = – 2.0 V ac (pulse width ≤ 20 ns)

\*\* V<sub>IH</sub> (max) = V<sub>CC</sub> + 0.3 V dc; V<sub>IH</sub> (max) = V<sub>CC</sub> + 2.0 V ac (pulse width ≤ 20 ns)

**DC CHARACTERISTICS**

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V <sub>in</sub> = 0 to V <sub>CC</sub> )	I <sub>kg(I)</sub>	—	± 1	μA
Output Leakage Current (E = V <sub>IH</sub> or G = V <sub>IH</sub> , V <sub>out</sub> = 0 to V <sub>CC</sub> )	I <sub>kg(O)</sub>	—	± 1	μA
Output High Voltage (I <sub>OH</sub> = – 4.0 mA)	V <sub>OH</sub>	2.4	—	V
Output Low Voltage (I <sub>OL</sub> = 8.0 mA)	V <sub>OL</sub>	—	0.4	V

**POWER SUPPLY CURRENTS**

Parameter	Symbol	– 12	– 15	– 20	– 25	Unit
AC Active Supply Current (I <sub>out</sub> = 0 mA, V <sub>CC</sub> = Max, f = f <sub>max</sub> )	I <sub>CCA</sub>	140	135	130	125	mA
AC Standby Current (E = V <sub>IH</sub> , V <sub>CC</sub> = Max, f = f <sub>max</sub> )	I <sub>SB1</sub>	40	35	35	30	mA
CMOS Standby Current (V <sub>CC</sub> = Max, f = 0 MHz, E ≥ V <sub>CC</sub> – 0.2 V, V <sub>in</sub> ≤ V <sub>SS</sub> + 0.2 V, or ≥ V <sub>CC</sub> – 0.2 V)	I <sub>SB2</sub>	10	10	10	10	mA

**CAPACITANCE** (f = 1 MHz, dV = 3 V, T<sub>A</sub> = 25°C, Periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Address Input Capacitance	C <sub>in</sub>	6	pF
Control Pin Input Capacitance (E, G, W)	C <sub>in</sub>	8	pF
I/O Capacitance	C <sub>I/O</sub>	8	pF

## AC OPERATING CONDITIONS AND CHARACTERISTICS

( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $T_A = 0\text{ to } +70^\circ\text{C}$ , Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V  
 Input Pulse Levels ..... 0 to 3.0 V  
 Input Rise/Fall Time ..... 5 ns

Output Timing Measurement Reference Level ..... 1.5 V  
 Output Load ..... Figure 1a Unless Otherwise Noted

### READ CYCLE (See Note 1)

Parameter	Symbol	- 12		- 15		- 20		- 25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	$t_{AVAV}$	12	—	15	—	20	—	25	—	ns	2
Address Access Time	$t_{AVQV}$	—	12	—	15	—	20	—	25	ns	
Enable Access Time	$t_{ELQV}$	—	12	—	15	—	20	—	25	ns	3
Output Enable Access Time	$t_{GLQV}$	—	6	—	8	—	10	—	12	ns	
Output Hold from Address Change	$t_{AXQX}$	3	—	3	—	3	—	3	—	ns	4,5,6
Enable Low to Output Active	$t_{ELQX}$	4	—	4	—	4	—	4	—	ns	4,5,6
Enable High to Output High-Z	$t_{EHQZ}$	—	7	—	8	—	9	—	10	ns	4,5,6
Output Enable Low to Output Active	$t_{GLQX}$	0	—	0	—	0	—	0	—	ns	4,5,6
Output Enable High to Output High-Z	$t_{GHQZ}$	—	6	—	7	—	8	—	10	ns	4,5,6
Power Up Time	$t_{ELICCH}$	0	—	0	—	0	—	0	—	ns	
Power Down Time	$t_{EHICCL}$	—	12	—	15	—	20	—	25	ns	

#### NOTES:

1. W is high for read cycle.
2. All timings are referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with E going low.
4. At any given voltage and temperature,  $t_{EHQZ}$  (max) is less than  $t_{ELQX}$  (min), and  $t_{GHQZ}$  (max) is less than  $t_{GLQX}$  (min), both for a given device and from device to device.
5. Transition is measured  $\pm 500\text{ mV}$  from steady-state voltage with load of Figure 1b.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ( $E = V_{IL}$ ,  $G = V_{IL}$ ).

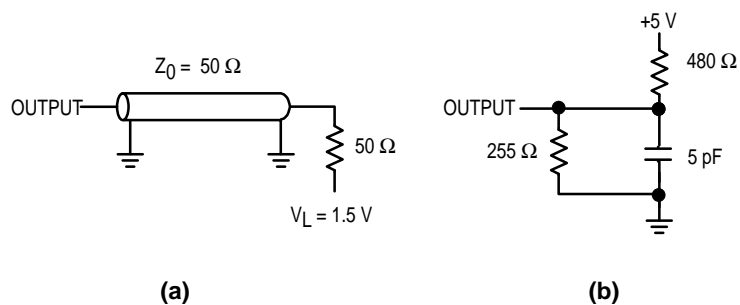
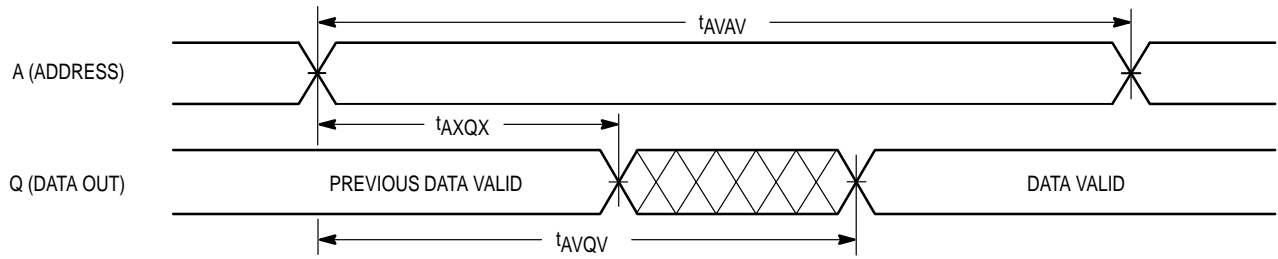


Figure 1. AC Test Loads

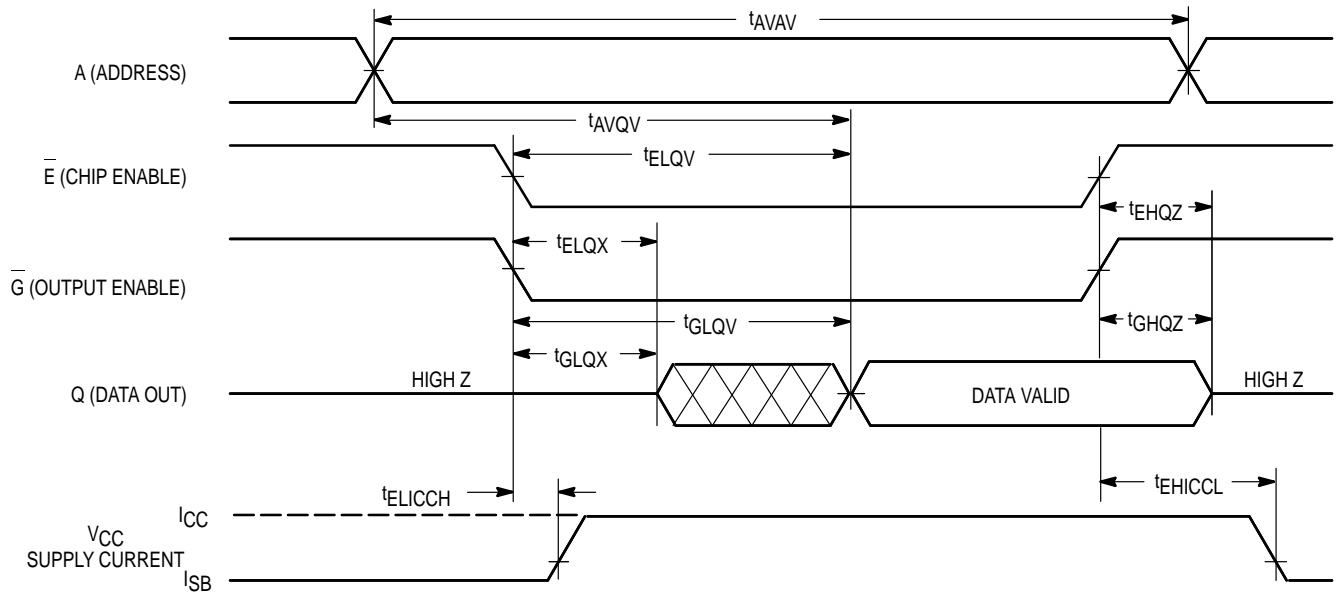
### TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

**READ CYCLE 1 (See Note 7)**



**READ CYCLE 2 (See Note 3)**



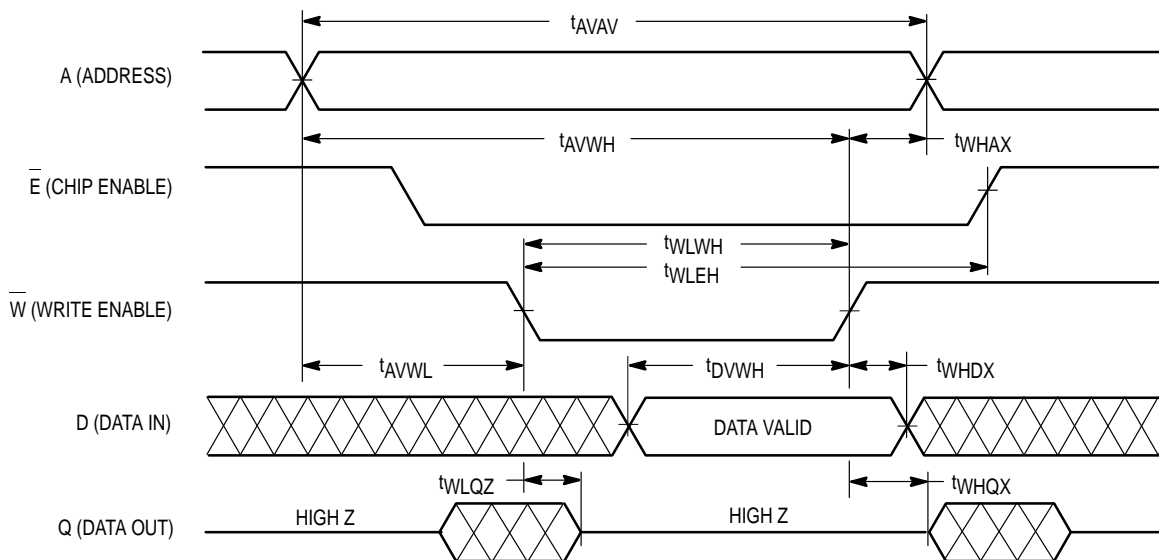
**WRITE CYCLE 1** ( $\overline{W}$  Controlled, See Notes 1 and 2)

Parameter	Symbol	- 12		- 15		- 20		- 25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	$t_{AVAV}$	12	—	15	—	20	—	25	—	ns	3
Address Setup Time	$t_{AVWL}$	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	$t_{AVWH}$	10	—	12	—	15	—	20	—	ns	
Write Pulse Width	$t_{WLWH}$ , $t_{WLEH}$	10	—	12	—	15	—	20	—	ns	
Write Pulse Width, G High	$t_{WLWH}$ , $t_{WLEH}$	10	—	10	—	12	—	15	—	ns	4
Data Valid to End of Write	$t_{DVWH}$	6	—	7	—	8	—	10	—	ns	
Data Hold Time	$t_{WHDX}$	0	—	0	—	0	—	0	—	ns	
Write Low to Output High-Z	$t_{WLQZ}$	—	6	—	7	—	8	—	10	ns	5,6,7
Write High to Output Active	$t_{WHQX}$	2	—	2	—	2	—	2	—	ns	5,6,7
Write Recovery Time	$t_{WHAX}$	0	—	0	—	0	—	0	—	ns	

**NOTES:**

1. A write occurs during the overlap of  $\overline{E}_{low}$  and  $\overline{W}$  low.
2. If G goes low coincident with or after W goes low, the output will remain in a high impedance state.
3. All timings are referenced from the last valid address to the first transitioning address.
4. If  $G \geq V_{IH}$ , the output will remain in a high impedance state.
5. At any given voltage and temperature,  $t_{WLQZ}$  (max) is less than  $t_{WHQX}$  (min), both for a given device and from device to device.
6. Transition is measured  $\pm 500$  mV from steady-state voltage with load of Figure 1b.
7. This parameter is sampled and not 100% tested.

**WRITE CYCLE 1** ( $\overline{W}$  Controlled, See Notes 1 and 2)



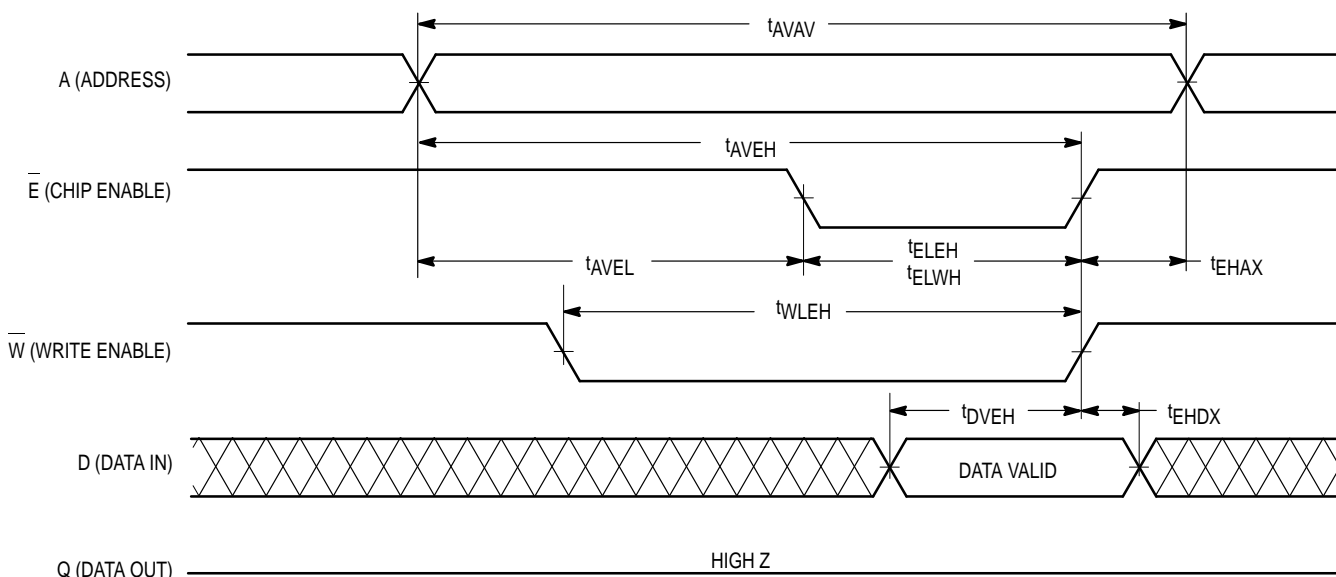
**WRITE CYCLE 2** ( $\bar{E}$  Controlled, See Note 1)

Parameter	Symbol	- 12		- 15		- 20		- 25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	$t_{AVAV}$	12	—	15	—	20	—	25	—	ns	
Address Setup Time	$t_{AVEL}$	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	$t_{AVEH}$	10	—	12	—	15	—	20	—	ns	
Enable to End of Write	$t_{ELEH}$ , $t_{ELWH}$	9	—	10	—	12	—	15	—	ns	3,4
Data Valid to End of Write	$t_{DVEH}$	6	—	7	—	8	—	10	—	ns	
Data Hold Time	$t_{EHDX}$	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	$t_{EHAX}$	0	—	0	—	0	—	0	—	ns	

**NOTES:**

1. A write occurs during the overlap of  $\bar{E}$  low and  $\bar{W}$  low.
2. All timings are referenced from the last valid address to the first transitioning address.
3. If  $\bar{E}$  goes low coincident with or after  $\bar{W}$  goes low, the output will remain in a high impedance state.
4. If  $\bar{E}$  goes high coincident with or before  $\bar{W}$  goes high, the output will remain in a high impedance state.

**WRITE CYCLE 2** ( $\bar{E}$  Controlled, See Note 1)



**ORDERING INFORMATION**  
(Order by Full Part Number)

**MCM 6206BA EJ XX X**

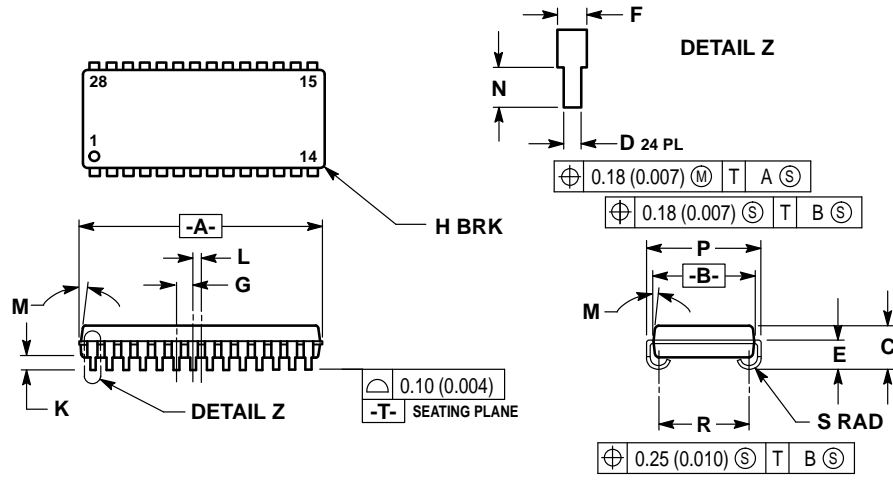
Motorola Memory Prefix — **MCM**  
Part Number — **6206BA**

**EJ** — Package (J = 300 mil SOJ, E = Evolutionary Pinout)  
**XX** — Speed (12 = 12 ns, 15 = 15 ns, 20 = 20 ns, 25 = 25 ns)  
**X** — Shipping Method (R = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6206BAEJ12 MCM6206BAEJ12R  
MCM6206BAEJ15 MCM6206BAEJ15R  
MCM6206BAEJ20 MCM6206BAEJ20R  
MCM6206BAEJ25 MCM6206BAEJ25R

# PACKAGE DIMENSIONS


CASE 810B-03  
300 MIL SOJ  
28 LEAD



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
3. CONTROLLING DIMENSION: INCH.
4. DIM R TO BE DETERMINED AT DATUM -T.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.720	0.730	18.29	18.54
B	0.295	0.305	7.50	7.74
C	0.128	0.148	3.26	3.75
D	0.015	0.020	0.39	0.50
E	0.088	0.098	2.24	2.48
F	0.026	0.032	0.67	0.81
G	0.050 BSC		1.27 BSC	
H	—	0.020	—	0.50
K	0.035	0.045	0.89	1.14
L	0.025 BSC		0.64 BSC	
M	0°	10°	0°	10°
N	0.030	0.045	0.76	1.14
P	0.330	0.340	8.38	8.64
R	0.260	0.270	6.60	6.86
S	0.030	0.040	0.77	1.01

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MCM6206BA/D

