

128K x 8 Bit Static Random Access Memory

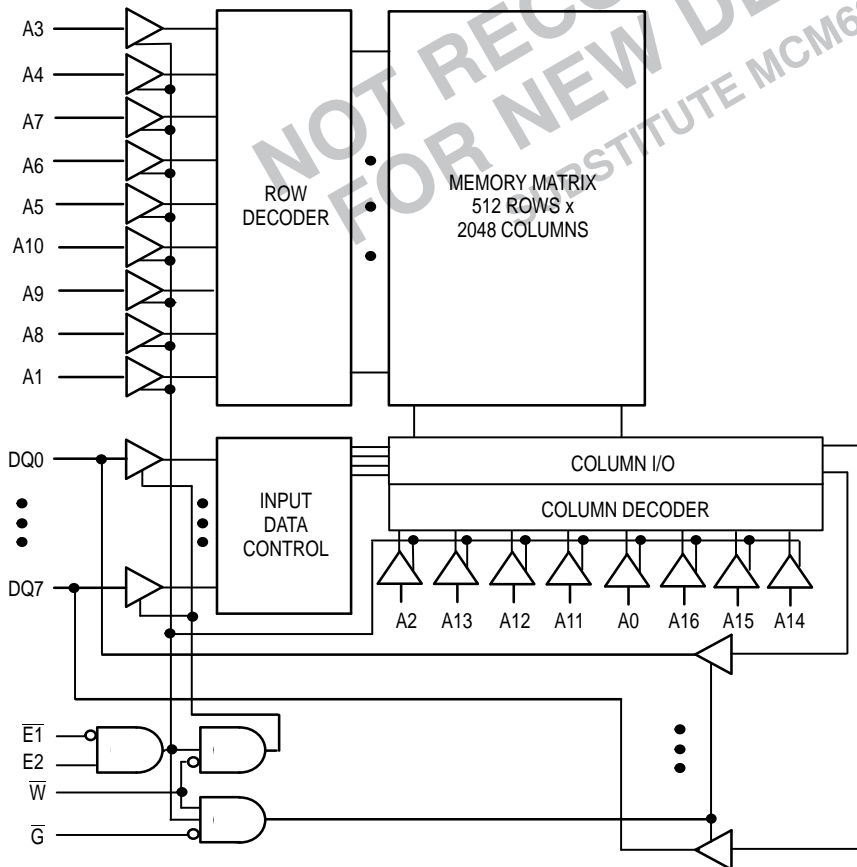
The MCM6226A is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits, fabricated using high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6226A is equipped with both chip enable ($\overline{E1}$ and E2) and output enable (\overline{G}) pins, allowing for greater system flexibility and eliminating bus contention problems.

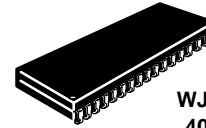
The MCM6226A is available in 400 mil, 32 lead surface-mount SOJ packages.

- Single 5 V \pm 10% Power Supply
- Fast Access Times: 20, 25, 35, and 45 ns
- Equal Address and Chip Enable Access Times
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Low Power Operation: 180/160/150/140 mA Maximum, Active AC

BLOCK DIAGRAM



MCM6226A



WJ PACKAGE
400 MIL SOJ
CASE 857A-02

PIN ASSIGNMENT

| | | | |
|-----------------|----|----|-----------------|
| NC | 1 | 32 | V _{CC} |
| A0 | 2 | 31 | A16 |
| A1 | 3 | 30 | E2 |
| A2 | 4 | 29 | \overline{W} |
| A3 | 5 | 28 | A15 |
| A4 | 6 | 27 | A14 |
| A5 | 7 | 26 | A13 |
| A6 | 8 | 25 | A12 |
| A7 | 9 | 24 | \overline{G} |
| A8 | 10 | 23 | A11 |
| A9 | 11 | 22 | $\overline{E1}$ |
| A10 | 12 | 21 | DQ7 |
| DQ0 | 13 | 20 | DQ6 |
| DQ1 | 14 | 19 | DQ5 |
| DQ2 | 15 | 18 | DQ4 |
| V _{SS} | 16 | 17 | DQ3 |

PIN NAMES

| | |
|----------------------|---------------------|
| A0 – A16 | Address Inputs |
| \overline{W} | Write Enable |
| \overline{G} | Output Enable |
| $\overline{E1}$, E2 | Chip Enables |
| DQ0 – DQ7 | Data Inputs/Outputs |
| NC | No Connection |
| V _{CC} | + 5 V Power Supply |
| V _{SS} | Ground |

TRUTH TABLE

| E1 | E2 | \bar{G} | W | Mode | I/O Pin | Cycle | Current |
|----|----|-----------|---|-----------------|------------------|-------|-------------------------------------|
| H | X | X | X | Not Selected | High-Z | — | I _{SB1} , I _{SB2} |
| X | L | X | X | Not Selected | High-Z | — | I _{SB1} , I _{SB2} |
| L | H | H | H | Output Disabled | High-Z | — | I _{CCA} |
| L | H | L | H | Read | D _{out} | Read | I _{CCA} |
| L | H | X | L | Write | D _{in} | Write | I _{CCA} |

H = High, L = Low, X = Don't Care

ABSOLUTE MAXIMUM RATINGS (See Note)

| Rating | Symbol | Value | Unit |
|--|------------------------------------|-------------------------------|------|
| Power Supply Voltage Relative to V _{SS} | V _{CC} | -0.5 to 7.0 | V |
| Voltage Relative to V _{SS} for Any Pin Except V _{CC} | V _{in} , V _{out} | -0.5 to V _{CC} + 0.5 | V |
| Output Current (per I/O) | I _{out} | ± 20 | mA |
| Power Dissipation | P _D | 1.1 | W |
| Temperature Under Bias | T _{bias} | -10 to +85 | °C |
| Operating Temperature | T _A | 0 to +70 | °C |
| Storage Temperature | T _{stg} | -55 to +150 | °C |

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min | Max | Unit |
|--|-----------------|-------|-------------------------|------|
| Supply Voltage (Operating Voltage Range) | V _{CC} | 4.5 | 5.5 | V |
| Input High Voltage | V _{IH} | 2.2 | V _{CC} + 0.3** | V |
| Input Low Voltage | V _{IL} | -0.5* | 0.8 | V |

* V_{IL} (min) = -0.5 V dc; V_{IL} (min) = -2.0 V ac (pulse width ≤ 20 ns).

** V_{IH} (max) = V_{CC} to 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS AND SUPPLY CURRENTS

| Parameter | Symbol | Min | Typ** | Max | Unit |
|---|---------------------|-----|--|-----|------|
| Input Leakage Current (All Inputs, V _{in} = 0 to V _{CC}) | I _{lkg(I)} | — | — | ± 1 | μA |
| Output Leakage Current ($\bar{E}^* = V_{IH}$, V _{out} = 0 to V _{CC}) | I _{lkg(O)} | — | — | ± 1 | μA |
| AC Active Supply Current (I _{out} = 0 mA, V _{CC} = max) | I _{CCA} | — | — | — | mA |
| | | | MCM6226A-20: t _{AVAV} = 20 ns | 150 | 180 |
| | | | MCM6226A-25: t _{AVAV} = 25 ns | 135 | 160 |
| | | | MCM6226A-35: t _{AVAV} = 35 ns | 125 | 150 |
| | | | MCM6226A-45: t _{AVAV} = 45 ns | 120 | 140 |
| AC Standby Current (V _{CC} = max, $\bar{E}^* = V_{IH}$, f = f _{max}) | I _{SB1} | — | 7 | 20 | mA |
| CMOS Standby Current ($\bar{E}^* \geq V_{CC} - 0.2$ V, V _{in} ≤ V _{SS} + 0.2 V or ≥ V _{CC} - 0.2 V, V _{CC} = max, f = 0 MHz) | I _{SB2} | — | 4 | 15 | mA |
| Output Low Voltage (I _{OL} = +8.0 mA) | V _{OL} | — | — | 0.4 | V |
| Output High Voltage (I _{OH} = -4.0 mA) | V _{OH} | 2.4 | — | — | V |

* $\bar{E}1$ and E2 are represented by \bar{E} in this data sheet. E2 is of opposite polarity to $\bar{E}1$.

**Typical values are measured at 25°C, V_{CC} = 5 V.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

| Characteristic | Symbol | Typ | Max | Unit | |
|-------------------|---|------------------|-----|------|----|
| Input Capacitance | All Inputs Except Clocks and DQ | C _{in} | 4 | 6 | pF |
| | $\overline{E1}$, E2, \overline{G} , and \overline{W} | C _{ck} | 5 | 8 | pF |
| I/O Capacitance | DQ | C _{I/O} | 5 | 8 | pF |

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels 0 to 3.0 V Output Timing Measurement Reference Level 1.5 V
 Input Rise/Fall Time 2 ns Output Load See Figure 1A
 Input Timing Measurement Reference Level 1.5 V

READ CYCLE TIMING (See Notes 1, 2, and 3)

| Parameter | Symbol | 6226A-20 | | 6226A-25 | | 6226A-35 | | 6226A-45 | | Unit | Notes |
|-------------------------------------|---------------------|----------|-----|----------|-----|----------|-----|----------|-----|------|---------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| Read Cycle Time | t _{AVAV} | 20 | — | 25 | — | 35 | — | 45 | — | ns | 4 |
| Address Access Time | t _{AVQV} | — | 20 | — | 25 | — | 35 | — | 45 | ns | |
| Enable Access Time | t _{ELQV} | — | 20 | — | 25 | — | 35 | — | 45 | ns | 5 |
| Output Enable Access Time | t _{GLQV} | — | 8 | — | 10 | — | 15 | — | 15 | ns | |
| Output Hold from Address Change | t _{AXQX} | 5 | — | 5 | — | 5 | — | 5 | — | ns | |
| Enable Low to Output Active | t _{ELQX} | 5 | — | 5 | — | 5 | — | 5 | — | ns | 6, 7, 8 |
| Output Enable Low to Output Active | t _{GLQX} | 0 | — | 0 | — | 0 | — | 0 | — | ns | 6, 7, 8 |
| Enable High to Output High-Z | t _{EHQZ} | 0 | 9 | 0 | 10 | 0 | 12 | 0 | 15 | ns | 6, 7, 8 |
| Output Enable High to Output High-Z | t _{GHQZ} | 0 | 9 | 0 | 10 | 0 | 12 | 0 | 15 | ns | 6, 7, 8 |
| Power Up Time | t _{ELICCH} | 0 | — | 0 | — | 0 | — | 0 | — | ns | |
| Power Down Time | t _{EHICCL} | — | 20 | — | 25 | — | 35 | — | 45 | ns | |

NOTES:

- \overline{W} is high for read cycle.
- Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
- $\overline{E1}$ and E2 are represented by \overline{E} in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
- All timings are referenced from the last valid address to the first transitioning address.
- Addresses valid prior to or coincident with \overline{E} going low.
- At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
- Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
- This parameter is sampled and not 100% tested.
- Device is continuously selected ($\overline{E} \leq V_{IL}$, $\overline{G} \leq V_{IL}$).

AC TEST LOADS

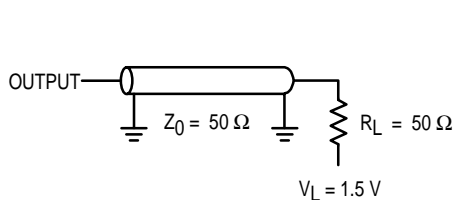


Figure 1A

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

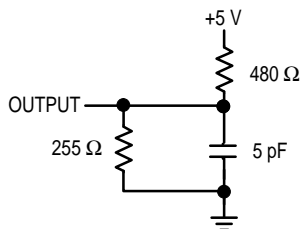
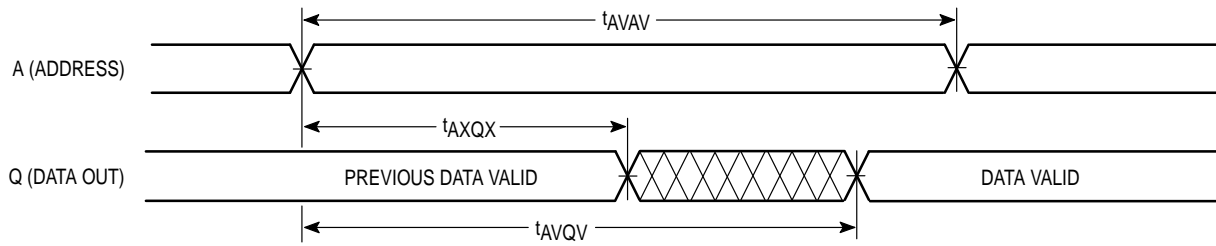
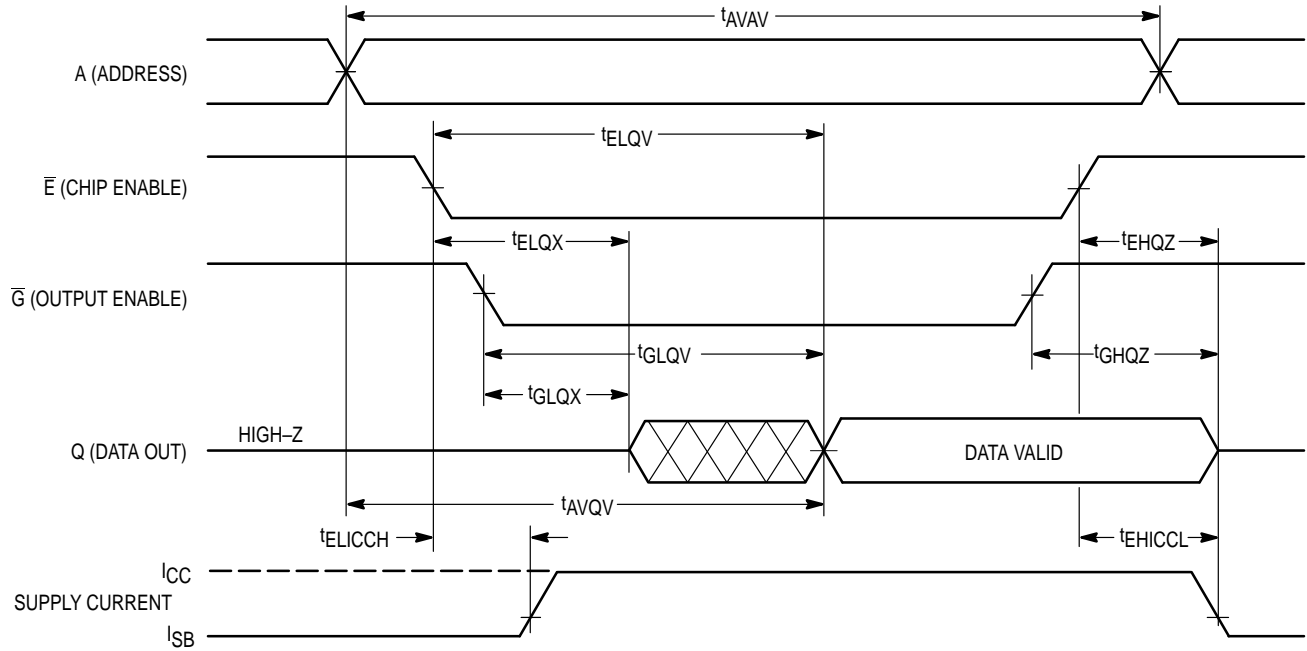


Figure 1B

READ CYCLE 1 (See Notes 1, 2, 3, and 9)



READ CYCLE 2 (See Notes 3 and 5)

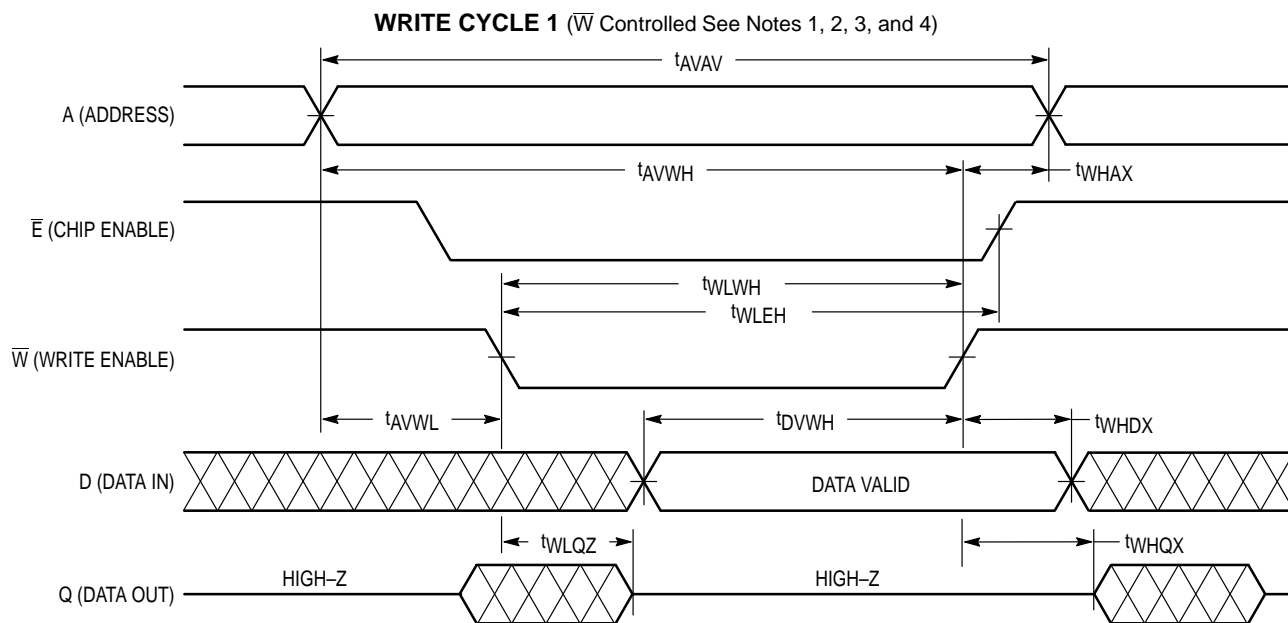


WRITE CYCLE 1 (\overline{W} Controlled, See Notes 1, 2, 3, and 4)

| Parameter | Symbol | 6226A-20 | | 6226A-25 | | 6226A-35 | | 6226A-45 | | Unit | Notes |
|-------------------------------|----------------------------|----------|-----|----------|-----|----------|-----|----------|-----|------|---------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| Write Cycle Time | t_{AVAV} | 20 | — | 25 | — | 35 | — | 45 | — | ns | 5 |
| Address Setup Time | t_{AVWL} | 0 | — | 0 | — | 0 | — | 0 | — | ns | |
| Address Valid to End of Write | t_{AVWH} | 15 | — | 17 | — | 20 | — | 25 | — | ns | |
| Write Pulse Width | t_{WLWH} , t_{WLEH} | 15 | — | 17 | — | 20 | — | 25 | — | ns | |
| Data Valid to End of Write | t_{DVWH} | 10 | — | 10 | — | 15 | — | 20 | — | ns | |
| Data Hold Time | t_{WHDX} | 0 | — | 0 | — | 0 | — | 0 | — | ns | |
| Write Low to Data High-Z | t_{WLQZ} | 0 | 9 | 0 | 10 | 0 | 15 | 0 | 20 | ns | 6, 7, 8 |
| Write High to Output Active | t_{WHQX} | 5 | — | 5 | — | 5 | — | 5 | — | ns | 6, 7, 8 |
| Write Recovery Time | t_{WHAX} | 0 | — | 0 | — | 0 | — | 0 | — | ns | |

NOTES:

1. A write occurs during the overlap of \overline{E} low and \overline{W} low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ and $E2$ are represented by \overline{E} in this data sheet. $E2$ is of opposite polarity to $\overline{E1}$.
4. If \overline{G} goes low coincident with or after \overline{W} goes low, the output will remain in a high-impedance state.
5. All timings are referenced from the last valid address to the first transitioning address.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.



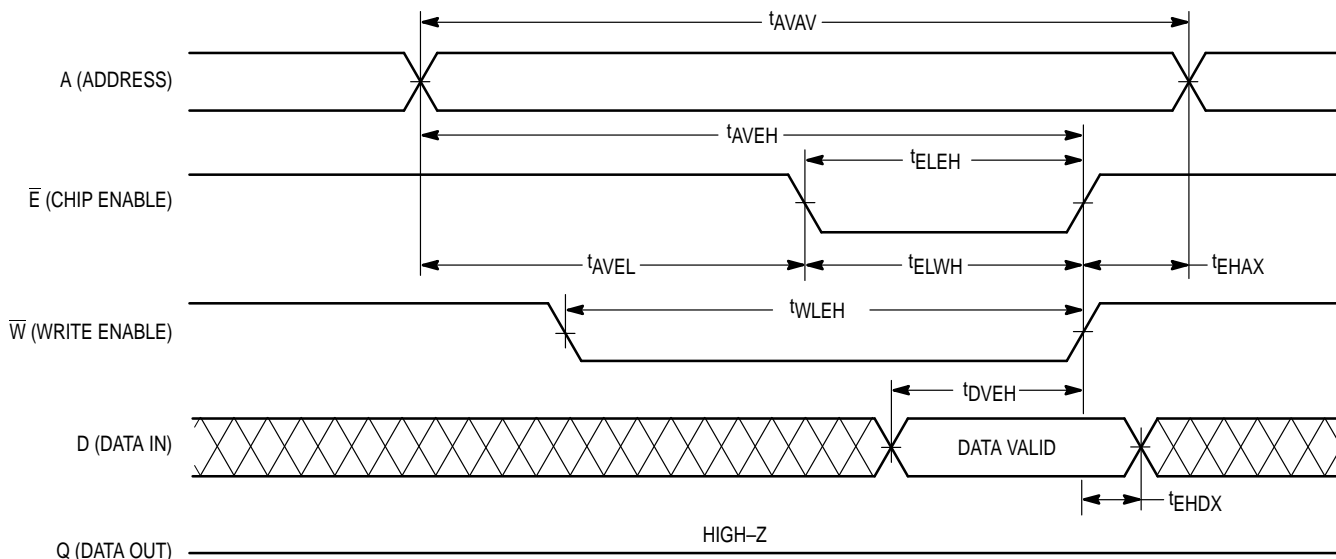
WRITE CYCLE 2 (\bar{E} Controlled, See Notes 1, 2, 3, and 4)

| Parameter | Symbol | 6226A-20 | | 6226A-25 | | 6226A-35 | | 6226A-45 | | Unit | Notes |
|-------------------------------|----------------------------|----------|-----|----------|-----|----------|-----|----------|-----|------|-------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| Write Cycle Time | t_{AVAV} | 20 | — | 25 | — | 35 | — | 45 | — | ns | 5 |
| Address Setup Time | t_{AVEL} | 0 | — | 0 | — | 0 | — | 0 | — | ns | |
| Address Valid to End of Write | t_{AVEH} | 15 | — | 17 | — | 20 | — | 25 | — | ns | |
| Enable to End of Write | t_{ELEH} , t_{ELWH} | 15 | — | 17 | — | 20 | — | 25 | — | ns | 6, 7 |
| Write Pulse Width | t_{WLEH} | 15 | — | 17 | — | 20 | — | 25 | — | ns | |
| Data Valid to End of Write | t_{DVEH} | 10 | — | 10 | — | 15 | — | 20 | — | ns | |
| Data Hold Time | t_{EHDX} | 0 | — | 0 | — | 0 | — | 0 | — | ns | |
| Write Recovery Time | t_{EHAX} | 0 | — | 0 | — | 0 | — | 0 | — | ns | |

NOTES:

1. A write occurs during the overlap of \bar{E} low and \bar{W} low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\bar{E}1$ and $E2$ are represented by \bar{E} in this data sheet. $E2$ is of opposite polarity to $\bar{E}1$.
4. If \bar{G} goes low coincident with or after \bar{W} goes low, the output will remain in a high-impedance state.
5. All timings are referenced from the last valid address to the first transitioning address.
6. If \bar{E} goes low coincident with or after \bar{W} goes low, the output will remain in a high-impedance state.
7. If \bar{E} goes high coincident with or before \bar{W} goes high, the output will remain in a high-impedance state.

WRITE CYCLE 2 (\bar{E} Controlled See Notes 1, 2, 3, and 4)



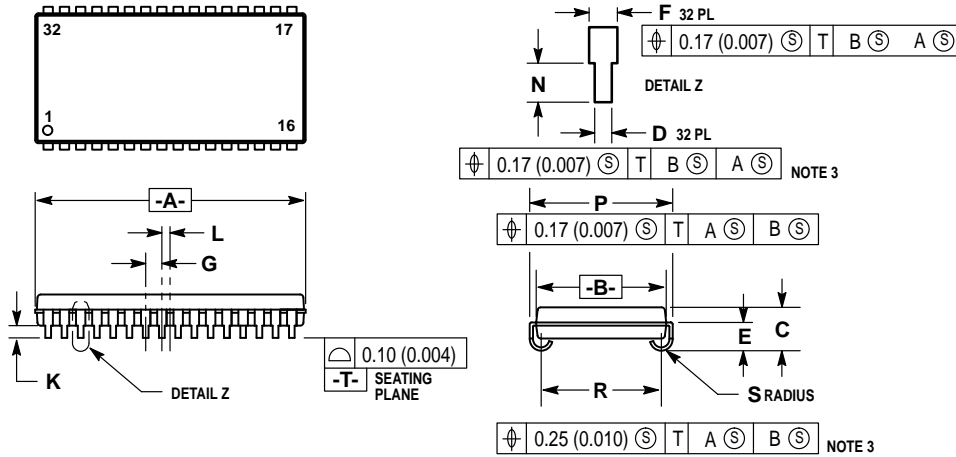
ORDERING INFORMATION
(Order by Full Part Number)

MCM **6226A** **WJ** **XX** **XX**
 Motorola Memory Prefix _____
 Part Number _____
 Shipping Method (R2 = Tape and Reel, Blank = Rails)
 Speed (20 = 20 ns, 25 = 25 ns, 35 = 35 ns, 45 = 45 ns)
 Package (WJ = 400 mil SOJ)

Full Part Numbers — MCM6226AWJ20 MCM6226AWJ20R2
 MCM6226AWJ25 MCM6226AWJ25R2
 MCM6226AWJ35 MCM6226AWJ35R2
 MCM6226AWJ45 MCM6226AWJ45R2


PACKAGE DIMENSIONS

32 LEAD 400 MIL SOJ CASE 857A-02



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. TO BE DETERMINED AT PLANE -T-.
 4. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 5. DIMENSION A & B INCLUDE MOLD MISMATCH AND ARE DETERMINED AT THE PARTING LINE.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 20.83 | 21.08 | 0.820 | 0.830 |
| B | 10.03 | 10.29 | 0.395 | 0.405 |
| C | 3.26 | 3.75 | 0.128 | 0.148 |
| D | 0.41 | 0.50 | 0.016 | 0.020 |
| E | 2.24 | 2.48 | 0.088 | 0.098 |
| F | 0.67 | 0.81 | 0.026 | 0.032 |
| G | 1.27 BSC | | 0.050 BSC | |
| K | 0.89 | 1.14 | 0.035 | 0.045 |
| L | 0.64 BSC | | 0.025 BSC | |
| N | 0.76 | 1.14 | 0.030 | 0.045 |
| P | 11.05 | 11.30 | 0.435 | 0.445 |
| R | 9.27 | 9.52 | 0.365 | 0.375 |
| S | 0.77 | 1.01 | 0.030 | 0.040 |

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and  are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

Literature Distribution Centers:

USA/EUROPE: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.

JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan.

ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.



MOTOROLA

◇ CODELINE TO BE PLACED HERE

MCM6226A/D

