

# 128K x 8 Bit Static Random Access Memory

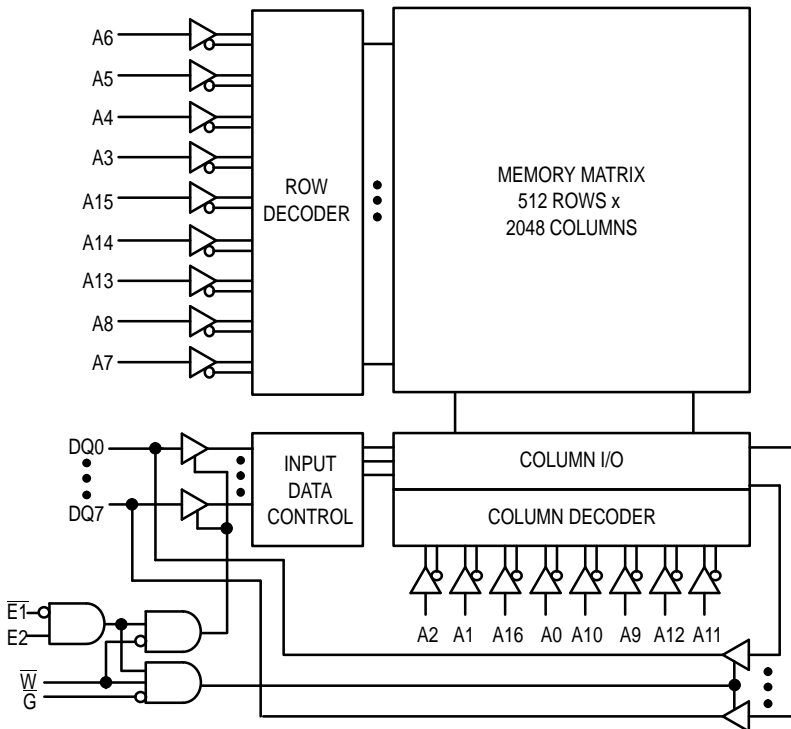
The MCM6226B is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits, fabricated using high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6226B is equipped with both chip enable ( $\overline{E1}$  and E2) and output enable ( $\overline{G}$ ) pins, allowing for greater system flexibility and eliminating bus contention problems.

The MCM6226B is available in 300 mil and 400 mil, 32 lead surface-mount SOJ packages.

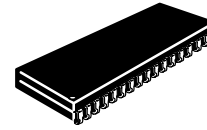
- Single 5 V  $\pm$  10% Power Supply
- Fast Access Times: 15/17/20/25/35 ns
- Equal Address and Chip Enable Access Times
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Low Power Operation: 130/125/120/115/110 mA Maximum, Active AC

### BLOCK DIAGRAM



## MCM6226B

WJ PACKAGE  
400 MIL SOJ  
CASE 857A-02



J PACKAGE  
300 MIL SOJ  
CASE 857-02

### PIN ASSIGNMENT

NC	1	32	VCC
A0	2	31	A16
A1	3	30	E2
A2	4	29	$\overline{W}$
A3	5	28	A15
A4	6	27	A14
A5	7	26	A13
A6	8	25	A12
A7	9	24	$\overline{G}$
A8	10	23	A11
A9	11	22	$\overline{E1}$
A10	12	21	DQ7
DQ0	13	20	DQ6
DQ1	14	19	DQ5
DQ2	15	18	DQ4
VSS	16	17	DQ3

### PIN NAMES

A0 – A16	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$ , E2	Chip Enables
DQ0 – DQ7	Data Inputs/Outputs
NC	No Connection
VCC	+ 5 V Power Supply
VSS	Ground

## TRUTH TABLE

E1	E2	$\bar{G}$	$\bar{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	X	Not Selected	High-Z	—	I <sub>SB1</sub> , I <sub>SB2</sub>
X	L	X	X	Not Selected	High-Z	—	I <sub>SB1</sub> , I <sub>SB2</sub>
L	H	H	H	Output Disabled	High-Z	—	I <sub>CCA</sub>
L	H	L	H	Read	D <sub>out</sub>	Read	I <sub>CCA</sub>
L	H	X	L	Write	D <sub>in</sub>	Write	I <sub>CCA</sub>

H = High, L = Low, X = Don't Care

## ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V <sub>SS</sub>	V <sub>CC</sub>	-0.5 to 7.0	V
Voltage Relative to V <sub>SS</sub> for Any Pin Except V <sub>CC</sub>	V <sub>in</sub> , V <sub>out</sub>	-0.5 to V <sub>CC</sub> + 0.5	V
Output Current (per I/O)	I <sub>out</sub>	± 20	mA
Power Dissipation	P <sub>D</sub>	1.1	W
Temperature Under Bias	T <sub>bias</sub>	-10 to +85	°C
Operating Temperature	T <sub>A</sub>	0 to +70	°C
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

## DC OPERATING CONDITIONS AND CHARACTERISTICS

(V<sub>CC</sub> = 5.0 V ± 10%, T<sub>A</sub> = 0 to 70°C, Unless Otherwise Noted)

### RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V <sub>CC</sub>	4.5	5.5	V
Input High Voltage	V <sub>IH</sub>	2.2	V <sub>CC</sub> + 0.3**	V
Input Low Voltage	V <sub>IL</sub>	-0.5*	0.8	V

\* V<sub>IL</sub> (min) = -0.5 V dc; V<sub>IL</sub> (min) = -2.0 V ac (pulse width ≤ 20 ns).

\*\* V<sub>IH</sub> (max) = V<sub>CC</sub> + 0.3 V dc; V<sub>IH</sub> (max) = V<sub>CC</sub> + 2 V ac (pulse width ≤ 20 ns).

### DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V <sub>in</sub> = 0 to V <sub>CC</sub> )	I <sub>lkg(I)</sub>	—	± 1	μA
Output Leakage Current ( $\bar{E}^* = V_{IH}$ , V <sub>out</sub> = 0 to V <sub>CC</sub> )	I <sub>lkg(O)</sub>	—	± 1	μA
AC Active Supply Current (I <sub>out</sub> = 0 mA, V <sub>CC</sub> = max)	I <sub>CCA</sub>	—	130 125 120 115 110	mA
AC Standby Current (V <sub>CC</sub> = max, $\bar{E}^* = V_{IH}$ , f ≤ f <sub>max</sub> )	I <sub>SB1</sub>	—	40 35 30 25 20	mA
CMOS Standby Current ( $\bar{E}^* \geq V_{CC} - 0.2$ V, V <sub>in</sub> ≤ V <sub>SS</sub> + 0.2 V or ≥ V <sub>CC</sub> - 0.2 V, V <sub>CC</sub> = max, f = 0 MHz)	I <sub>SB2</sub>	—	5	mA
Output Low Voltage (I <sub>OL</sub> = +8.0 mA)	V <sub>OL</sub>	—	0.4	V
Output High Voltage (I <sub>OH</sub> = -4.0 mA)	V <sub>OH</sub>	2.4	—	V

\* $\bar{E}^1$  and E2 are represented by  $\bar{E}$  in this data sheet. E2 is of opposite polarity to  $\bar{E}^1$ .

**CAPACITANCE** (f = 1.0 MHz, dV = 3.0 V, T<sub>A</sub> = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit	
Input Capacitance	All Inputs Except Clocks and DQs	C <sub>in</sub>	4	6	pF
	E <sub>1</sub> , E <sub>2</sub> , $\overline{G}$ , and $\overline{W}$	C <sub>ck</sub>	5	8	pF
I/O Capacitance	DQ	C <sub>I/O</sub>	5	8	pF

**AC OPERATING CONDITIONS AND CHARACTERISTICS**

(V<sub>CC</sub> = 5.0 V ± 10%, T<sub>A</sub> = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V      Output Timing Measurement Reference Level ..... 1.5 V  
 Input Rise/Fall Time ..... 2 ns      Output Load ..... See Figure 1A  
 Input Timing Measurement Reference Level ..... 1.5 V

**READ CYCLE TIMING** (See Notes 1, 2, and 3)

Parameter	Symbol	6226B-15		6226B-17		6226B-20		6226B-25		6226B-35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t <sub>AVAV</sub>	15	—	17	—	20	—	25	—	35	—	ns	4
Address Access Time	t <sub>AVQV</sub>	—	15	—	17	—	20	—	25	—	35	ns	
Enable Access Time	t <sub>ELQV</sub>	—	15	—	17	—	20	—	25	—	35	ns	5
Output Enable Access Time	t <sub>GLQV</sub>	—	6	—	7	—	7	—	8	—	8	ns	
Output Hold from Address Change	t <sub>AXQX</sub>	5	—	5	—	5	—	5	—	5	—	ns	
Enable Low to Output Active	t <sub>ELQX</sub>	5	—	5	—	5	—	5	—	5	—	ns	6, 7, 8
Output Enable Low to Output Active	t <sub>GLQX</sub>	0	—	0	—	0	—	0	—	0	—	ns	6, 7, 8
Enable High to Output High-Z	t <sub>EHQZ</sub>	0	6	0	7	0	7	0	8	0	8	ns	6, 7, 8
Output Enable High to Output High-Z	t <sub>GHQZ</sub>	0	6	0	7	0	7	0	8	0	8	ns	6, 7, 8

NOTES:

1.  $\overline{W}$  is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. E<sub>1</sub> and E<sub>2</sub> are represented by  $\overline{E}$  in this data sheet. E<sub>2</sub> is of opposite polarity to  $\overline{E}$ .
4. All timings are referenced from the last valid address to the first transitioning address.
5. Addresses valid prior to or coincident with  $\overline{E}$  going low.
6. At any given voltage and temperature, t<sub>EHQZ</sub> max is less than t<sub>ELQX</sub> min, and t<sub>GHQZ</sub> max is less than t<sub>GLQX</sub> min, both for a given device and from device to device.
7. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
8. This parameter is sampled and not 100% tested.
9. Device is continuously selected ( $\overline{E} \leq V_{IL}$ ,  $\overline{G} \leq V_{IL}$ ).

**AC TEST LOADS**

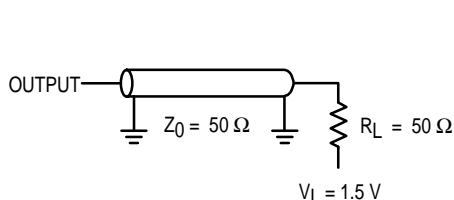


Figure 1A

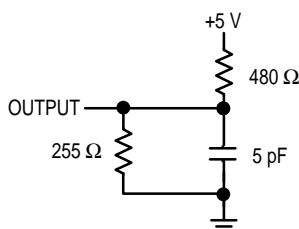
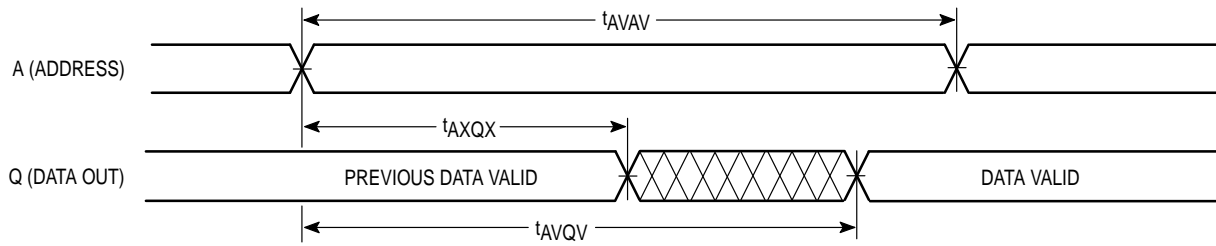


Figure 1B

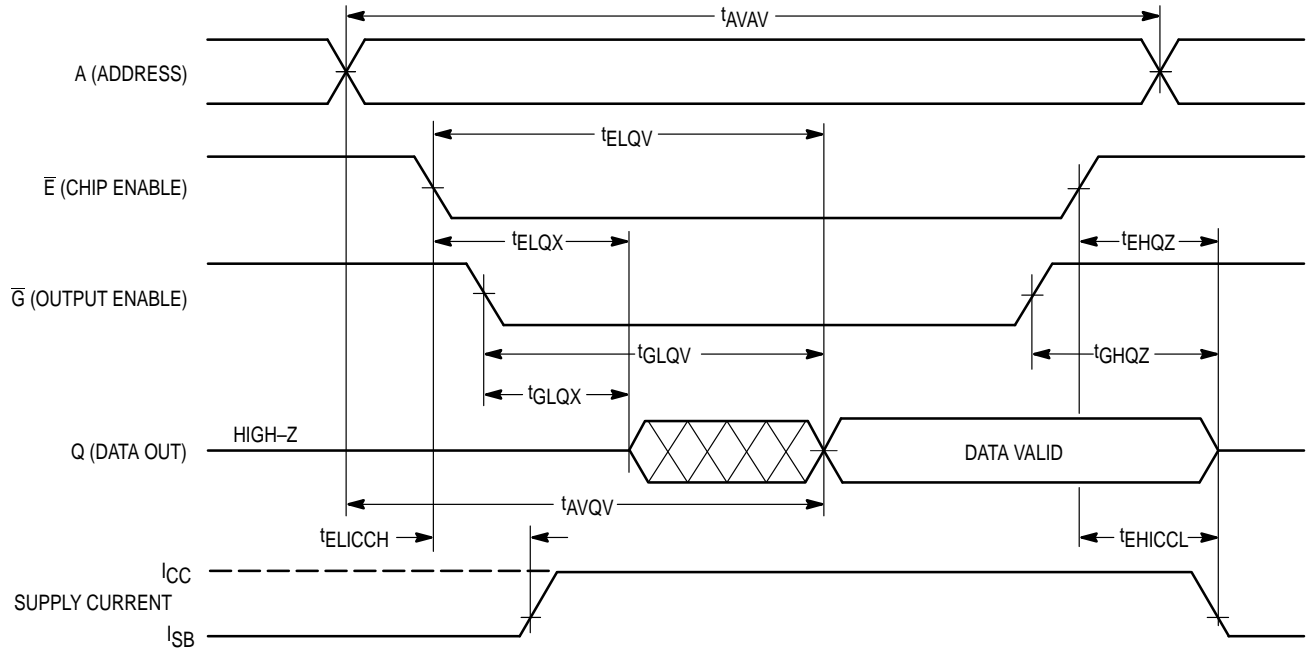
**TIMING LIMITS**

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

**READ CYCLE 1** (See Notes 1, 2, 3, and 9)



**READ CYCLE 2** (See Notes 3 and 5)



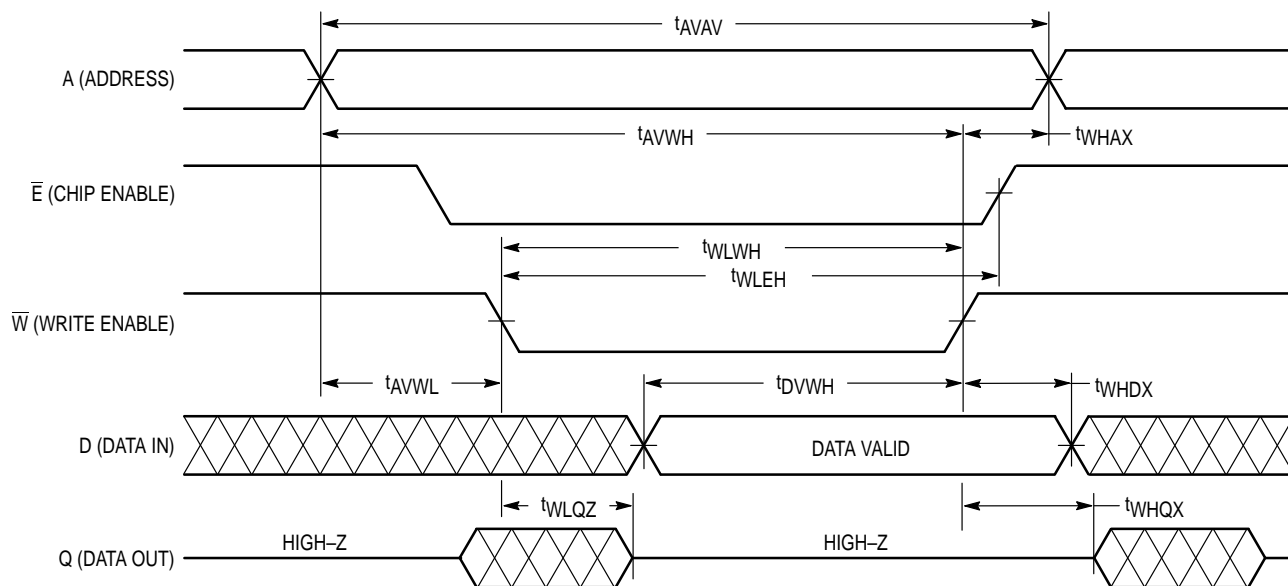
**WRITE CYCLE 1** ( $\overline{W}$  Controlled, See Notes 1, 2, 3, and 4)

Parameter	Symbol	6226B-15		6226B-17		6226B-20		6226B-25		6226B-35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	$t_{AVAV}$	15	—	17	—	20	—	25	—	35	—	ns	5
Address Setup Time	$t_{AVWL}$	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	$t_{AVWH}$	12	—	14	—	15	—	17	—	20	—	ns	
Write Pulse Width	$t_{WLWH}$ , $t_{WLEH}$	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	$t_{DVWH}$	7	—	8	—	8	—	10	—	11	—	ns	
Data Hold Time	$t_{WHDX}$	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Data High-Z	$t_{WLQZ}$	0	6	0	7	0	7	0	8	0	8	ns	6, 7, 8
Write High to Output Active	$t_{WHQX}$	5	—	5	—	5	—	5	—	5	—	ns	6, 7, 8
Write Recovery Time	$t_{WHAX}$	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:

1. A write occurs during the overlap of  $\overline{E}$  low and  $\overline{W}$  low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3.  $\overline{E}1$  and  $E2$  are represented by  $\overline{E}$  in this data sheet.  $E2$  is of opposite polarity to  $\overline{E}1$ .
4. If  $\overline{G}$  goes low coincident with or after  $\overline{W}$  goes low, the output will remain in a high-impedance state.
5. All timings are referenced from the last valid address to the first transitioning address.
6. Transition is measured  $\pm 500$  mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. At any given voltage and temperature,  $t_{WLQZ}$  max is less than  $t_{WHQX}$  min both for a given device and from device to device.

**WRITE CYCLE 1** ( $\overline{W}$  Controlled See Notes 1, 2, 3, and 4)



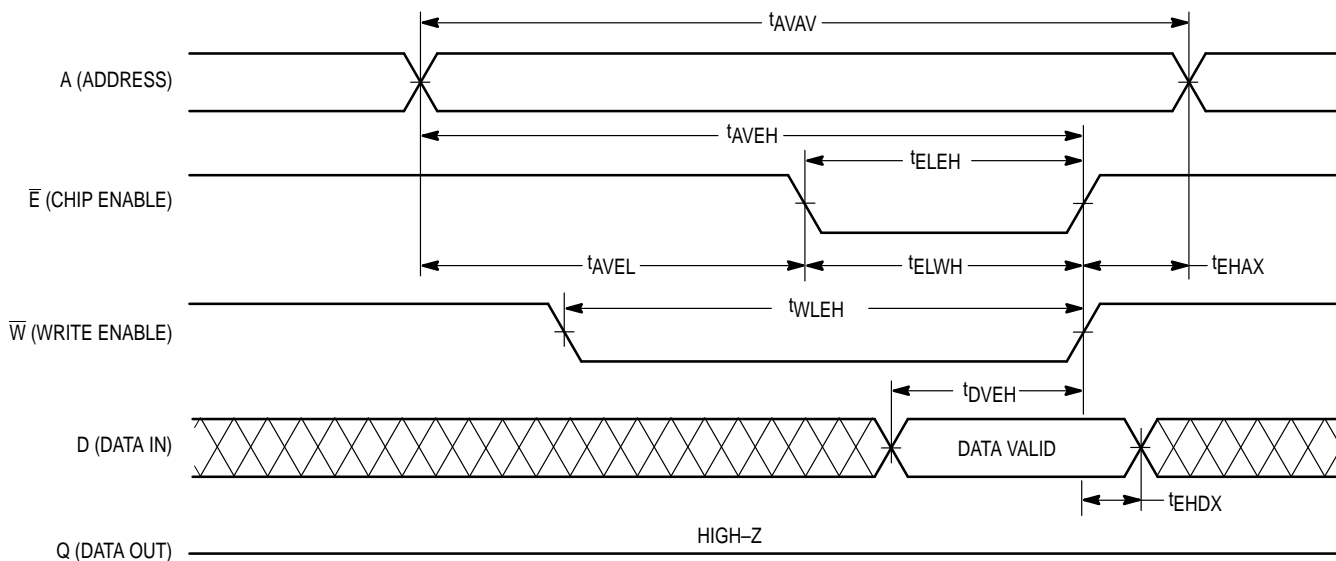
**WRITE CYCLE 2** ( $\bar{E}$  Controlled, See Notes 1, 2, 3, and 4)

Parameter	Symbol	6226B-15		6226B-17		6226B-20		6226B-25		6226B-35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	$t_{AVAV}$	15	—	17	—	20	—	25	—	35	—	ns	5
Address Setup Time	$t_{AVEL}$	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	$t_{AVEH}$	12	—	14	—	15	—	17	—	20	—	ns	
Enable to End of Write	$t_{ELEH}$ , $t_{ELWH}$	10	—	11	—	12	—	15	—	20	—	ns	6, 7
Write Pulse Width	$t_{WLEH}$	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	$t_{DVEH}$	7	—	8	—	8	—	10	—	11	—	ns	
Data Hold Time	$t_{EHDX}$	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	$t_{EHAX}$	0	—	0	—	0	—	0	—	0	—	ns	

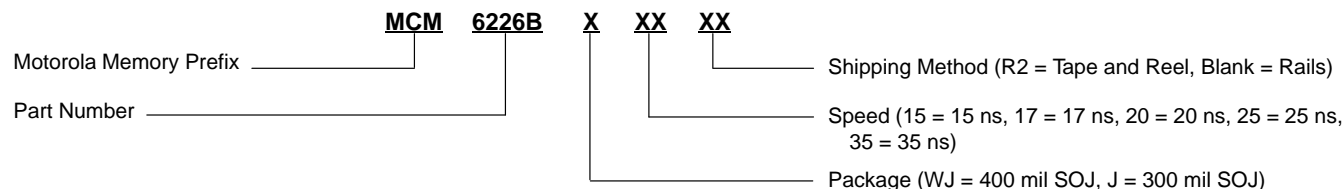
**NOTES:**

1. A write occurs during the overlap of  $\bar{E}$  low and  $\bar{W}$  low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3.  $\bar{E}1$  and  $E2$  are represented by  $\bar{E}$  in this data sheet.  $E2$  is of opposite polarity to  $\bar{E}1$ .
4. If  $\bar{G}$  goes low coincident with or after  $\bar{W}$  goes low, the output will remain in a high-impedance state.
5. All timings are referenced from the last valid address to the first transitioning address.
6. If  $\bar{E}$  goes low coincident with or after  $\bar{W}$  goes low, the output will remain in a high-impedance state.
7. If  $\bar{E}$  goes high coincident with or before  $\bar{W}$  goes high, the output will remain in a high-impedance state.

**WRITE CYCLE 2** ( $\bar{E}$  Controlled See Notes 1, 2, 3, and 4)



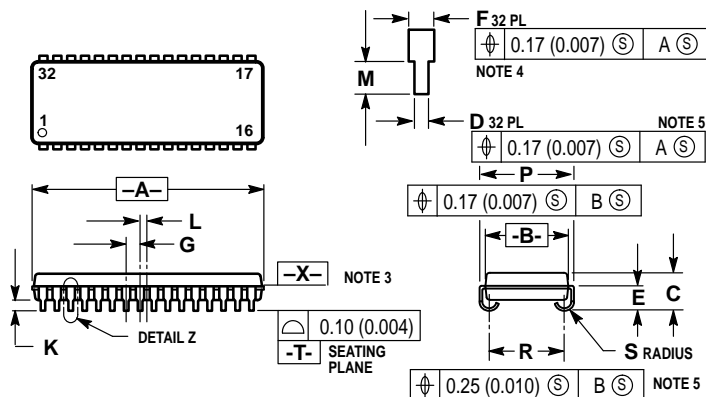
**ORDERING INFORMATION**  
(Order by Full Part Number)



Full Part Numbers —	MCM6226BJ15	MCM6226BJ15R2	MCM6226BWJ15	MCM6226BWJ15R2
	MCM6226BJ17	MCM6226BJ17R2	MCM6226BWJ17	MCM6226BWJ17R2
	MCM6226BJ20	MCM6226BJ20R2	MCM6226BWJ20	MCM6226BWJ20R2
	MCM6226BJ25	MCM6226BJ25R2	MCM6226BWJ25	MCM6226BWJ25R2
	MCM6226BJ35	MCM6226BJ35R2	MCM6226BWJ35	MCM6226BWJ35R2

# PACKAGE DIMENSIONS

CASE 857-02  
32 LEAD  
300 MIL SOJ

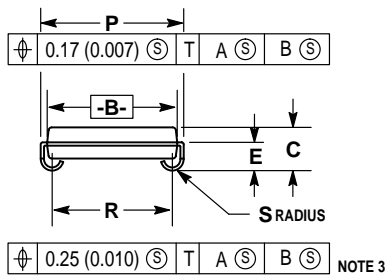
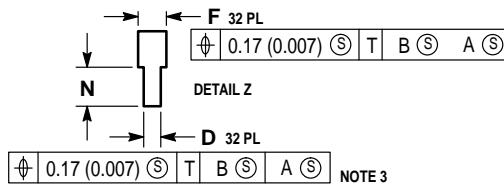
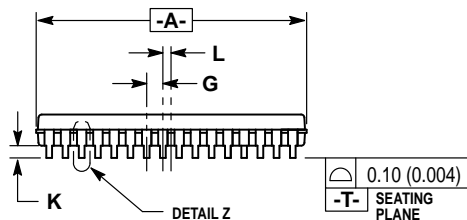


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DATUM PLANE -X- LOCATED AT TOP OF MOLD PARTING LINE AND COINCIDENT WITH TOP OF LEAD, WHERE LEAD EXITS BODY.
4. TO BE DETERMINED AT PLANE -X-.
5. TO BE DETERMINED AT PLANE -T-.
6. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
7. 857-01 IS OBSOLETE, NEW STANDARD 857-02.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.83	21.08	0.820	0.830
B	7.50	7.74	0.295	0.305
C	3.26	3.75	0.128	0.148
D	0.41	0.50	0.016	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
K	0.89	1.14	0.035	0.045
L	0.64 BSC		0.025 BSC	
N	0.76	1.14	0.030	0.045
P	8.38	8.64	0.330	0.340
R	6.60	6.86	0.260	0.270
S	0.77	1.01	0.030	0.040

**32 LEAD  
400 MIL SOJ  
CASE 857A-02**



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TO BE DETERMINED AT PLANE -T-.
4. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION A & B INCLUDE MOLD MISMATCH AND ARE DETERMINED AT THE PARTING LINE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.83	21.08	0.820	0.830
B	10.03	10.29	0.395	0.405
C	3.26	3.75	0.128	0.148
D	0.41	0.50	0.016	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
K	0.89	1.14	0.035	0.045
L	0.64 BSC		0.025 BSC	
N	0.76	1.14	0.030	0.045
P	11.05	11.30	0.435	0.445
R	9.27	9.52	0.365	0.375
S	0.77	1.01	0.030	0.040

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MCM6226B/D

