

54AC74 • 54ACT74 Dual D-Type Positive Edge-Triggered Flip-Flop

General Description

The 'AC/'ACT74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, \bar{Q}) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

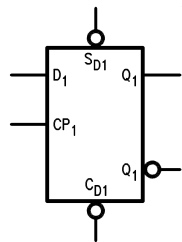
Asynchronous Inputs:

- LOW input to \bar{S}_D (Set) sets Q to HIGH level
- LOW input to \bar{C}_D (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on \bar{C}_D and \bar{S}_D makes both Q and \bar{Q} HIGH

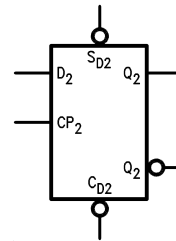
Features

- I_{CC} reduced by 50%
- Output source/sink 24 mA
- 'ACT74 has TTL-compatible inputs
- Standard Microcircuit Drawing (SMD)
 - 'AC74: 5962-88520
 - 'ACT74: 5962-87525

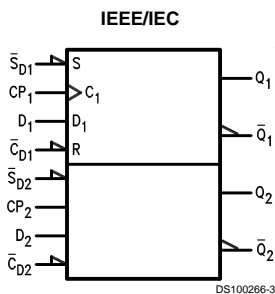
Logic Symbols



DS100266-1



DS100266-2

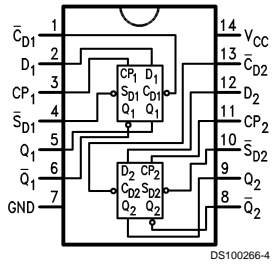


DS100266-3

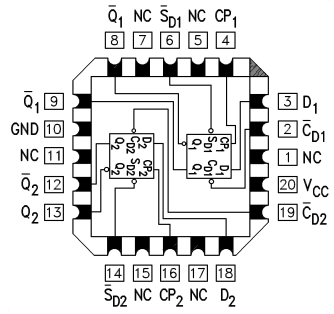
Pin Names	Description
D_1, D_2	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\bar{C}_{D1}, \bar{C}_{D2}$	Direct Clear Inputs
$\bar{S}_{D1}, \bar{S}_{D2}$	Direct Set Inputs
$Q_1, \bar{Q}_1, Q_2, \bar{Q}_2$	Outputs

Connection Diagrams

Pin Assignment for DIP and Flatpak



Pin Assignment for LCC



Truth Table

(Each Half)

Inputs				Outputs	
\bar{S}_D	\bar{C}_D	CP	D	Q	\bar{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↗	H	H	L
H	H	↘	L	L	H
H	H	L	X	Q_0	\bar{Q}_0

H = HIGH Voltage Level

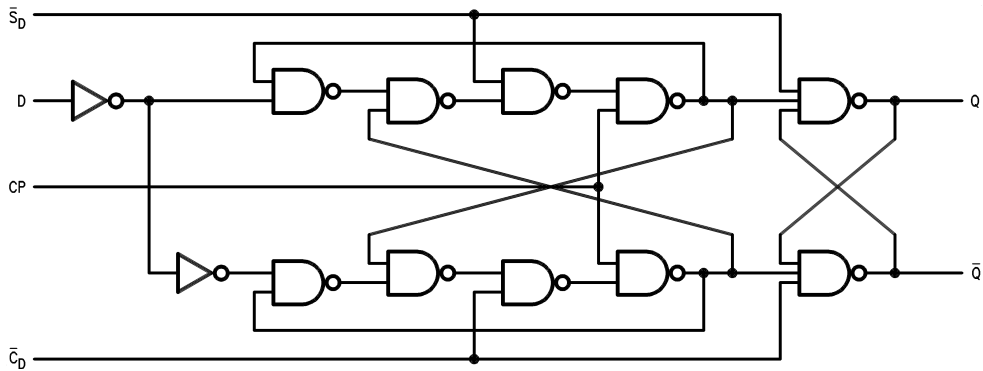
L = LOW Voltage Level

X = Immaterial

↗ = LOW-to-HIGH Clock Transition

$Q_0(\bar{Q}_0)$ = Previous $Q(\bar{Q})$ before LOW-to-HIGH Transition of Clock

Logic Diagram



DS100266-6

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	-65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54AC/ACT	-55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	54AC	Units	Conditions	
			$T_A =$ -55°C to +125°C			
			Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	3.15			
		5.5	3.85			
V_{IL}	Maximum Low Level Input Voltage	3.0	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	1.35			
		5.5	1.65			
V_{OH}	Minimum High Level Output Voltage	3.0	2.9	V	$I_{OUT} = -50 \mu A$	
		4.5	4.4			
		5.5	5.4			
			3.0	2.4	V	(Note 2) $V_{IN} = V_{IL}$ or V_{IH} -12 mA I_{OH} -24 mA -24 mA
			4.5	3.7		
			5.5	4.7		
V_{OL}	Maximum Low Level Output Voltage	3.0	0.1	V	$I_{OUT} = 50 \mu A$	
		4.5	0.1			
		5.5	0.1			
			3.0	0.5	V	(Note 2) $V_{IN} = V_{IL}$ or V_{IH} 12 mA I_{OL} 24 mA 24 mA
			4.5	0.5		
			5.5	0.5		
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	μA	$V_I = V_{CC}, GND$	

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V _{CC} (V)	54AC	Units	Conditions
			T _A = -55°C to +125°C		
			Guaranteed Limits		
I _{OLD}	(Note 3) Minimum Dynamic Output Current	5.5	50	mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5	-50	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5	40.0	µA	V _{IN} = V _{CC} or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V _{CC} (V)	54ACT	Units	Conditions
			T _A = -55°C to +125°C		
			Guaranteed Limits		
V _{IH}	Minimum High Level Input Voltage	4.5	2.0	V	V _{OUT} = 0.1V or V _{CC} - 0.1V
		5.5	2.0		
V _{IL}	Maximum Low Level Input Voltage	4.5	0.8	V	V _{OUT} = 0.1V or V _{CC} - 0.1V
		5.5	0.8		
V _{OH}	Minimum High Level Output Voltage	4.5	4.4	V	I _{OUT} = -50 µA
		5.5	5.4		
		4.5	3.70	V	(Note 5) V _{IN} = V _{IL} or V _{IH} I _{OH} -24 mA -24 mA
		5.5	4.70		
V _{OL}	Maximum Low Level Output Voltage	4.5	0.1	V	I _{OUT} = 50 µA
		5.5	0.1		
		4.5	0.50	V	(Note 5) V _{IN} = V _{IL} or V _{IH} I _{OL} 24 mA 24 mA
		5.5	0.50		
I _{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	V _I = V _{CC} , GND
I _{CCT}	Maximum I _{CC} /Input	5.5	1.6	mA	V _I = V _{CC} - 2.1V
I _{OLD}	(Note 6) Minimum Dynamic Output Current	5.5	50	mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5	-50	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5	40.0	µA	V _{IN} = V _{CC} or GND

Note 5: All outputs loaded; thresholds on input associated with output under test.

Note 6: Maximum test duration 2.0 ms, one output loaded at a time.

Note 7: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V) (Note 8)	54AC		Units	Fig. No.
			T _A = -55°C to +125°C C _L = 50 pF			
			Min	Max		
f _{max}	Maximum Clock Frequency	3.3	70		MHz	
		5.0	95			
t _{PLH}	Propagation Delay C _{Dn} or S _{Dn} to Q _n or Q _n	3.3	1.0	13.0	ns	
		5.0	1.0	9.5		
t _{PHL}	Propagation Delay C _{Dn} or S _{Dn} to Q _n or Q _n	3.3	1.0	14.0	ns	
		5.0	1.0	10.5		
t _{PLH}	Propagation Delay CP _n to Q _n or Q _n	3.3	1.0	17.5	ns	
		5.0	1.0	12.0		
t _{PHL}	Propagation Delay CP _n to Q _n or Q _n	3.3	1.0	13.5	ns	
		5.0	1.0	10.0		

Note 8: Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements

Symbol	Parameter	V _{CC} (V) (Note 9)	54AC		Units	Fig. No.
			T _A = -55°C to +125°C C _L = 50 pF			
			Guaranteed Limits			
t _s	Set-up Time, HIGH or LOW D _n to CP _n	3.3	5.0		ns	
		5.0	4.0			
t _h	Hold Time, HIGH or LOW D _n to CP _n	3.3	0.5		ns	
		5.0	0.5			
t _w	CP _n or C _{Dn} or S _{Dn} Pulse Width	3.3	8.0		ns	
		5.0	5.5			
t _{rec}	Recovery Time C _{Dn} or S _{Dn} to CP	3.3	0.5		ns	
		5.0	0.5			

Note 9: Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V) (Note 10)	54ACT		Units
			T _A = -55°C to +125°C C _L = 50 pF		
			Min	Max	
f _{max}	Maximum Clock Frequency	5.0	85		MHz
t _{PLH}	Propagation Delay C _{Dn} or S _{Dn} to Q _n or Q _n	5.0	1.0	11.5	ns
t _{PHL}	Propagation Delay C _{Dn} or S _{Dn} to Q _n or Q _n	5.0	1.0	12.5	ns
t _{PLH}	Propagation Delay CP _n to Q _n or Q _n	5.0	1.0	14.0	ns
t _{PHL}	Propagation Delay CP _n to Q _n or Q _n	5.0	1.0	12.0	ns

AC Electrical Characteristics (Continued)

Note 10: Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

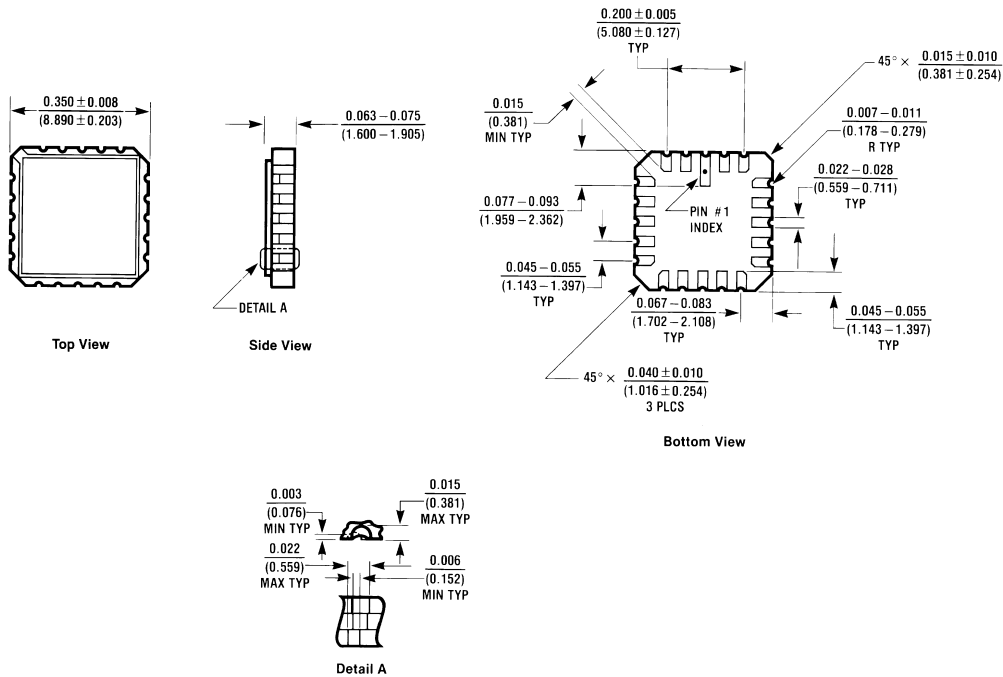
Symbol	Parameter	V _{CC} (V) (Note 11)	54ACT	Units	Fig. No.
			T _A = -55°C C _L = 50 pF Guaranteed Limits		
t _s	Set-up Time, HIGH or LOW D _n to CP _n	5.0	4.0	ns	
t _h	Hold Time, HIGH or LOW D _n to CP _n	5.0	1.0	ns	
t _w	CP _n or \overline{C}_{Dn} or \overline{S}_{Dn} Pulse Width	5.0	7.0	ns	
t _{rec}	Recovery Time \overline{C}_{Dn} or \overline{S}_{Dn} to CP	5.0	0.5	ns	

Note 11: Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

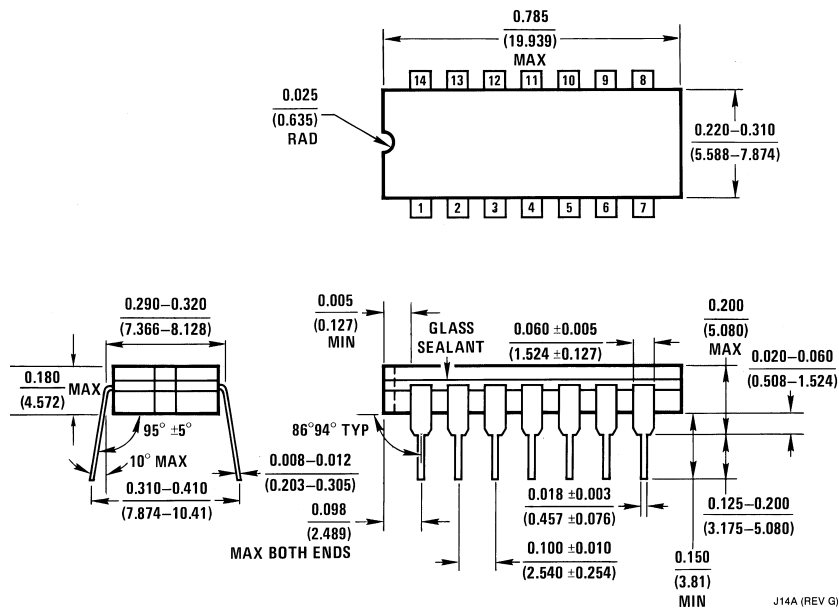
Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	35.0	pF	V _{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted



E20A (REV D)

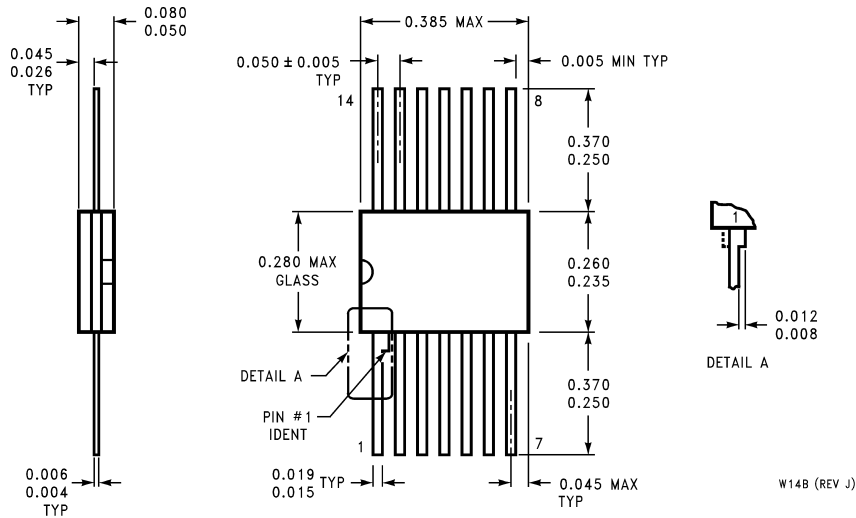
**20-Terminal Ceramic Leadless Chip Carrier (L)
 NS Package Number E20A**



J14A (REV G)

**14-Lead Ceramic Dual-In-Line Package (D)
 NS Package Number J14A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**14-Lead Ceramic Flatpak (F)
NS Package Number W14B**

W14B (REV J)

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