National Semiconductor

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LM3101 Secondary-Side PWM Controller

General Description

The LM3101 is a precision high-speed PWM controller. It is designed to provide secondary-side feedback for offline Switch-Mode Power Supplies (SMPS) using pulse communication to the primary-side driver. The LM3101 is applicable in all of the popular converter topologies such as flyback or forward.

The LM3101 combined with its companion LM3001 Primary-Side Driver forms a regulator chip-set that provides precision control of offline or other isolated DC/DC converters. The communication is realized between the two chips by a small pulse transformer, with one or two turns on its primary and secondary. This type of communication does not introduce any poles or zeroes in the control loop and yields the fastest possible loop response for the isolated switching regulator.

The secondary-side controller contains a precision 1.242V reference, an error amplifier, and a trimmed oscillator which is programmed with a single resistor. The LM3101 can realize voltage, current or charge mode control. Power supply monitor features include power-on reset with programmable delay and overvoltage protection.

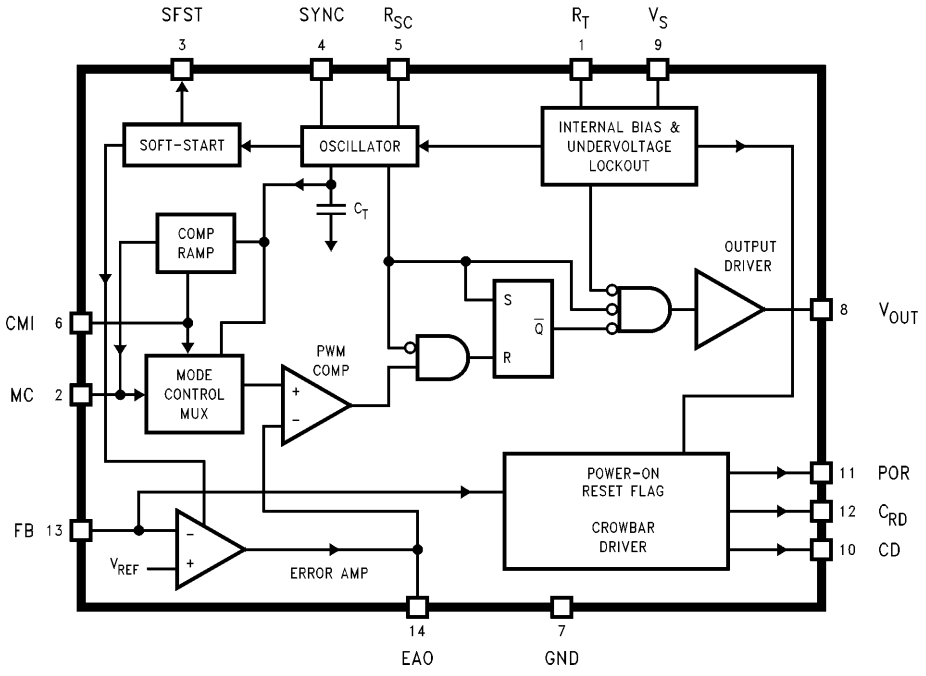
Features

- ±2% precision voltage reference
- Wide-bandwidth (8 MHz) error amplifier
- External synchronization
- Frequency shift during an output short circuit
- Power-on reset flag with programmable delay
- Overvoltage crowbar trigger circuit
- Ramped reference Soft-Start
- Operation beyond 1 MHz
- Voltage, current, or charge mode control

Typical Applications

- Isolated offline switching power supplies
- Isolated DC/DC power converters
- Flyback regulator
- Forward converter

Block Diagram



TL/H/11436–1

RRD-B30M75/Printed in U. S. A.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_S)	16V
Junction Temperature Range	$-65°C \le T_J \le +150°C$
ESD	1 kV
Lead Temperature (Soldering, 5 sec.)	260°C

Operating Ratings

Supply Voltage	$4.5V \le V_S \le 15V$
Junction Temperature Range	$-40°C \le T_J \le +125°C$

Electrical Characteristics

Specifications with standard typeface are for $T_J = 25°C$, and those in **bold typeface** apply over full **Operating Temperature Range**. Pin 2, MC, is connected to V_S by a 5 kΩ resistor—this selects voltage mode control operation. Unless otherwise specified, $T_A = 25°C$, $V_S = 5V$, $R_{FS} = 25\ k\Omega$ ($F_O = 500$ kHz).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
REFERENCE SECTION (Note 2)						
V_{REF}	Reference Voltage		1.230 **1.217**	1.242	1.254 **1.266**	V
$\Delta V_{REF}/\Delta V_S$	Line Regulation	$4.5V \le V_S \le 15V$		0.01	0.03	%/V
$\Delta V_{REF}/\Delta T$	Temperature Stability (Note 3)	$-40°C \le T_J \le +125°C$		**0.003**		%/°C
ERROR AMPLIFIER SECTION						
A_{VOL}	Open Loop Voltage Gain		75	90		dB
I_B	Input Bias Current		-1.0 $-$**2.0**	-0.5		μA
GBW	Gain-Bandwidth Product	$F_{TEST} = 100$ kHz	4.5	8		MHz
θ_M	Phase Margin	$A_V = 1$		52		Deg
SR	Slew Rate		2.5	6		V/μs
OSCILLATOR SECTION						
F_O	Oscillator Frequency (Note 4)	$R_T = 25\ k\Omega$	450 **425**	500	550 **575**	kHz
		$R_T = 12.5\ k\Omega$	0.88 **0.85**	1.0	1.12 **1.15**	MHz
F_{SC}	Oscillator Frequency in Output Short Circuit	$R_T = 25\ k\Omega$ ($F_O = 500$ kHz), $R_{SC} = 13\ k\Omega$ (Note 5)	120	187	260	kHz
		$R_T = 12.5\ k\Omega$ ($F_O = 1$ MHz), $R_{SC} = 6.34\ k\Omega$ (Note 5)	210	335	470	kHz
$\Delta F_O/\Delta T$	Temperature Stability	(Note 3)		**0.1**		%/°C
$\Delta F_O/\Delta V_S$	Line Stability	$4.5V \le V_S \le 15V$			0.9	%/V
V_{SYNC}	Synch Signal Amplitude	AC Coupled, Negative Edge Trigger (Note 6)	1.5 **2**			V_{PP}
$\Delta I_{COMP}/\Delta t$	Compensation Current Ramp Slope	$R_T = 25\ k\Omega$ $R_{MC} = 5\ k\Omega$ (Note 7)	155	208	260	μA/μs

Electrical Characteristics Specifications with standard typeface are for T_J = 25°C, and those in **bold typeface** apply over full **Operating Temperature Range**. Pin 2, MC is connected to V_S by a 5 kΩ resistor—this selects voltage mode control operation. Unless otherwise specified, T_A = 25°C, V_S = 5V, R_{FS} = 25 kΩ (F_O = 500 kHz). (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
PULSE WIDTH MODULATOR SECTION						
D_{MAX}	Maximum Duty Cycle	F_O = 500 kHz	88 **84**	92		%
		F_O = 1 MHz	84 **80**	90		%
D_{MIN}	Minimum Duty Cycle (Note 8)	F_O = 500 kHz		2.5	6 **8**	%
		F_O = 1 MHz		4	10 **12**	%
t_{dCS}	Current Sense Time Delay			75	100	ns
OUTPUT SECTION						
t_R	Rise Time	C_L = 100 pF		20		ns
t_F	Fall Time	C_L = 100 pF		30		ns
V_{OL}	Output Voltage	I_L = 4 mA Sinking F_O = 100 kHz		1.3	1.4 **1.6**	V
V_{OH}	Output Voltage	I_L = 4 mA Sourcing F_O = 100 kHz	3.6 **3.4**	3.8		V
OVER-VOLTAGE CROWBAR TRIGGER SECTION						
$\%V_{THC}$	Relative Trigger Threshold	Relative to Nominal Feedback Pin Voltage (Note 10)	18 **16**	20	22 **24**	%
I_{CD}	Crowbar Driver Output Current	R_{CD} = 10Ω	170	240		mA
t_{CD}	Crowbar Delay	R_{CD} = 10Ω, V_{CD} = 1V		400		ns
t_C	Minimum Trigger Pulse Width	(Note 11)		400		ns
POWER-ON RESET FLAG SECTION						
$\%V_{THP}$	Relative POR Trigger Threshold	Relative to Nominal Feedback Pin Voltage (Note 10)	−6 **−6.5**	−4.5	−3 **−2.5**	%
V_{POR}	POR Output Voltage	V_{FB} = 1.11V I_{POR} = 1.6 mA		0.2	0.5	V
V_{SM}	Minimum Supply Voltage (Note 12)	$V_{POR} \leq$ 0.5V I_{POR} = 1.6 mA		1	1.2	V
t_{DR}	Power-On Reset Delay	C_{RD} = 2 nF	65 **50**	120	185 **265**	μs
UNDER-VOLTAGE LOCKOUT SECTION						
V_{UV}	Start-Up Threshold	(Note 13)	3.65	3.92	4.20	V
V_{UVH}	Threshold Hysteresis			300		mV
SUPPLY SECTION						
I_S	Supply Current	V_S = 5V		11	16 **20**	mA
		4.5V ≤ V_S ≤ 15V		15	24 **28**	mA
I_{SFST}	Soft-Start Current (Note 14)	V_{SFST} = 0V	14.5	19.5	20.5	μA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: The reference voltage is measured at the error amplifier's output with the error amplifier connected as a non-inverting amplifier with a gain of one.

Note 3: The temperature coefficients of V_{REF} or F_O are defined as the worst-case ΔV_{REF} or ΔF_O measured at Specified Temperatures divided by the total span of the Specified Temperture Range (see graphs). There is no guarantee that the Specified Temperatures are exactly at the minimum of maximum deviation.

Note 4: The frequency of the internal oscillator is set by connecting a resistor, R_T, from pin 1 to ground. See detailed description of this feature in the Pin-by-Pin Description section or the Functional Description of this datasheet.

Note 5: A resistor, R_{SC}, is connected from pin 5 to the regulator's output. See detailed description of this feature in the Pin-by-Pin Description section or the Functional Description section of this datasheet.

Note 6: For this test, the frequency of synchronization, F_{SYNC}, is 600 kHz, C_{SYNC} is 220 pF, and R_{SYNC} is 1 kΩ. The internal oscillator will synchronize to an AC signal that is 1.1 to 1.5 times the free running oscillator frequency, F_O. See Functional Description section or Pin-by-Pin Description section for more detail on synchronization.

Note 7: I_{COMP} is sourced from pin 6 (CMI). See Functional Description section or Pin-by-Pin Description section for more detail on current mode operation.

Note 8: Minimum duty cycle is the smallest duty cycle that can be produced by the LM3101 in a given oscillator period. The controller can operate with effectively zero duty cycle—it skips cycles if the regulation cannot be maintained with the minimum duty cycle. This means that the output voltage of the switching converter is regulated down to no load.

Note 9: The current sense time delay is the time span between an input applied to the CMI pin (pin 6) and the change of state of V_{OUT} (pin 8) due to the input.

Note 10: Both these specifications, $\%V_{THC}$ and $\%V_{THP}$, are relative to the nominal feedback voltage, V_{FB}, by the factor: $[(V_{TH}-V_{FB})/V_{FB}]$.

Note 11: An internal delay circuit prevents triggering of the overvoltage crowbar circuit, for pulse widths less than 400 ns, to ensure noise immunity.

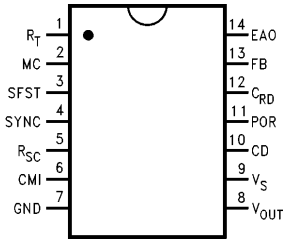
Note 12: This is the minimum supply voltage for which the power-on reset flag will continue to be valid (low).

Note 13: For $V_S < V_{UV}$, the output is off—it is in a high-impedance state.

Note 14: A resistor/capacitor circuit is normally connected from the soft start circuit, pin 3, to ground. The circuit provides a slow or "soft" start of the IC by slowly ramping the reference voltage from a lower initial value set by the resistor to its normal operating value. See detailed description of this feature in the Pin-by-Pin Description section or the Functional Description section of this datasheet.

Connection Diagram and Ordering Information

14-Lead Package
Top View



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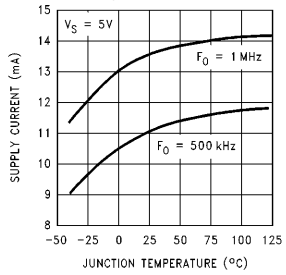
For Surface Mount Package
Order Number LM3101M
See NS Package Number M14B
For DIP Package
Order Number LM3101N
See NS Package Number N14A

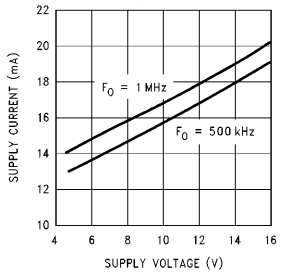
Typical Performance Characteristics

For F_O = 500 kHz, R_T = 25 kΩ
For F_O = 1 MHz, R_T = 12.5 kΩ

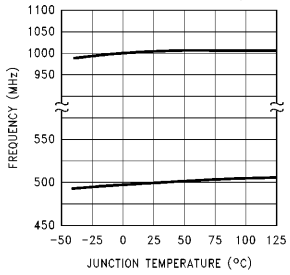
Supply Current



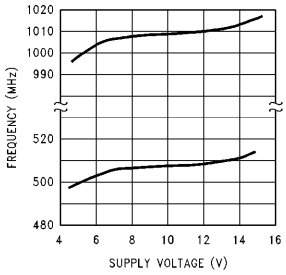
Supply Current vs Supply Voltage



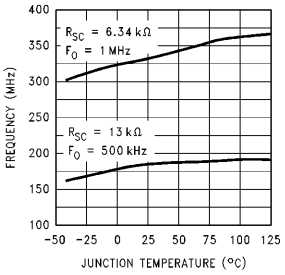
Oscillator Frequency



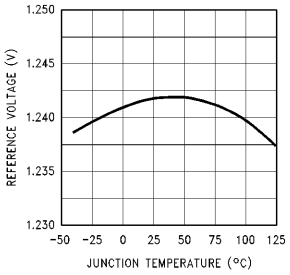
Oscillator Frequency vs Supply Voltage



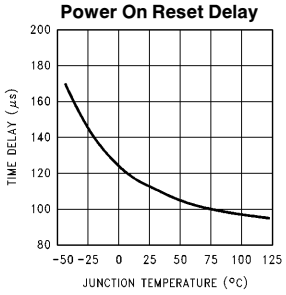
Short Circuit Oscillator Frequency



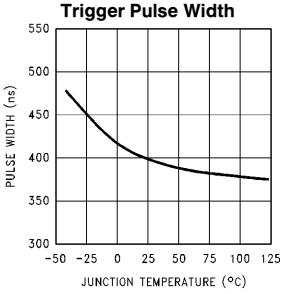
Reference Voltage



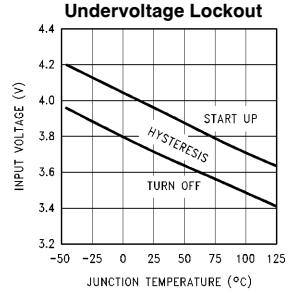
Power On Reset Delay



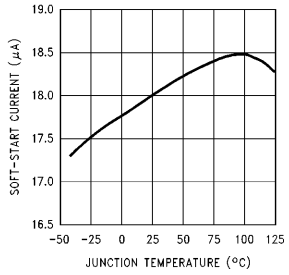
Minimum Over-Voltage Trigger Pulse Width



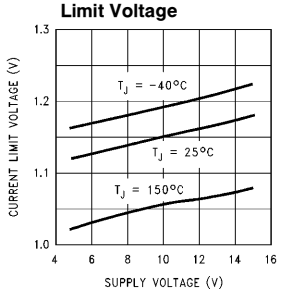
Undervoltage Lockout



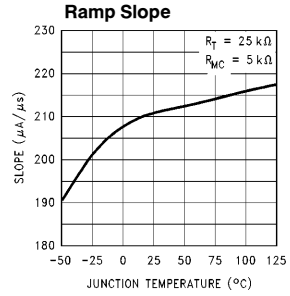
Soft-Start Current



Current Mode Input Limit Voltage



Compensation Current Ramp Slope



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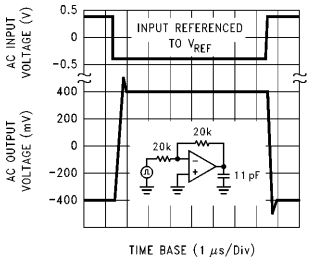
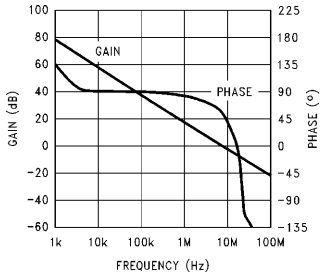
Typical Performance Characteristics (Continued)

Error Amplifier Step Response



Error Amplifier Open Loop Frequency Response



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Pin-by-Pin Description

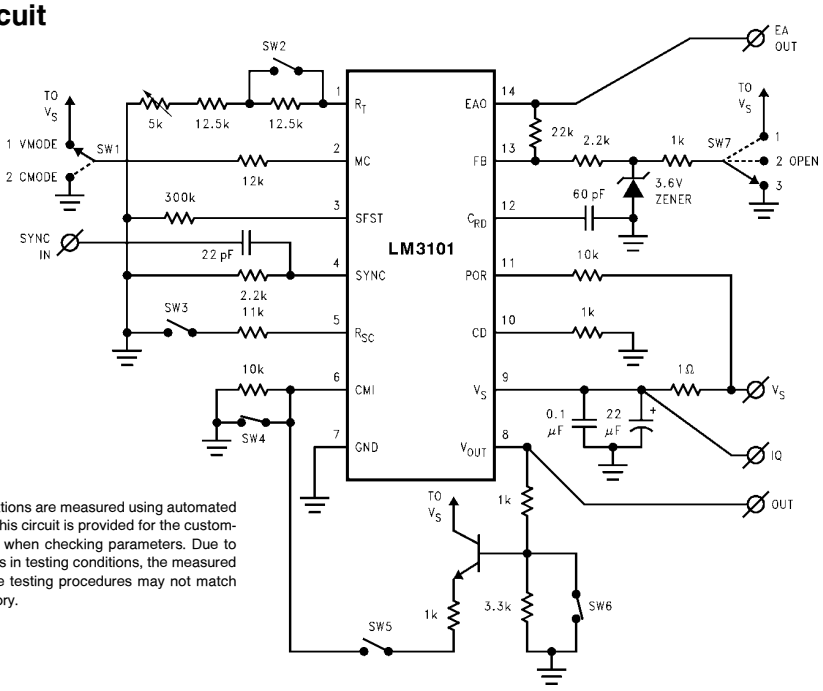
Pin #	Symbol	Function	Description
1	R_T	Frequency Setting Resistor	Connecting a resistor, R_T, between this pin and ground programs the frequency—from 50 kHz to 1 MHz—by the following equation: $R_T = 0.25/(F_O \bullet 20 \bullet 10^{-12})$ [F, Hz, Ω]. R_T also sets the internal bias current, which affects the operation of several sub-circuits within the IC.
2	MC	Mode Control	For voltage mode operation, connect a resistor, R_{MC}, from this pin to the supply voltage. For current mode operation, this pin is tied to ground via resistor R_{MC}. A current is sourced from the pin through the resistor such that it sets the slope of the compensating ramp, I_{COMP}, according to the equation: $\Delta I_{COMP}/\Delta T = 24 \bullet 10^3/(R_T \bullet R_{MC})$ [μA/μs, Ω].
3	SFST	Soft-Start Control	A series resistor-capacitor network tied from this pin to ground provides Soft-Start capability. The current charging the capacitor is: $I_{SFST} = 0.45/R_T$. [A, V, Ω]. Leave this pin open if it is not used.
4	SYNC	Synchronization Signal Input	An external negative pulse fed to this input will synchronize the internal oscillator. The frequency range of the external signal should be between 1.1 to 1.5 times the free-running frequency. Connect this pin to ground if it is not used.
5	R_{SC}	Short Circuit Frequency Shift Control	A resistor, R_{SC}, connected from this pin to the regulator output, determines the oscillator frequency during a short circuit by the formula: $R_{SC} = 0.09/[(0.267/R_T) - F_{SC} \bullet 20 \bullet -12]$ [F, Hz, Ω]. or, alternately, $F_{SC} = (1/20 \bullet 10^{-12}) \bullet [(0.267/R_T) - (0.09/R_{SC})]$ [F, Hz, Ω]. The recommended minimum ratio of short circuit frequency to oscillator frequency is one-third (nominal).
6	CMI	Current Mode Input	An analog voltage signal, proportional to the transformer primary current, fed to this input results in current mode operation. Connect this pin directly to ground if selecting voltage mode operation.
7	GND	Ground	Ground.
8	V_{OUT}	Output	Output pin. It produces a PWM pulse train that is fed back to the primary side of the regulator, via a pulse transformer.
9	V_S	Supply Voltage	Supply voltage.
10	CD	Crowbar Output Driver	This pin delivers a current when an overvoltage condition occurs on the output. It can be used to fire an external SCR to crowbar the output. Leave the pin open if not used.

Pin-by-Pin Description (Continued)

Pin #	Symbol	Function	Description
11	POR	Power-On Reset Flag	This open-collector output is driven low when either the supply voltage falls below the Undervoltage Lockout Threshold Voltage or the output voltage is less than the Power-on Reset Threshold Voltage. Leave the pin open if not used.
12	C_{RD}	Reset Delay Capacitor	Adding a capacitor between this pin and ground sets the power-on reset flag delay time according to the following formula: $C_{RD} = T_{DR}/60 \bullet 10^3$ [F, s, Ω]. Leave the pin open if not used. The POR flag will still operate if this function is not used.
13	FB	Feedback Input	A sample of the output voltage, via a resistor divider, is fed back into this pin, which is the inverting input of the error amplifier.
14	EAO	Error Amplifier Output	Error Amplifier Output. The output can source 1.5 mA typically and sink 300 μA typically. This pin is primarily used for loop compensation.

Note: Pins 1, 2, 4, 5, and 10 are internally clamped by a 5.6V zener diode. Do not force a voltage larger than 5V on these pins without a resistor to limit the current to below 1 mA. All other pins are limited to the supply voltage.

Test Circuit



LM3101 specifications are measured using automated test equipment. This circuit is provided for the customer's convenience when checking parameters. Due to possible variations in testing conditions, the measured values from these testing procedures may not match those of the factory.

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This test circuit is for exercising the LM3101 functions and measuring its specifications. With the switch positions shown, the supply current should measure 15 mA (typical) for a supply voltage of 15V. Changing the supply voltage to 5V and opening SW6 on the V_{OUT} pin should make the supply current 11 mA (typical). Changing SW7 to the supply voltage will shutdown the LM3101 output.

To test the oscillator section, adjust the 5 kΩ potentiometer at the R_T pin such that the oscillator frequency is approximately 500 kHz. Switch SW2 to obtain a 1 MHz frequency (typical). The maximum duty cycle of 92% typically can also be measured. Closing SW3 on pin R_{SC} and putting SW7 (pin FB) in the open position will change the oscillator frequency to approximately 180 kHz.

Switching the MC pin, SW1, to ground and opening SW4, the CMI pin, will put the device in current mode control. To measure the current sense time delay (typically 75 ns), close SW5 (connected to the CMI pin) and open SW6.

Functional Description

Oscillator/Synchronization Section

The operating frequency is set by a single resistor connected from the R_T pin (pin 1) to ground, according to the equation:

$$F_O = 0.25/(R_T \bullet 20\ pF) \qquad [kHz, \Omega].$$

Inserting a 25 kΩ for R_T sets the oscillator frequency at 500 kHz.

The oscillator is capable of synchronizing to an external source. To synchronize the oscillator, an external source is connected to the SYNC pin (pin 4) via a differentiator (see *Figure 1*). The external source delivers a pulse train to the differentiator, which converts this signal into an AC-coupled signal. The negative-edge of this signal, applied to the SYNC pin, will control the oscillator, and thus set the operating frequency. The recommended values for R_{SYNC} and C_{SYNC} are as follows:

$$R_{SYNC} = 1\ k\Omega \text{ (typical)}$$

and

$$C_{SYNC} \bullet R_{SYNC} > 1/(8 \bullet F_{SYNC}) \quad [F, \Omega, kHz].$$

To synchronize to a 600 kHz external source, and using a R_{SYNC} of 1 kΩ, the C_{SYNC} must be:

$$C_{SYNC} > 1/(8 \bullet R_{SYNC} \bullet F_{SYNC}) = 1/(8 \bullet 1\ k\Omega \bullet 600\ kHz) = 208\ pF \approx 220\ pF.$$

The oscillator frequency should range from 67% to 90% of the synchronization frequency. In the above example, the oscillator frequency can be between 400 kHz and 540 kHz.

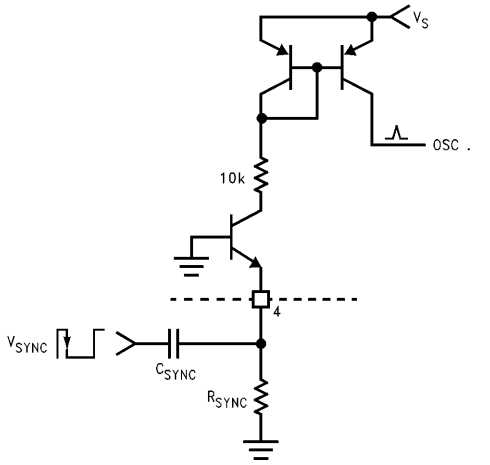

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FIGURE 1. Simplified Version of the Synchronization Circuit

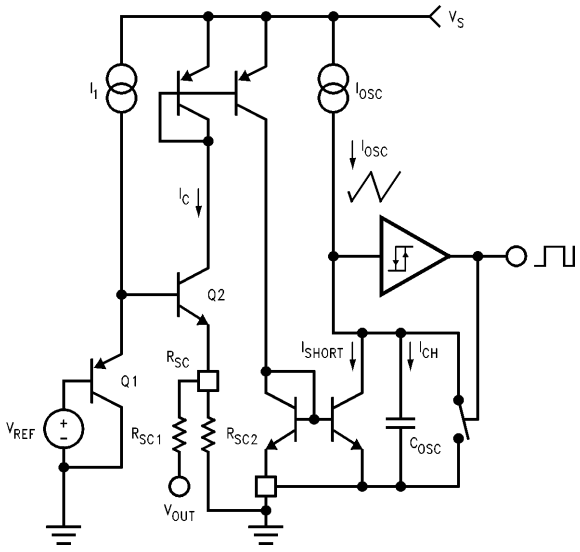

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FIGURE 2. Simplified Version of the Short Circuit Frequency Shift Circuit

Functional Description (Continued)

Frequency-Shift Circuit

The LM3101 has the ability to gradually reduce its operating frequency during an output short circuit. The amount that the frequency shifts and the output voltage threshold determining where the frequency starts to shift are both programmed by two external resistors, R_{SC1} and R_{SC2}, connected to the pin R_{SC} (pin 5).

A simplified internal schematic of the Frequency Shift Circuit is shown in *Figure 2*. The oscillator operates at its nominal frequency as long as the voltage at the emitter of the transistor Q2 is higher than the internal reference voltage, V_{REF}. Q2 emitter voltage is the output voltage, V_{OUT}, scaled down by the resistor divider:

$$V_{RSC} = V_{Q2E} = V_{OUT} \bullet R_{SC2}/(R_{SC1} + R_{SC2}) \quad [V, \Omega]$$

where $V_{Q2} > V_{REF}$ (1.24V) for normal operation.

If V_{OUT} drops, due to an overload, a current starts to flow through Q2. A cascoded current mirror causes one-tenth of this current to be subtracted from the timing capacitor charge current. Reducing the timing capacitor charge current results in decreasing the oscillator frequency. The breakpoint where the frequency-shift starts is programmed by the ratio of the two resistors:

$$V_{OUT(SC)} = 1.24V \bullet [1 + (R_{SC1}/R_{SC2})] \quad [V, \Omega].$$

The typical short circuit frequency is set by the following equations:

$$F_{SC} = [I_{OSC} - 0.1 \bullet \{((1.24V - V_{OUT(SC)})/R_{SC1}) + (1.24V/R_{SC2})\}] [1/(20\ pF \bullet 1.24V)] \quad [kHz, \mu A, V, \Omega]$$

where $I_{OSC} = 0.25 \bullet (1.24V/R_T)$.

For example, say 140 kΩ and 100 kΩ were selected for R_{SC1} and R_{SC2}, respectively, with R_T set to 25 kΩ. Then the output voltage level where the frequency starts to decay is:

$$V_{OUT(CL)} = 1.24V \bullet [1 + (140\ k\Omega/100\ k\Omega)] \cong 3.0V,$$

and the short circuit frequency is (I_{OSC} = 12.4 μA and assuming V_{OUT} is 0V during a short circuit):

$$F_{SC} = [12.4\ \mu A - 0.1 \bullet \{(1.24V/140\ k\Omega) + (1.24V/100\ k\Omega)\}] [1/(20\ pF \bullet 1.24V)] = 414.3\ kHz \cong 415\ kHz.$$

If R_{SC2} is omitted, the frequency starts to shift when V_{OUT} drops below V_{REF}. The short circuit frequency equation then becomes:

$$F_{SC} = (1/20\ pF) \bullet [(0.267/R_T) - (0.09/R_{SC1})] \quad [kHz, \Omega]$$

$$\downarrow$$

$$R_{SC1} = 0.09/[(0.267/R_T) - (F_{SC} \bullet 20\ pF)] \quad [\Omega, kHz].$$

Selecting a short-circuit frequency that is greater than one-third the operating frequency or 188 kHz leads to a resistor value of:

$$R_{SC1} = 0.09/[(0.267/25\ k\Omega) - (188\ kHz \bullet 20\ pF)] = 13\ k\Omega.$$

Mode Control

The LM3101 can operate in voltage mode, current mode, or charge mode control. Two multi-function pins are involved in setting the operating mode, the Mode Control pin (MC - pin 2) and the Current Mode Input pin (CMI - pin 6). *Figure 3* shows the simplified schematic diagram of the mode control circuit. To operate with voltage mode control, the MC pin is pulled high with a resistor (typically 3 kΩ), and the CMI pin is connected to ground. The mode comparator senses the MC pin voltage and sets the mode control multiplexer to voltage mode control. Notice that there is a 5.6V zener diode clamping the MC pin voltage.

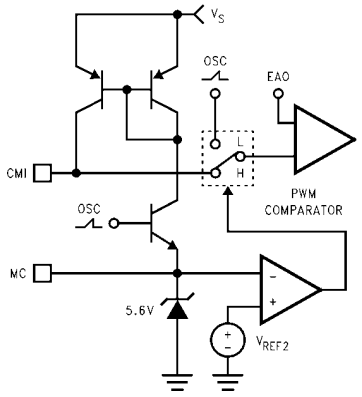

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FIGURE 3. Simplified Version of the Mode Control Circuit

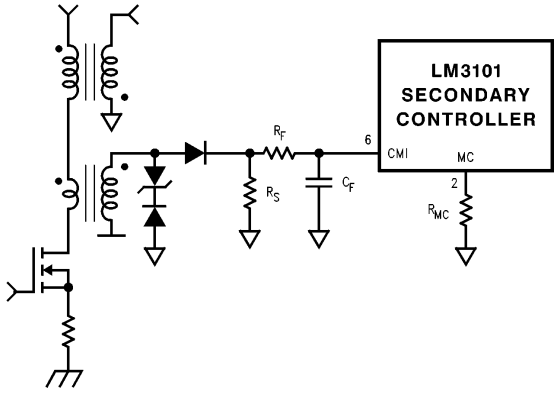

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FIGURE 4. Current Mode Sense Circuit

Functional Description (Continued)

To operate under current mode or charge mode control, insert a resistor, R_{MC}, between the MC pin and ground, and connect the CMI pin to the Current Mode Sense Circuit (see *Figure 4*). At the MC pin, a voltage, proportional to the oscillator ramp voltage, develops (see *Figure 3*). The voltage ramp applied to R_{MC} generates a current ramp, which is duplicated on the CMI pin due to the current mirror. The current ramp, which flows, out of the CMI pin to the resistor, R_F, is the compensation ramp, needed to stabilize converters operating at duty cycles above 50%. The slope of the compensating ramp can be scaled by R_F, which is connected between the CMI pin and the terminating resistor, R_S, of the current sense transformer. In all practical cases, R_F will be much greater than R_S. For both control modes, the current ramp provides slope compensation according to the equation:

$$\Delta I_{COMP}/\Delta t = 24 \bullet 10^3/(R_T \bullet R_{MC}) \quad [\mu A/\mu s, \Omega].$$

So, with R_T equal 25 kΩ and R_{MC} equal 6 kΩ, the compensation ramp slope is:

$$\Delta I_{COMP}/\Delta t = 24 \bullet 10^3/(25\ k\Omega \bullet 6\ k\Omega) = 160\ \mu A/\mu s.$$

The resistor R_F together with the capacitor C_F serves as an RC filter for the leading edge spike of the current sense waveform (the spike is caused by the output rectifier reverse recovery and/or the winding capacitance of the power transformer).

CHARGE MODE CONTROL

Under charge mode control, the current sense transformer drives a capacitor, C_1, that integrates the sensed switch current on a cycle-by-cycle basis. *Figure 5* shows the integrating current sense circuitry and the simplified details of the associated internal circuitry of the LM3101. Transistor Q_1 discharges the integrating capacitor C_1 once every switch cycle—during the switch off-time (Q1 can provide up to 20 mA of discharge current). Charge mode control yields the fastest average current control loop.

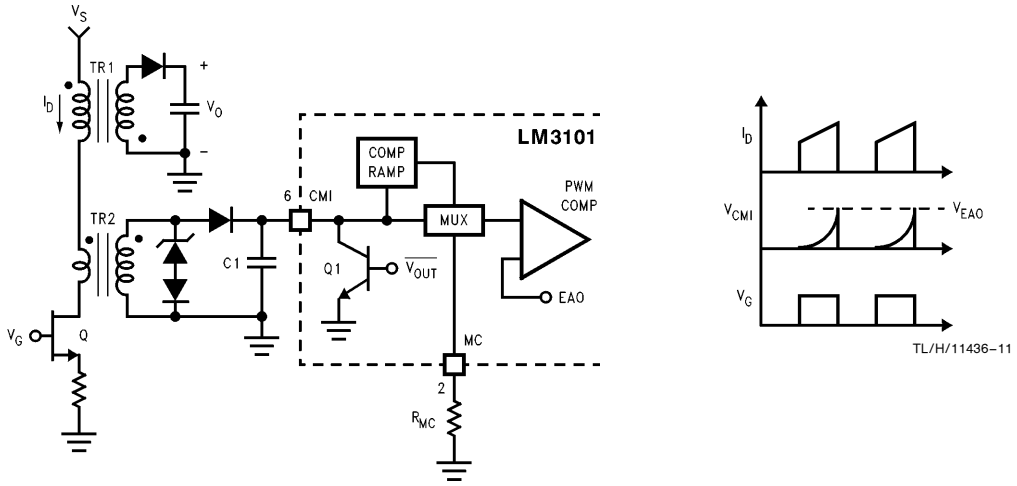

FIGURE 5. Charge Mode Operation

Functional Description (Continued)

Soft-Start Section

Soft-Start is accomplished by gradually increasing the reference voltage during start-up. The gradual increase is implemented by charging the Soft-Start capacitor, C_{SFST}, on pin 3 (the SFST pin). The charging current is set according to the following equation:

$$I_{SFST} = 0.45/R_T \qquad [A, \Omega].$$

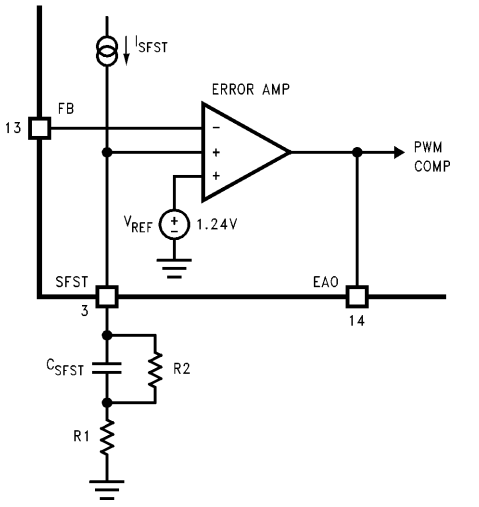

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FIGURE 6. Soft-Start Block Diagram

Typically, I_{SFST} starts to flow when the supply voltage is raised above 3V.

As shown in *Figure 6*, at the beginning of start-up, C_{SFST} is not charged up, and the SFST pin pulls down the reference voltage from its nominal value to:

$$V_{SFSTO} = I_{SFST} \bullet R_1 \qquad [V, A, \Omega].$$

V_{SFSTO} is designed to be 85% of the nominal reference voltage. The reference voltage rises smoothly from V_{SFSTO} to its nominal value as C_{SFST} charges up. When C_{SFST} charges up completely, the reference voltage is at its nominal value, start-up is over and steady-state operation begins.

The discharge time of C_{SFST} is set by the RC network as:

$$t_{DS} = 5 \bullet C_{SFST} \bullet R_2.$$

This is the time delay required to prepare the Soft-Start cycle after the LM3101 and the entire regulator has been turned off. R_2 must be large enough so that the final value of V_{SFST} is greater than the reference voltage:

$$V_{SFST} = I_{SFST} \bullet (R_1 + R_2) \geq 1.24V \qquad [V, A, \Omega].$$

Power Supply Monitor Functions

The LM3101 provides two monitor functions, a power-on reset flag with programmable delay, and a crowbar driver output for overvoltage conditions.

POWER-ON RESET

The power-on reset (POR) flag monitors the output voltage via the feedback pin (FB - pin 13). The POR flag will go low after the output voltage reaches 95% of its nominal value, and the subsequent programmed delay has passed. The POR flag pin (pin 11) is an open-collector pin which needs an external resistor to pull it up. This pin is valid with supply voltages as low as 1V while sinking 1.6 mA.

To program the reset delay, connect an external capacitor to the C_{RD} pin (pin 12). The practical range of delay is from 10 μs to 5 ms, and follows the equation:

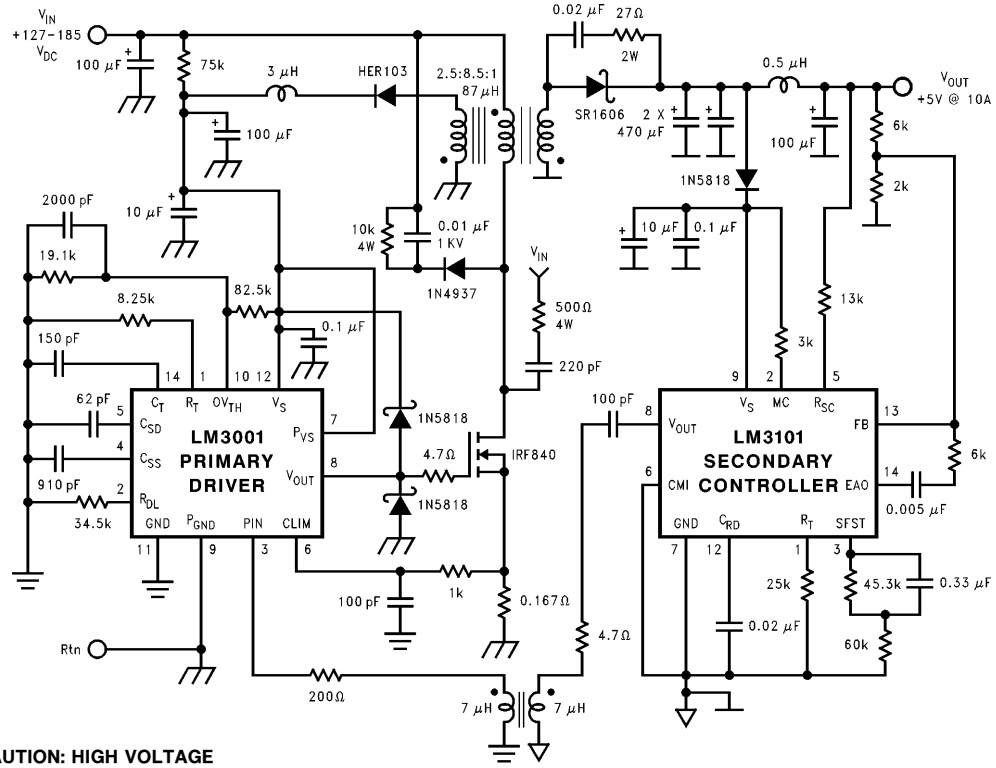
$$T_{RD} = C_{RD} \bullet 60 \bullet 10^3 \qquad [s, F].$$

For a power-on reset delay of 120 μs, the reset delay capacitor must be 0.002 μF.

CROWBAR DRIVER OUTPUT

The second monitor function is a crowbar driver output (CD–pin 10). If the output voltage gets higher than 120% of its nominal value, the CD pin can supply more than 200 mA to an external SCR trigger input. The SCR will fire, shorting the regulator output and saving the load circuitry from excessive supply voltage.

Typical Applications



CAUTION: HIGH VOLTAGE
Handle with Extreme Care

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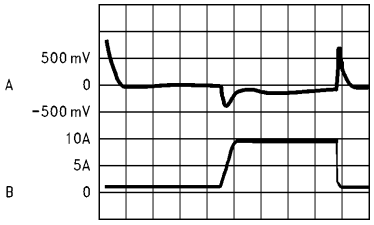
FIGURE 7. Offline Voltage Mode Flyback Regulator

This 500 kHz Offline Converter delivers 50W (5V @ 10A) from an input supply ranging from 90 VAC to 132 VAC (127 VDC to 185 VDC). The regulator achieves a line regulation of 0.06% and a load regulation of 0.05%. A 0.5 µH inductor and 100 µF capacitor form an LC filter that reduces the output ripple voltage to 50 mV. As shown in *Figure 8*, the regulator can respond to a ''step'' change in load current from 1A to 10A in about 12 µs. The efficiency of the converter is approximately 80% at full load.



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A: Output Voltage, 500 mV/div., AC Coupled
B: Load Current, 5A/div.
Horizontal Time Base: 20 µs/div.

FIGURE 8. Load Step Response

Typical Applications (Continued)

POWER STAGE OPERATION

The LM3001 Primary-Side PWM Driver sends a pulse-width-modulated signal (via pin 8) to a power switch, which in turn, drives a power transformer.

The power switch used in this case is an IRF840 Power MOSFET. It is an N-channel enhancement mode device that has a drain-to-source voltage (V_{DSS}) rating of 500V and a pulsed drain current (I_{DM}) rating of 32A. Even though the Power MOFSET has a high V_{DSS}, snubber circuits are needed to limit the drain voltage.

The power transformer has a primary inductance of 87 μH. The primary-to-secondary turns ratio is 8.5 to 1 and the secondary-to-tertiary turns ratio is 1 to 2.5. The tertiary winding delivers the LM3001 supply voltage (pins 7 and 12) to the primary-side driver.

There is an internal Overvoltage Threshold circuit (pin 10) monitoring the input voltage via a resistor divider. The overvoltage trip point is 3.3V typically. With the resistor values shown, the maximum supply voltage is approximately 17.5V.

The output rectifier, an SR1606, delivers the secondary current to the output. The SR1606 is specified for 16A forward current, 60V reverse breakdown voltage, and comes to a TO220-AB package. Since the SR1606 dissipates 7W to 8W at full load, it requires a heatsink. An RC snubber is placed in parallel to reduce the ringing voltage caused by the output rectifier turning off during the discontinous mode of operation.

Two Cornell Dubilier type 226 470 μF, 25V high frequency capacitors, with low ESRs of 0.25Ω, are used as the output capacitors.

OUTPUT VOLTAGE CONTROL

The output voltage is controlled by the LM3101 Secondary-Side PWM Controller. The LM3101 uses its error amplifier to compare the scaled-down output voltage against the internal precision 1.24V reference voltage. The error amplifier provides compensation for the regulator frequency response, by way of an RC feedback network.

The resulting error voltage is converted into a pulse-width-modulated waveform at the system oscillator frequency of approximately 500 kHz. This waveform is then differentiated (using an external high-pass RC filter) into a series of positive and negative pulses representing the desired switch duty cycle.

The pulses are transferred through a pulse transformer to the LM3001 Primary-Side Driver. The driver takes the feedback pulse signal and converts it into a PWM gate drive for the Power MOSFET.

FAULT RECOVERY OPERATION

A 0.167Ω resistor sets the peak primary current limits to 2.28A for the pulse-by-pulse limiting, and to 3.60A for the second-level limit. An RC network filters the current limit voltage to prevent the current limit (pin 6) from being activated by the reverse recovery spike of the output rectifier. When the second level current limit is triggered, the LM3001 shuts down and discharges the capacitor connected to pin 5 (the Shutdown Delay capacitor). After the capacitor is recharged to a voltage of approximately 2.1V, the device will try to restart. If the overcurrent condition persists, the device will shut down again.

The LM3101 provides the fault protection in case of an output short circuit. During normal operation, the operating frequency of this circuit is determined by a 25 kΩ resistor connected to pin 1 of the LM3101. However, during a short circuit condition on the output, the frequency of the LM3101 (and the entire circuit operating frequency) drops, yielding a very low duty cycle. This short-circuit frequency is set by the 13 kΩ resistor connected to pin 5.

The LM3101 Mode Control and Current Mode Input pins (pins 2 and 6 respectively) are for current mode control operation. The MC pin determines which control mode is being used—the resistor tied to the supply voltage means voltage mode control (the resistor tied to ground would indicate current mode control).

START-UP OPERATION

When power is initially applied to the regulator, the LM3001 Primary-Side PWM Driver receives its supply current through a 75 kΩ resistor connected to the input voltage (see *Figure 7*). Once the supply pin voltage reaches the threshold of 11.8V (typical), the LM3001 turns on, sending pulse signals (with an amplitude of approximately 10V) to the gate of the Power MOSFET. Because the output is driving Power MOSFETs, which need gate-to-source voltages greater than 10V for hard turn-on (low $R_{DS(ON)}$), the threshold voltage of 11.8V was selected to insure sufficient output voltage.

At the beginning of the start-up process, the secondary side of the regulator is still unbiased—hence the LM3001 does not receive a feedback signal from the secondary side (see the Start-up Sequence in *Figure 9*). Before the LM3101 Secondary-Side PWM Controller is controlling the circuit, the initial operating frequency of the gate drive is determined by the LM3001 internal oscillator. The oscillator uses an external capacitor and resistor, on pins 14 and 1 respectively. The initial operating frequency in this case is approximately 500 kHz. During this time, the regulator is operating in a ''free-running'' state.

Also during the start-up, the LM3001 executes Soft-Start by using the Soft-Start capacitor on pin 4. The voltage across this capacitor is compared to the oscillator ramp on pin 14 (see the LM3001 block diagram). In the offline regulator, the Soft-Start time is 15 μs approximately.

During this time, as the Soft-Start capacitor charges up, the duty cycle increases with each progressive cycle, until finally the duty cycle reaches its maximum value set by the Duty Cycle Limit circuit (R_{DL} - pin 2) or the Current Limit circuit (CLIM - pin 6). The Soft-Start phase ends when the duty cycle is limited by the R_{DL} circuit. A resistor at this pin connects to an internal current source which together will generate a voltage that will be compared to the oscillator ramp voltage. This comparison will determine the maximum duty cycle during this phase of the start-up cycle. For the circuit in *Figure 7*, the duty cycle is limited to 63% by the R_{DL} circuit.

Typical Applications (Continued)

The duty cycle will reach the R_{DL} limit for several cycles, letting energy build up in the transformer—see the drain current waveform in *Figure 9*. When the residual energy builds up enough, the duty cycle starts to decrease because it is now determined by the CLIM circuit. A voltage of 0.38V or greater at this pin will toggle a pulse-by-pulse comparator on every cycle (see the LM3001 block diagram). In the application circuit, a 0.167Ω resistor will generate the current limit threshold voltage when a 2.28A (peak) current flows through it. With the CLIM circuit in control of the duty cycle, the duty cycle will decrease with each successive cycle. The duty cycle will continue to shrink until the pulse feedback from the LM3101 takes control.

As the LM3001 switches the Power MOSFET on and off, the Power Transformer starts delivering power to the secondary side of the circuit. This action will cause the supply voltage of the LM3101 and the output voltage to gradually rise. When the supply voltage reaches the Undervoltage Lockout Threshold (of 3.9V), the LM3101 starts supplying a pulse train to the differentiator circuit on pin 8. The resulting PWM signals are fed back to the LM3001 via the pulse transformer. The first pulse signal to the LM3001 will cause it to disconnect its internal oscillator from its PWM and Output Driver circuits and trigger the Output Driver from the pulse feedback signals (of the LM3101). At this point, control of the frequency and the duty cycle changes from the LM3001 to the LM3101.

The LM3101 also exercises Soft-Start capability (pin 3). An RC network connected to this pin allows the LM3101 to gradually increase the duty cycle to its nominal value (in the example, the secondary Soft-Start time delay is 500 μs approximately).

The method of Soft-Start used by the LM3101 ensures that the error amplifier is in its linear region before the output voltage reaches its nominal value, thus yielding a smooth start-up of the output without any overshoot (see *Figure 10*).

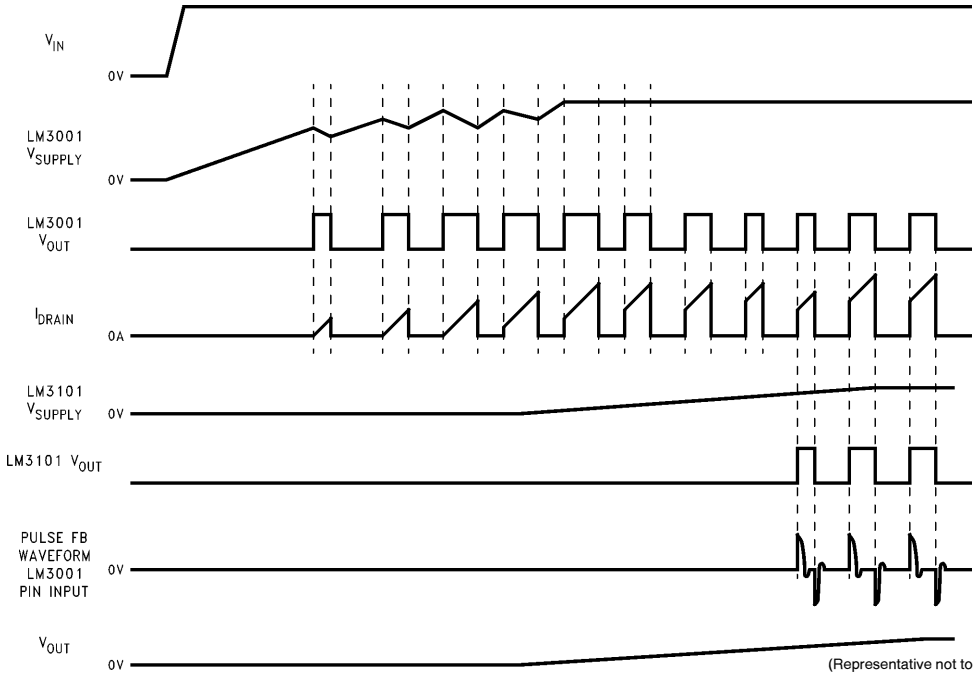

FIGURE 9. Start-Up Timing Sequence

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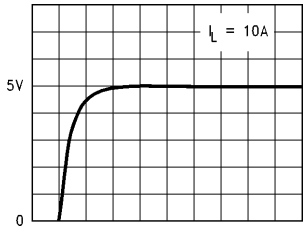
Typical Applications (Continued)



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Output Voltage, 1V/div.
Horizontal Time Base: 500 μs/div.

FIGURE 10. Output Voltage Start-up

At the end of the start-up sequence, the circuit is in steady-state or normal PWM operation.

Design Procedure

For the Offline Voltage Mode Flyback Regulator (*Figure 7*), the specifications for the power transformer, MOSFET switch, the switch snubber, and the output rectifier can be calculated based on the system specifications:

System specifications:

V_O = 5 VDC
V_I Range = 90 VAC–132 VAC
I_O Range = 0.5A–10A
Efficiency (η) ≈ 80%
F_O = 500 kHz.

TRANSFORMER SPECIFICATIONS

Manipulating the transfer function of a flyback regulator results in a calculation for the turns ratio of the power transformer, involving the minimum input voltage, the output voltage, and the maximum duty cycle (D):

$$V_O + V_F = (V_{IN(MIN)} - V_{SW(ON)}) \bullet (N_S/N_P) \bullet (D_{(MAX)}/(1-D_{(MAX)}))$$

$$\downarrow$$

$$N_S/N_P = [(V_O + V_F)/(V_{IN(MIN)} - V_{SW(ON)})] \bullet ((1-D_{(MAX)})/D_{(MAX)})$$

Assume that the diode forward voltage (V_F) is about 0.7V and the drain-to-source voltage when the switch is on ($V_{SW(ON)}$) is approximately 0.9V. Selecting a 28% maximum duty cycle results in a turns ratio of:

$$N_S/N_P = (5.7V/126.1V) \bullet (1-0.28)/0.28 = 0.12$$

$$(N_P/N_S = 8.5/1).$$

Assuming an efficiency (η) of 80%, the average input current (at the maximum load current and for the entire period) is:

$$I_{IN} = (V_O)\,(I_O)/\,(V_{IN(MIN)} \bullet \eta) = (50W)/(127V \bullet 0.80) = 0.49A.$$

The average current when the switch is on is the average current over the entire period divided by the duty cycle:

$$I_{IN(TON)} = I_{IN}/D = (0.49A)/(0.28) = 1.77A.$$

Selecting the primary inductance ripple current (ΔI_P) to be a certain percentage of $I_{IN(TON)}$, and combining that with the duty cycle, input voltage, and operating frequency, gives the primary inductance by the equation:

$$L_P = (V_{IN(MIN)} - V_{SW(ON)}) \bullet D_{(MAX)}/\,(\Delta I_P \bullet F_O)$$

Assuming the percentage to be 46% in the example, then:

$$L_P = 126.1V \bullet 0.28/(0.81A \bullet 500\ kHz) \cong 87\ \mu H.$$

MOSFET PARAMETERS

The peak current through the primary inductance and the Power MOSFET is the average current when the switch is on plus one-half the primary inductance ripple current:

$$I_{PRI(PK)} = I_{IN(TON)} + (\Delta I_P/2) = 1.77A + (0.81A/2) = 2.18A$$

Assuming ideal conditions, the maximum voltage at the drain of the Power MOSFET when the switch is off is:

$$V_{SW(OFF)} = (V_O + V_F)\,(N_P/N_S) + V_{IN(MAX)} = (5.7V)\,(8.5) + 185V = 233V \longrightarrow 250V.$$

However, leakage inductance exists in the transformer, causing a voltage spike immediately after the switch turns off. This voltage spike will add to the rest of the drain voltages, making $V_{SW(OFF)}$ even greater. With a leakage inductance that is 2% of the transformer primary inductance and selecting a switch which has a fall time of 2% the total off-time, the added voltage will be:

$$V_{LL} = 2\% \bullet L_P \bullet I_{PRI(PK)} \bullet F_O/[2\% \bullet (1-D_{(MAX)})].$$

The maximum duty cycle of 28% is used for worst case purposes. Thus, the leakage inductance voltage spike is:

$$V_{LL} = 0.02 \bullet 87\ \mu H \bullet 2.18A \bullet 500\ kHz/[0.02 \bullet (1-0.28)] = 130V \longrightarrow 150V.$$

This means the actual peak drain voltage is approximately 400V. When choosing the Power MOSFET, add some margin to this number. A 500V MOSFET was used in this application.

SNUBBER DESIGN

A ''snubber'' circuit, consisting of a 1N4937 fast recovery diode and a parallel RC network, is inserted around the transformer primary to clamp the voltage spike. This is to reduce the switch voltage stress when it is off. The ''snubber'' components are calculated in the following manner:

$$C_{SN} \geq 0.02 \bullet L_P \bullet I_{P(PK)}{}^2/(V_{MAX}{}^2 - V_{SN}{}^2) = 0.02 \bullet 87\ \mu H \bullet (2.18A)^2/[(255V)^2 - (250V)^2] \cong 3.3\ nF$$

and

$$R_{SN} \leq [(V_{MAX} + V_{SN} - V_{IN})/2]^2 \bullet [100/(F_O \bullet L_P \bullet I_{P(PK)}{}^2)] = [(255V + 250V - 185V)/2]^2 \bullet [100/(500\ kHz \bullet 87\ \mu H \bullet (2.18A)^2)] \cong 12\ k\Omega.$$

In the Offline Flyback Regulator application, a 0.01 μF capacitor and a 10 kΩ resistor are used as the snubber components. V_{MAX} is the selected maximum voltage at the drain of the MOSFET. Usually the RC values are selected so that V_{MAX} is 5V to 10V higher than V_{SN}. The power dissipation of the resistor is:

$$P = [(V_{MAX} + V_{SN} - V_{IN})/2]^2/R = [(255V + 250V - 185V)/2]^2/10\ k\Omega = 2.56W.$$

To add some margin, a 4W resistor is chosen.

The fast recovery diode must have a reverse voltage rating greater than V_{MAX}. The 1N4937 has a 600V rating.

OUTPUT DIODE PARAMETERS

The peak secondary current can be calculated using the peak primary current and the turns ratio (this equation is for single output flyback regulators):

$$I_{SEC(PK)} = I_{PRI(PK)} \bullet (N_P/N_S) = 2.18A \bullet 8.5 = 18.43A \longrightarrow 20A.$$

Typical Applications (Continued)

The maximum average current through the secondary and the diode, when the switch is off, is the maximum load current divided by the inverse of the duty cycle:

$$I_{SEC(OFF)} = I_{LOAD}/(1-D_{(MAX)}) = 10A/0.72 = 13.90A \approx 15A.$$

The maximum average secondary current for the entire period is the maximum load current (10A).

The maximum reverse-bias voltage on the output rectifier is:

$$V_{RV} = V_{IN(MAX)} \bullet (N_S/N_P) + V_O + V_F = (185V)\,(1/8.5) + 5.7V = 27.47V \approx 30V.$$

A suitable diode for this circuit is the SR1606, which has a reverse voltage rating of 60V and an average current rating of 16A.

Telecom Converter

The schematic of a flyback regulator, used in Telecom applications, is shown in *Figure 11*. The circuit has many of the component values that are in the offline converter. Notable exceptions are the power transformer, in which the turns ratio and primary inductance has changed (due to the change in the input voltage range), and the Power MOSFET, which has a lower on-resistance and a lower breakdown voltage rating.

The most significant difference in the circuit design is the change in the mode of operation—from voltage mode to current mode. For current mode operation, the LM3101 Mode Control pin (MC−pin 2) is connected to ground by a 6 kΩ resistor, and the Control Mode pin (CMI− pin 6) is connected to the current sense transformer through a half-wave rectifier circuit and a low-pass filter. The filter is needed to remove the leading edge spike on the current waveform, caused by the rectifier recovery and interwinding capacitance of the power transformer.

Smaller component differences include reducing the current sensing resistor in the primary side ground path (to allow for the larger primary current), and removing a primary side snubber circuit (due to smaller peak voltages at the drain). Also, the output rectifier and Power MOSFET snubbers are modified.

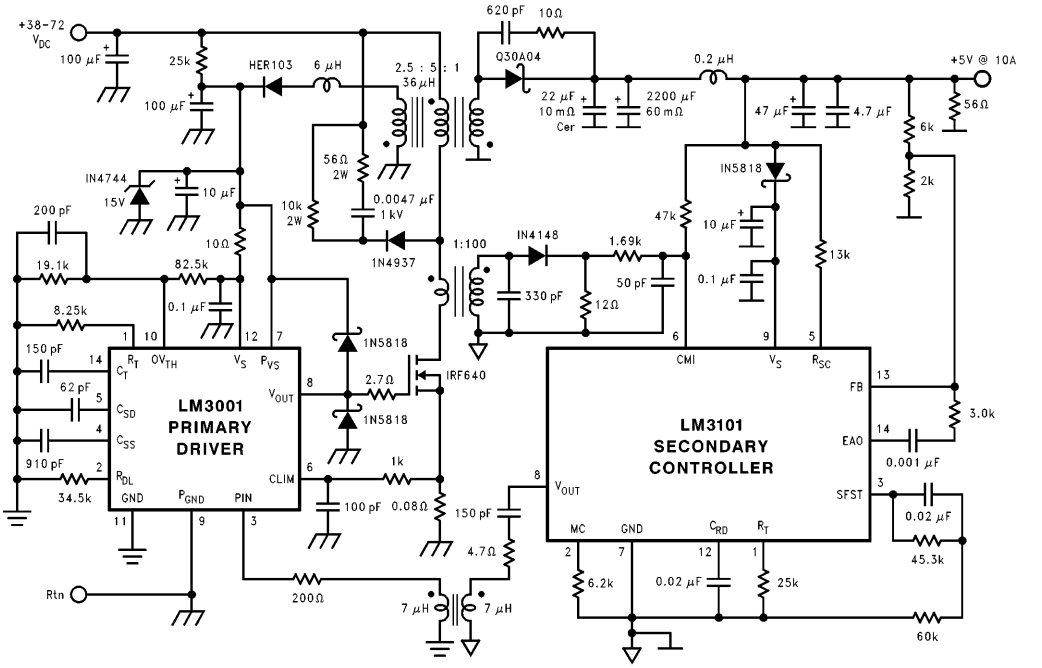

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FIGURE 11. Telecom Current Mode Flyback Regulator

Application Hints

Pulse Feedback Section

During steady-state operation, the LM3101 delivers pulse-width modulated signals to the feedback circuit. The feedback circuit will convert that signal into a series of AC-coupled pulse signals and apply them to the LM3001 via the pulse transformer (the first positive-edged pulse from the LM3101 will cause the LM3001 to disconnect its internal oscillator from its PWM and Output Driver circuits). The feedback pulses will trigger the LM3001 Output Driver to apply PWM drive signals to the Power MOSFET gate. The timing diagram in *Figure 12* demonstrates the feedback communication.

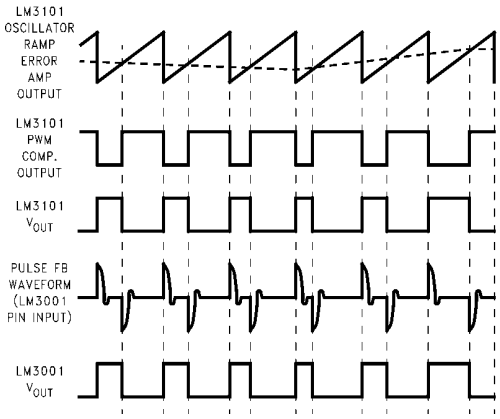


FIGURE 12. Pulse Feedback Timing Diagram

Pulse Interface Circuit

The pulse interface circuit provides isolation for the feedback circuit of the Offline Flyback Regulator. The differentiator circuit converts the PWM waveform into a pulse train. The differentiator delivers a train of $1V_{PK}$, 15 ns wide pulses to the pulse transformer. The core should have high permeability (typically 10,000) at the switching frequency to allow the transfer of energy with a very small transformer (size). This one-to-one transformer transfers the pulse train to the LM3001 via a 200Ω resistor, which is used mainly to filter noise from the system.

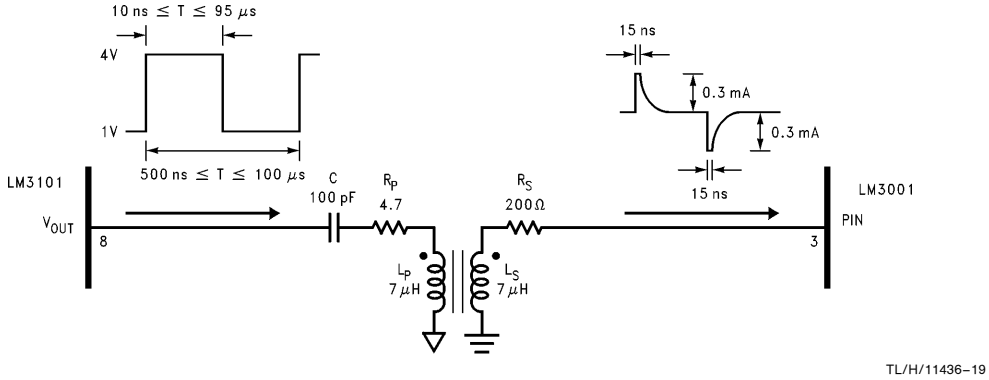
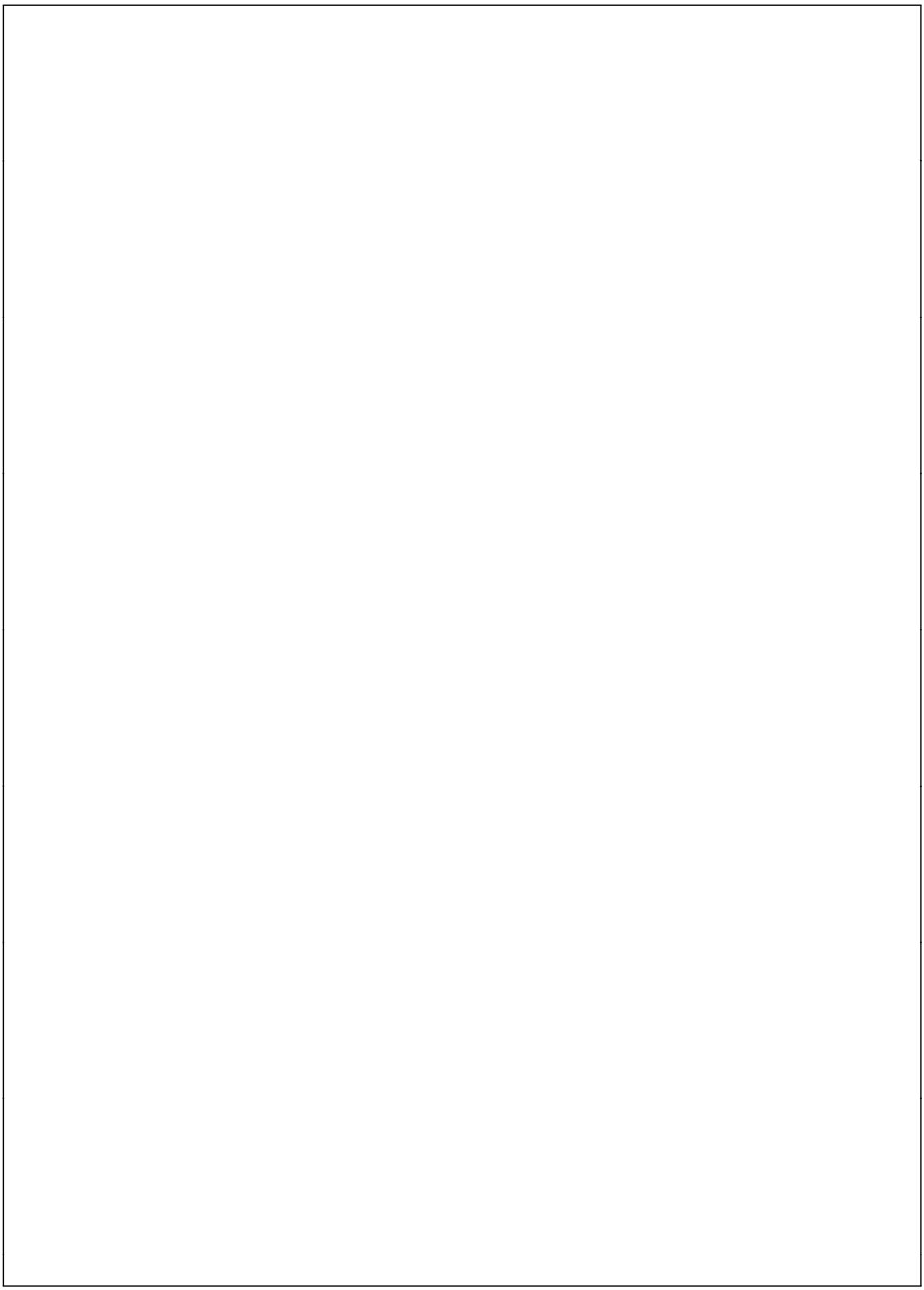
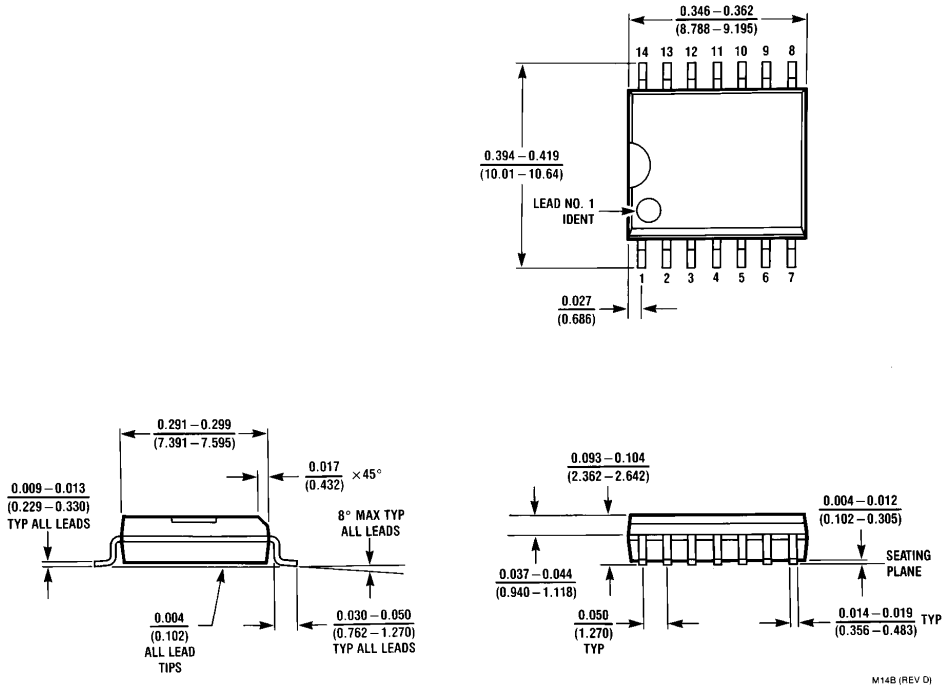


FIGURE 13. Pulse Interface Circuit

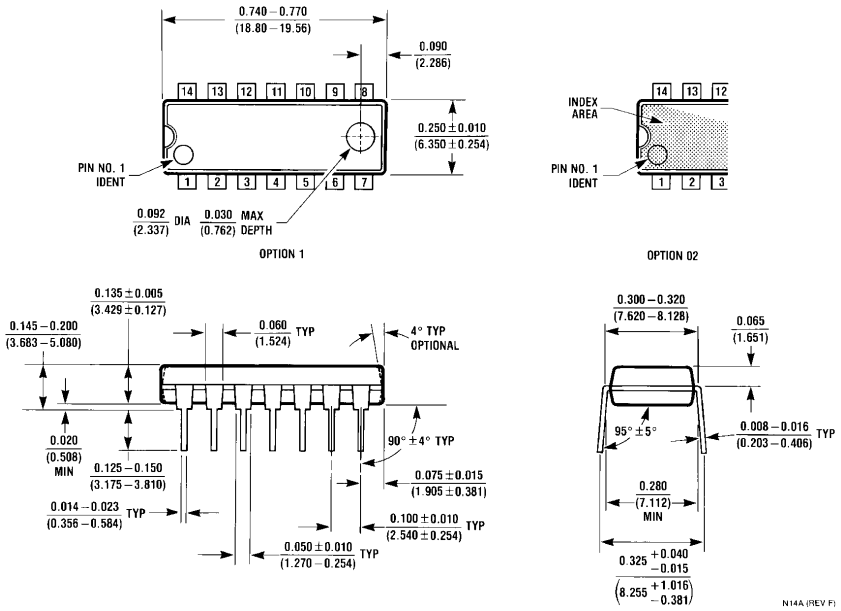


Physical Dimensions inches (millimeters)



14-Lead Package
For Surface Mount Package
Order Number LM3101M
NS Package Number M14B

Physical Dimensions inches (millimeters) (Continued)



For DIP Package
Order Number LM3101N
NS Package Number N14A

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