National Semiconductor

November 1992

NM95C12 1K-Bit CMOS EEPROM with Programmable Switches

General Description

The NM95C12 is a 976-bit, CMOS EEPROM with 8 non-volatile programmable outputs that can be used as DIP switches in both analog and digital modes. The 976 bits of memory are divided into 61 registers of 16 bits each and each register can be individually accessed. Registers 61–63 are dedicated to storing the switch settings.

In addition to the 976 bits of EEPROM memory, the NM95C12 contains eight individually programmable outputs which can be used as switches and two additional registers used in conjunction with the switch logic which are volatile. Each switch output may be programmed to provide either a High or Low level. These outputs may also be programmed to form four individual pairs of SPST switches.

The switch configuration information is obtained from a non volatile register whenever power is first applied to the device. This ensures the switches will always have a user determined state upon power-up.

Features

- 8 DIP switch positions or 4 SPST switch positions
- Digital and analog switch functions
- 976 bits of CMOS EEPROM memory available
- 4 mA (max) operating current, 50 μA (max) standby current
- Software write protection
- Serial I/O interface fully MICROWIRE compatible
- Single +5V ±10% operation
- 40 year data retention
- Endurance: 10^6 data changes
- Reliable floating gate technology
- Sequential register read
- Self-timed write cycle
- No erase required before write
- Compatible with COPS™ microcontrollers
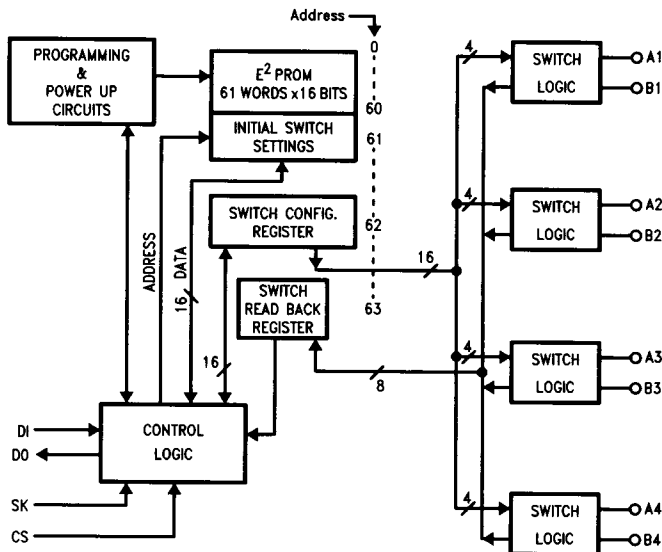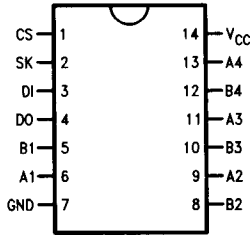- Packages available: 14-pin DIP, 14-pin SO
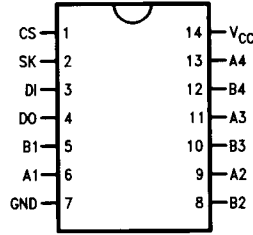
Block Diagram

FIGURE 1. Block Diagram

TL/D/9632–1

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COPS™ microcontrollers is a trademark of National Semiconductor Corporation.

Connection Diagrams

SO Package

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       _____
CS  —|1      14|— V_CC
SK  —|2      13|— A4
DI  —|3      12|— B4
DO  —|4      11|— A3
B1  —|5      10|— B3
A1  —|6       9|— A2
GND —|7       8|— B2
       _____
```

TL/D/9632-3

Top View
Order Number NM95C12M,
NM95C12EM and NM95C12MM
See NS Package M14A

Dual-In-Line Package

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       _____
CS  —|1      14|— V_CC
SK  —|2      13|— A4
DI  —|3      12|— B4
DO  —|4      11|— A3
B1  —|5      10|— B3
A1  —|6       9|— A2
GND —|7       8|— B2
       _____
```

TL/D/9632-2

Top View
Order Number NM95C12N,
NM95C12EN and NM95C12MN
See NS Package N14A

Pin Names

CS	Chip Select
SK	Serial Clock
DI	Serial Data In
DO	Serial Data Out
A1–A4	Switch Terminals
B1–B4	Switch Terminals

Pin Descriptions

Pin Name	Description
CS	Chip Select, Input—This input must be high while communicating with the NM95C12. When this input is LOW, the chip is powered down into the standby mode. It should be noted that the CS does not control the A1 through A4 and B1 through B4 outputs and hence has no effect on them. The CS input must be made LOW after completing an instruction to prepare the control logic to accept the next instruction. If the CS input becomes LOW prematurely, the operation in progress is aborted. If programming the E^2 memory is in progress and the CS goes LOW, the programming is not aborted but will proceed to its normal completion.
SK	Serial Clock, Input—This input is used for clocking the serial I/O. The CS input must be high for clocking to have any effect. Information presented on the DI input will be shifted into the device on the LOW to HIGH transition of the clock. Information from the device will be available on the DO output serially, in response to the LOW to HIGH transition of the clock.
DI	Serial Data In, Input—All information needed for the operation of the device is entered serially from this input. HIGH represents logic '1' and LOW represents logic '0'. The entry order is most significant bit first and least significant bit last.
DO	Serial Data Out, Output, 3-state—When data is read, data from the addressed location will be available on this output serially, in sync with the LOW to HIGH transitions on the SK input. Normally the DO pin is in high impedance state. During a read instruction, when the last bit of the address is shifted in, the DO will go LOW indicating that data will follow. The data will follow in response to the clock transitions. The data will come out most significant bit first and least significant bit last. During E^2 programming operations, this output is also used as the status indicator. During programming operations, LOW indicates Busy (programming in progress) and HIGH indicates Ready. The DO output will be in the high impedance state if the CS input is LOW unconditionally.
A1–A4 B1–B4	Switch Terminals—These pins provide the simulated DIP switch features and hence are called terminals. The behavior of these pins is determined by the settings in the Switch Configuration Register and are independent of the CS input.
V_CC	+5V Power Supply.
GND	Ground.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC}	6.5V
Voltage at Any Pin	-0.3 to $+6.5V$
Storage Temperature Range	$-65°C$ to $+150°C$
Maximum Power Dissipation @25°C	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature

NM95C12	0°C to $+70°C$
NM95C12E	$-40°C$ to $+85°C$
NM95C12M*	$-55°C$ to $+125°C$
Power Supply Voltage (V_{CC})	4.5V to 5.5V

*Contact factory for availability

DC Electrical Characteristics $V_{CC} = 5V \pm 10\%$

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	$C_S = V_{IH}$, SK = 1 MHz		4	mA
I_{CC2}	Operating Current TTL Input Levels	$C_S = V_{IH}$, SK = 1 MHz		6	mA
I_{CC3}	Standby Current CMOS Input Levels on Switches	$C_S = 0V$		50	μA
I_{CC4}	Standby Current TTL Input Levels on Switches	$C_S = 0V$		800	μA
I_{iL}	Input Leakage	$V_{IN} = 0V$ to V_{CC}	-2.5	$+2.5$	μA
I_{oL}	Output Leakage	$V_{OUT} = 0V$ to V_{CC}	-2.5	2.5	μA
V_{IL}	Input Low Voltage		-0.1	0.8	V
V_{IH}	Input High Voltage		2.0	$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA		0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -400 \mu A$	2.4		V
R_{ON}	Switch On Resistance			200	Ω
R_{OFF}	Switch Off Resistance		10		$M\Omega$
V_S	Maximum Voltage Allowed on any Switch Terminal			$V_{CC} + 1$	V
I_S	Max Current Allowed through Switch Terminals			10	mA

AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$ unless otherwise specified

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
f_{SK}	SK Clock Frequency	NM95C12 NM95C12E NM95C12M		0 0 0	1 1 0.5	MHz
t_{SKH}	SK High Time	NM95C12 NM95C12E NM95C12M	(Note 2) (Note 2) (Note 3)	250 300 500		ns
t_{SKL}	SK Low Time	NM95C12 NM95C12E NM95C12M	(Note 2) (Note 2) (Note 3)	250 250 500		ns
t_{SKS}	SK Setup	NM95C12 NM95C12E NM95C12M		50 50 100		ns ns ns
t_{CS}	Minimum CS Low Time	NM95C12 NM95C12E NM95C12M	(Note 4) (Note 4) (Note 5)	250 250 500		ns
t_{CSS}	CS Setup Time	NM95C12 NM95C12E NM95C12M	Relative to SK	50 50 100		ns

AC Electrical Characteristics V_{CC} = 5V ±10% unless otherwise specified (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{PUSR}	Power Up Slew Rate			1		ms
t_{DIS}	DI Setup Time	NM95C12 NM95C12E NM95C12M	Relative to SK	100 100 200		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time		Relative to SK	20		ns
t_{PD1}	Output Delay to "1"	NM95C12 NM95C12E NM95C12M	AC Test		500 500 1000	ns
t_{PD0}	Output Delay to "0"	NM95C12 NM95C12E NM95C12M	AC Test		500 500 1000	ns
t_{SV}	CS to Status Valid	NM95C12 NM95C12E NM95C12M	AC Test		500 500 1000	ns
t_{DF}	CS to DO in TRI-STATE®	NM95C12 NM95C12E NM95C12M	CS = V_{IL} AC Test		100 100 200	ns
t_{ISWD}	Switch Delay from Switch Input	NM95C12 NM95C12E NM95C12M	AC Test		250 250 500	ns
t_{SWPD0}	Switch Delay to 0 from Config. Change	NM95C12 NM95C12E NM95C12M	AC Test		500 500 1000	ns
t_{SWPD1}	Switch Delay to 1 from Config. Change	NM95C12 NM95C12E NM95C12M	AC Test		500 500 1000	ns
t_{SWS}	A1–A4, B1–B4 Setup Time for SRR Read	NM95C12 NM95C12E NM95C12M		100 100 200		ns
t_{SWH}	A1–A4, B1–B4 Hold Time for SRR Read	NM95C12 NM95C12E NM95C12M		100 100 200		ns
t_{WP}	Write Cycle Time				10	ms
t_{DH}	DO Hold Time		Relative to SK	10		ns

Capacitance (Note 6)
T_A = 25°C, f = 1 MHz

Symbol	Test	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IN}	Input Capacitance	5	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", the device should not be operated at these limits. The table of "Electrical Characteristics" provides actual operating limits.

Note 2: The SK frequency specification for Commercial and Extended temperature range parts specifies a minimum SK clock period of 1 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 1 μs. For example, if t_{SKL} = 250 ns, then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Military parts specifies a minimum SK clock period of 2 μs; therefore, in an SK clock cycle t_{SKH} + t_{SKL} must be greater than or equal to 2 μs. For example, if t_{SKL} = 500 ns, then the minimum t_{SKH} = 1.5 μs in order to meet the SK frequency specification.

Note 4: For Commercial and Extended temperature range parts, CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Military parts, CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Note 7: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from +65°C to +85°C.

Functional Description

Figure 1 is a block diagram of the NM95C12. It consists of a 62-word X 16-bit E²PROM array, a 16-bit Switch Configuration Register (SCR), a 16-bit Switch Readback Register (SRR), four identical blocks of switch logic, programming and power-up circuits and the necessary control logic. It may be noted that only eight bit positions of the SRR are used in the NM95C12.

ADDRESS SPACE

Registers 0–60 of the E²PROM are available to the user as general purpose non-volatile memory. Data may be read or programmed into this memory using the appropriate instructions. Address location 61 is an E² location which also can be read or programmed like any other E² location. However, address 61 is used in the NM95C12 to provide the initial switch configuration information automatically on power-up.

The SCR is located at address 62. The SCR is not an E² location and hence is volatile. It does not have endurance limits or programming time requirements associated with it, allowing the switches to be reconfigured an unlimited number of times.

The SCR is automatically loaded from address 61 on power-up. The SCR controls the switch logic and hence the behavior of the terminals A1 through A4 and B1 through B4.

Located at address 63 is the Switch Readback Register (SRR). This is a read only register.

TABLE I. Switch Configurations

MODE*	Z	Y	X	W	SWITCH CONFIGURATION	COMMENTS
0	0	0	0	0		A = 0 , B = 0
1	0	0	0	1		A = 0 , B = 1
2	0	0	1	0		A = 1 , B = 0
3	0	0	1	1		A = 1 , B = 1
4	0	1	0	0		A = 0 , B = TRI-STATE
5	0	1	0	1		A = B
6	0	1	1	0		A = $\bar{B}$
7	0	1	1	1		A = 1 , B = TRI-STATE
8	1	0	0	0		A = TRI-STATE , B = 0
9	1	0	0	1		B = A
10	1	0	1	0		B = $\bar{A}$
11	1	0	1	1		A = TRI-STATE , B = 1
12	1	1	0	X		Analog Switch Open
13	1	1	1	X		Analog Switch Closed

*Modes 0 thru 11 are logic level functions. Modes 12 and 13 are Analog switch functions.

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Functional Description (Continued)

SWITCH CONFIGURATIONS

The 16-bit SCR format is shown in *Figure 2*. It consists of four 4-bit fields. Each field controls its corresponding switch control logic. The individual bits in each field are labelled W, X, Y, and Z. Table I shows the relationship between these bit values and the resulting behavior of the terminals. It should be remembered that the CS input has no effect on the behavior of the terminals.
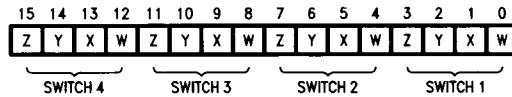
SWITCH READBACK REGISTER

The SRR allows the current logic level present at the switch terminals to be read back via the Microwire bus. The SRR is loaded by the rising edge of SK immediately after the last instruction bit is clocked in (The same clock edge that loads A0). The SRR is loaded on this clock edge only when register 63 (Switch Readback Register) is being read. In the case of switch mode 13 (Analog switch mode), the SRR will not report the actual levels present at the terminals due to this mode being analog levels. In mode 13, bits 15–8 of the SRR will be all 0's to indicate a closed analog switch. This is done to avoid ambiguous logic levels which could exist when the device is used in the analog switch mode.

The bit assignments and conceptual function of the SRR is shown in *Figure 3*. As shown, only bits 15 thru 8 are used, and bits 7 thru 0 are always read as logical 0. The SRR is a Read-Only register and if it is written, the device will not perform a write or generate a Ready/Busy status. The SRR is not implemented in EEPROM, allowing an infinite number of cycles in the register.

INSTRUCTION SET

The NM95C12 instruction set contains five instructions, and each instruction is ten bits long. The first 2 bits of the instruction are the start bits (SB) and are always a logical "01", followed by the op code (2 bits) and the address field (6 bits). The WRITE and WRALL instructions are followed by sixteen bits of data (D15–D0) which is written into the memory. Table II is a list of the instructions and their format.

FIGURE 2. Switch Configuration Register (SCR)
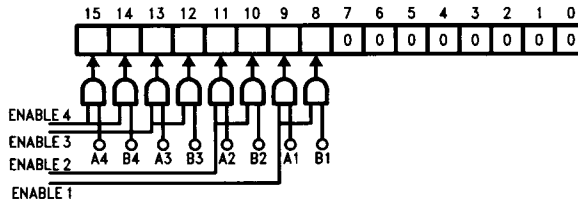
TL/D/9632–4

FIGURE 3. Switch Readback Register (SRR)

TL/D/9632–5

TABLE II. NM95C12 Instructions

Instruction	SB	Op Code	Address	Data	Comments
READ	01	10	A5–A0		Reads data stored in memory, starting at specified address.
WEN	01	00	11XXXX		Write enable must precede all programming modes.
WRITE	01	01	A5–A0	D15–D0	Writes register.
WRALL	01	00	01XXXX	D15–D0	Writes all registers.
WDS	01	00	00XXXX		Disables all programming instructions.

Functional Description (Continued)

WDS (Write Disable): When this instruction is issued, all subsequent writing into the NM95C12 is locked out. Any attempt to write into a locked device is ignored. The NM95C12 powers up in the locked state. The WEN is the only instruction that unlocks the device. The write disable operation has no effect on read operations. Thus reading will occur normally even from a locked device.

WRALL (Write All): When this instruction is executed, the NM95C12 bulk-programs the same 16-bit data pattern into all of its E^2 memory locations (address 0 through 61). The SCR is unaffected since it is not an E^2 location. The data pattern must follow immediately after the last bit of this instruction. The chip enters into the self-timed program mode after CS is brought low, before the next rising edge of SK.

WEN (Write Enable): This instruction is used to unlock the write circuits. The circuits will remain unlocked until the WDS instruction locks them. The NM95C12 powers up in the locked state and hence WEN must be executed prior to any programming instructions.

WRITE (Write/Program): This instruction writes a 16-bit data word into the address location specified by the A_0–A_5 bits of the instruction. The 16 data bits must follow the last bit of the instruction. After loading the WRITE instruction and the 16-bit data, the chip enters into the self-timed program mode when CS is brought low before the next rising edge of the SK clock. If the addressed location is the SCR, then the chip does not enter into the self-timed E^2 programming mode (the SCR is not an E^2 location) but loads the switch configuration data into the SCR. The WRITE instruction can only be aborted by deselecting the chip (CS LOW) before entering all the instruction bits. The NM95C12 does not require erasing prior to writing.

READ (Read): This instruction reads the data from the addressed location. As before, the instruction also contains the address. The data will come out serially on the DO output on the rising edge of the clock. A logical '0' precedes the 16-bit data (dummy bit).

The NM95C12 has a convenient feature called sequential register read. Normally, the CS input is made LOW after the last data bit is shifted out. However, if the CS input is left HIGH and clocking continues, data from the next address location will be delivered on the DO pin. This sequential read can continue indefinitely whereby the address is automatically incremented after delivering 16 bits of data. It should be noted that in the sequential register read mode, address wrap-around will occur.

During a sequential register read there will be a dummy bit preceding the first word read, after which, the bit stream will be continuous without any dummy bits separating the data words.

Ready/Busy Indication

Programming an E^2 memory takes several milliseconds. Unlike some devices which require the user to keep track of the elapsed time to ensure completion of the programming cycle, the NM95C12 contains an on-chip timer. The timer starts when the CS input goes LOW after the last data bit is entered. After entering a programming cycle (CS forced LOW), the timer status may be observed by forcing the CS input back HIGH. The timer status is available on the DO pin if the CS input is forced HIGH within one ms of starting the programming cycle. LOW on the DO pin indicates that the programming is still in progress while HIGH indicates the device is READY for the next instruction. It should be noted that if the CS input is made HIGH for status observation, it must be made LOW when READY is indicated before loading the next instruction.

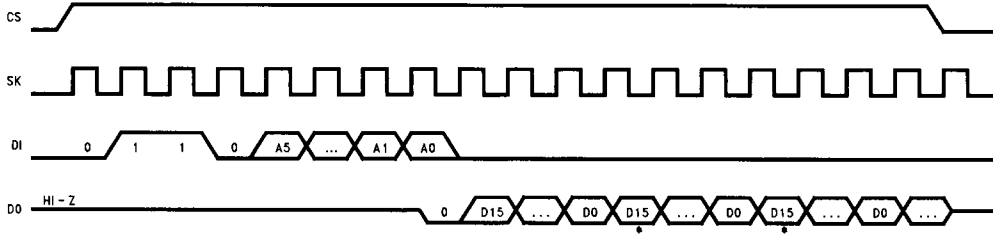## Timing Diagrams

Synchronous Data Timing
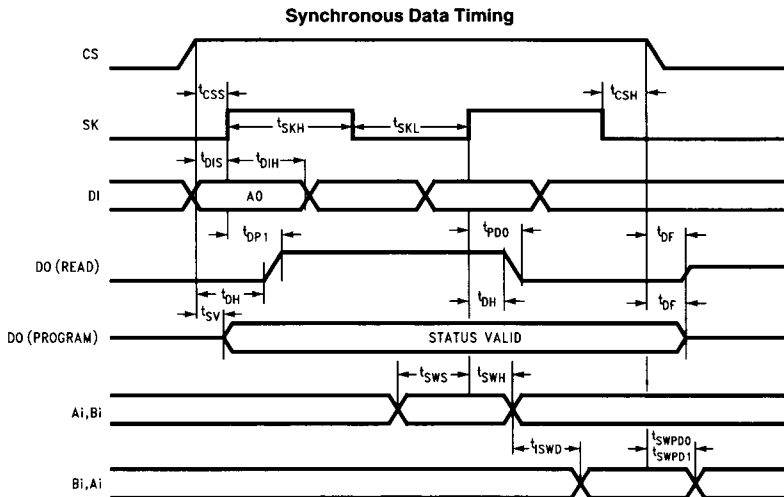
TL/D/9632–7

*This is the minimum SK period (Note 2).

††t_{SKS} is not needed if DI = V_{IL} when CS is going active (HIGH).
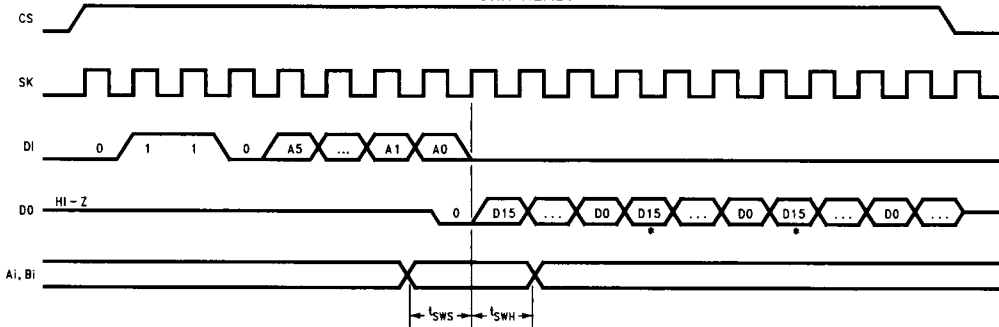
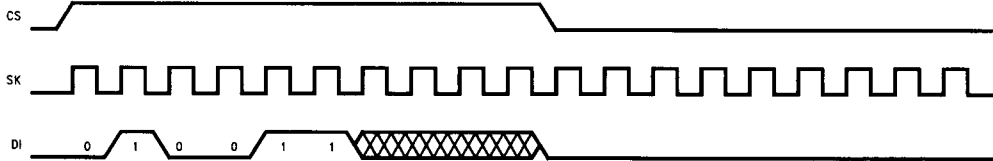# Timing Diagrams (Continued)

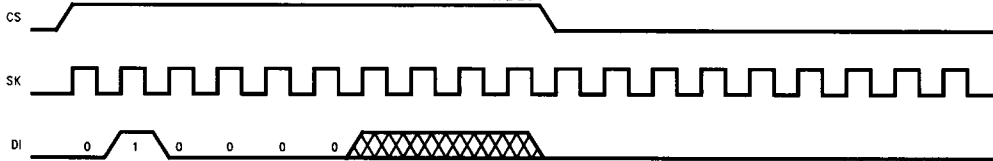## Instruction Sequence

READ:

TL/D/9632–8

SRR READ:

$\leftarrow t_{SWS} \rightarrow \leftarrow t_{SWH} \rightarrow$

TL/D/9632–14

WEN:

TL/D/9632–9

WDS:
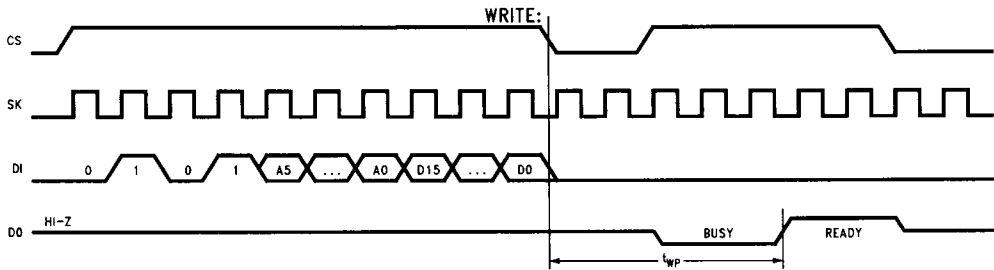

TL/D/9632–10

*The memory automatically cycles to the next register.
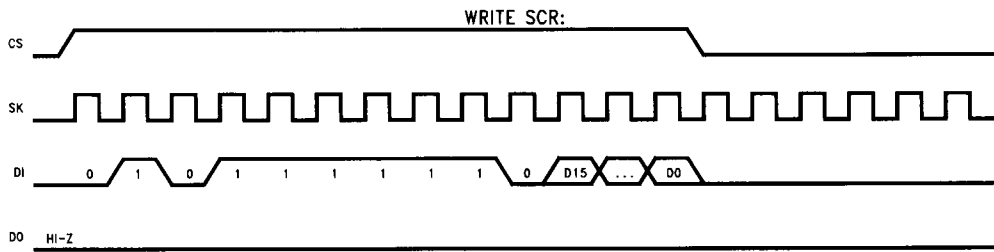
Timing Diagrams (Continued)
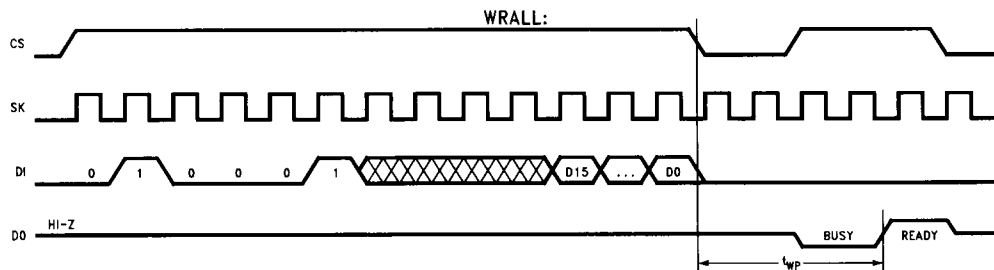
Instruction Sequence (Continued)

WRITE:
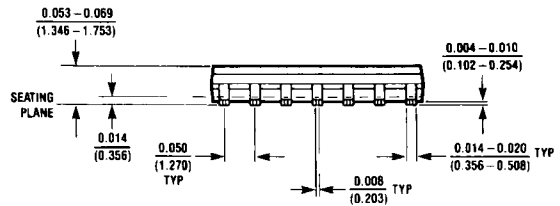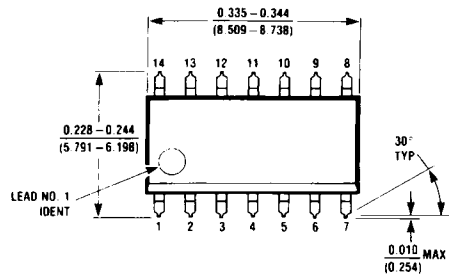
CS

SK

DI   0   1   0   1   A5 ⟩⟨ ... ⟩⟨ A0 ⟩⟨ D15 ⟩⟨ ... ⟩⟨ D0

DO   HI–Z   BUSY   READY

t_{WP}

TL/D/9632–11

WRITE SCR:

CS

SK

DI   0   1   0   1   1   1   1   1   1   0 ⟨ D15 ⟩⟨ ... ⟩⟨ D0 ⟩

DO   HI–Z

TL/D/9632–12

WRALL:

CS

SK

DI   0   1   0   0   0   1 ⟨XXXXXXXXX⟩⟨ D15 ⟩⟨ ... ⟩⟨ D0

DO   HI–Z   BUSY   READY

t_{WP}

TL/D/9632–13

9

Physical Dimensions inches (millimeters)
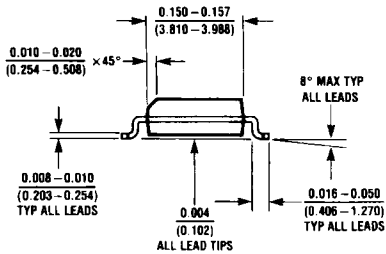
Molded Package Small Outline (M)
Order Number NM95C12M,
NM95C12EM or NM95C12MM
NS Package Number M14A

Physical Dimensions inches (millimeters) (Continued)
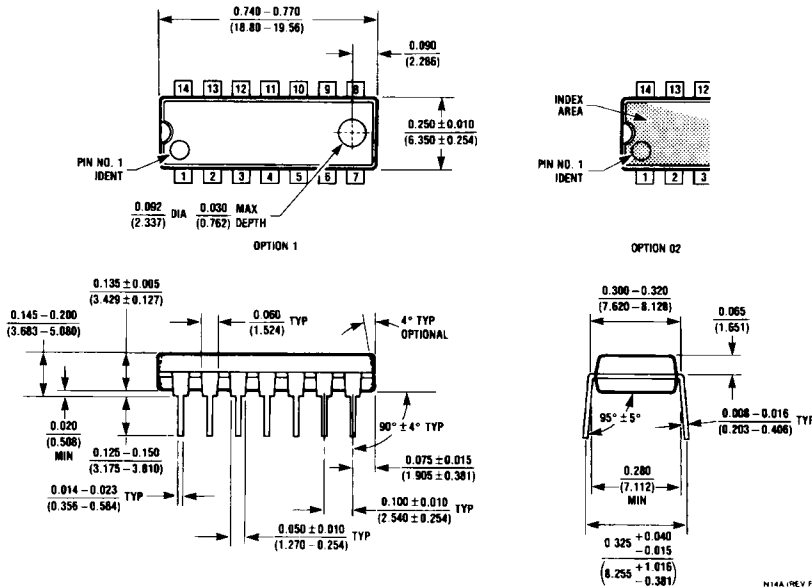
Molded Dual-In-Line Package (N)
Order Number NM95C12N,
NM95C12EN or NM95C12MN
NS Package Number N14A

LIFE SUPPORT POLICY