

Octal Bus Buffer/Line Driver Inverting with 3-State Outputs

The MC74VHC240 is an advanced high speed CMOS octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHC240 is an inverting 3-state buffer, and has two active-low output enables. This device is designed to drive bus lines or buffer memory address registers.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: $t_{PD} = 3.6$ ns (Typ) at $V_{CC} = 5V$
- Low Power Dissipation: $I_{CC} = 4\mu A$ (Max) at $T_A = 25$ °C
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\% \ V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 0.9V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 120 FETs or 30 Equivalent Gates

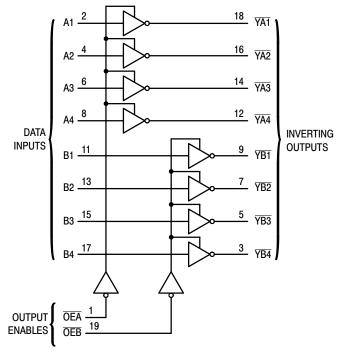


Figure 1. LOGIC DIAGRAM

MC74VHC240



DW SUFFIX 20-LEAD SOIC WIDE PACKAGE CASE 751D-05



DT SUFFIX 20-LEAD TSSOP PACKAGE CASE 948E-02



M SUFFIX 20-LEAD SOIC EIAJ PACKAGE CASE 967-01

ORDERING INFORMATION

MC74VHCXXXDW SOIC WIDE MC74VHCXXXDT TSSOP MC74VHCXXXM SOIC EIAJ

OEA [1●	20] V _{CC}
A1 [2	19	OEB
YB4 [3	18	YA1
A2 [4	17] B4
<u>∀B3</u> [5	16	YA2
A3 [6	15] B3
YB2	7	14] YA3
A4 [8	13] B2
YB1	9	12	YA4
GND [10	11] B1
			•

Figure 1. PIN ASSIGNMENT

FUNCTION TABLE

INP	JTS	OUTPUTS
OEA, OEB	A, B	ŸĀ, ŸB
L	L	Н
L	Н	L
Н	Х	Z

MAXIMUM RATINGS*

Symbol	Paramete	r	Value	Unit
V _{CC}	DC Supply Voltage		- 0.5 to + 7.0	V
V _{in}	DC Input Voltage		- 0.5 to + 7.0	V
V _{out}	DC Output Voltage		-0.5 to $V_{CC} + 0.5$	V
I _{IK}	Input Diode Current		- 20	mA
I _{OK}	Output Diode Current		± 20	mA
l _{out}	DC Output Current, per Pin		± 25	mA
I _{CC}	DC Supply Current, V _{CC} and G	ND Pins	± 75	mA
P _D	Power Dissipation in Still Air,	SOIC Packages† TSSOP Package†	500 450	mW
T _{stg}	Storage Temperature		- 65 to + 150	°C

Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

†Derating — SOIC Packages: - 7 mW/°C from 65° to 125°C TSSOP Package: - 6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V _{CC}	DC Supply Voltage	DC Supply Voltage		5.5	V
V _{in}	DC Input Voltage	DC Input Voltage			V
V _{out}	DC Output Voltage		0	V _{CC}	V
T _A	Operating Temperature, All Package Ty	pes	- 40	+ 85	°C
t _r , t _f		$f_{CC} = 3.3V \pm 0.3V$ $f_{CC} = 5.0V \pm 0.5V$	0 0	100 20	ns/V

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND \leq (V_{in} or V_{out}) \leq V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS

		Parameter Test Conditions	V _{cc}		T _A = 25°C		$T_A = -40$	0 to 85°C	
Symbol	Parameter		V	Min	Тур	Max	Min	Max	Unit
V _{IH}	Minimum High-Level Input Voltage		2.0 3.0 to 5.5	1.50 V _{CC} x 0.7			1.50 V _{CC} x 0.7		V
V _{IL}	Maximum Low–Level Input Voltage		2.0 3.0 to 5.5			0.50 V _{CC} x 0.3		0.50 V _{CC} x 0.3	V
V _{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -50 \mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -4\text{mA}$ $I_{OH} = -8\text{mA}$	3.0 4.5	2.58 3.94			2.48 3.80		
V _{OL}	Maximum Low–Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 50 \mu A$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL} \\ I_{OL} = 4mA \\ I_{OL} = 8mA$	3.0 4.5			0.36 0.36		0.44 0.44	
l _{in}	Maximum Input Leakage Current	V _{in} = 5.5V or GND	0 to 5.5			± 0.1		± 1.0	μА

DC ELECTRICAL CHARACTERISTICS

			v _{cc}	V _{CC} T _A = 25°C		T _A = - 40 to 85°C			
Symbol	Parameter	Test Conditions	v	Min	Тур	Max	Min	Max	Unit
I _{OZ}	Maximum Three–State Leakage Current	$V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	5.5			± 0.25		± 2.5	μА
Icc	Maximum Quiescent Supply Current	V _{in} = V _{CC} or GND	5.5			4.0		40.0	μА

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0 \text{ns}$)

					T _A = 25°C		$T_A = -40$	0 to 85°C	
Symbol	Parameter	Test Condi	tions	Min	Тур	Max	Min	Max	Unit
t _{PLH} , t _{PHL}	Maximum Propagation Delay, A to YA or B to YB	$V_{CC} = 3.3 \pm 0.3 V$	$C_L = 15pF$ $C_L = 50pF$		5.3 7.8	7.5 11.0	1.0 1.0	9.0 12.5	ns
		$V_{CC} = 5.0 \pm 0.5 V$	$C_L = 15pF$ $C_L = 50pF$		3.6 5.1	5.5 7.5	1.0 1.0	6.5 8.5	
t _{PZL} , t _{PZH}	Output Enable Time OEA to YA or OEB to YB	$V_{CC} = 3.3 \pm 0.3V$ $R_L = 1k\Omega$	$C_L = 15pF$ $C_L = 50pF$		6.6 9.1	10.6 14.1	1.0 1.0	12.5 16.0	ns
		$V_{CC} = 5.0 \pm 0.5V$ $R_L = 1k\Omega$			4.7 6.2	7.3 9.3	1.0 1.0	8.5 10.5	
t _{PLZ} , t _{PHZ}	Output Disable Time OEA to YA or OEB to YB	$V_{CC} = 3.3 \pm 0.3V$ $R_L = 1k\Omega$	C _L = 50pF		10.3	14.0	1.0	16.0	ns
		$V_{CC} = 5.0 \pm 0.5V$ $R_L = 1k\Omega$	C _L = 50pF		6.7	9.2	1.0	10.5	
t _{OSLH} , t _{OSHL}	Output to Output Skew	V _{CC} = 3.3 ± 0.3V (Note 1.)	C _L = 50pF			1.5		1.5	ns
		V _{CC} = 5.0 ± 0.5V (Note 1.)	C _L = 50pF			1.0		1.0	
C _{in}	Maximum Input Capacitance				4	10		10	pF
C _{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)				6				pF

		Typical @ 25°C, V _{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 2.)	17	pF

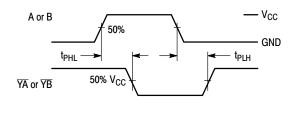
^{1.} Parameter guaranteed by design. t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSHL} = |t_{PHLm} - t_{PHLn}|.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0 \text{ns}$, $C_L = 50 \text{pF}$, $V_{CC} = 5.0 \text{V}$)

		T _A = 25°C		
Symbol	Parameter	Тур	Max	Unit
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	0.6	0.9	V
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	- 0.6	- 0.9	V
V _{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V _{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

^{2.} C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per bit). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

SWITCHING WAVEFORMS



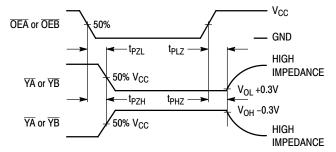
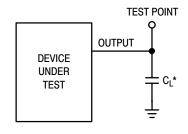


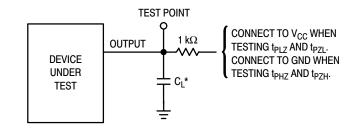
Figure 2.

Figure 3.

TEST CIRCUITS



*Includes all probe and jig capacitance



*Includes all probe and jig capacitance

Figure 4. Test Circuit

Figure 5. Test Circuit

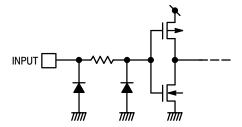
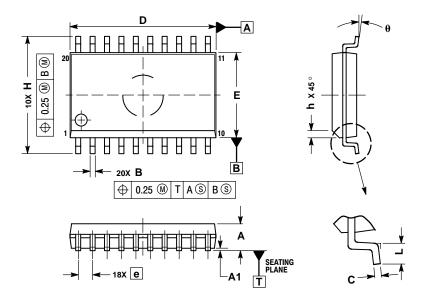


Figure 6. Input Equivalent Circuit

OUTLINE DIMENSIONS

DW SUFFIX SOIC CASE 751D-05 **ISSUE F**

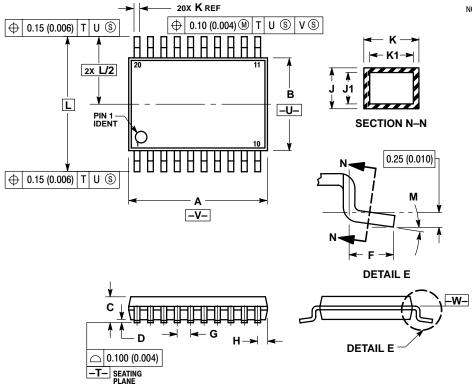


- NOTES:
 1. DIMENSIONS ARE IN MILLIMETERS.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
 5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS					
DIM	MIN	MAX				
Α	2.35	2.65				
A1	0.10	0.25				
В	0.35	0.49				
С	0.23	0.32				
D	12.65	12.95				
Е	7.40	7.60				
е	1.27	BSC				
Н	10.05	10.55				
h	0.25	0.75				
L	0.50	0.90				
θ	0 °	7 °				

OUTLINE DIMENSIONS

DT SUFFIX TSSOP CASE 948E-02 **ISSUE A**



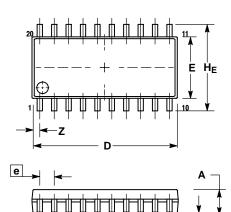
- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- DIMENSION B DOES NOT INCLUDE INTERLEAD
 FLASH OR PROTRUSION. INTERLEAD FLASH OR
 PROTRUSION SHALL NOT EXCEED 0.25 (0.010)
- PROTRUSION SHALL NOT EXCEED 0.25 (0.010)
 PER SIDE.

 5. DIMENSION K DOES NOT INCLUDE DAMBAR
 PROTRUSION. ALLOWABLE DAMBAR
 PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN
 EXCESS OF THE K DIMENSION AT MAXIMUM
 MATERIAL CONDITION.
- 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	6.40	6.60	0.252	0.260	
В	4.30	4.50	0.169	0.177	
С		1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	BSC	0.026 BSC		
Н	0.27	0.37	0.011	0.015	
J	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
K	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
Г	6.40	BSC	0.252	BSC	
М	0°	8°	0°	8°	

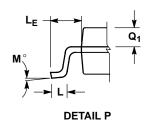
OUTLINE DIMENSIONS

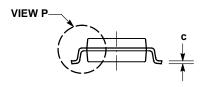
M SUFFIX SOIC EIAJ CASE 967-01 ISSUE 0



0.10 (0.004)

0.13 (0.005) M





NOTES:

- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.

 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) DEED RICE.
- PROTRUSIONS SHALL NUT EXCEED U.13 (U.50U)
 PER SIDE.

 4. TERMINAL NUMBERS ARE SHOWN FOR
 REFERENCE ONLY.

 5. THE LEAD WIDTH DIMENSION (b) DOES NOT
 INCLUDE DAMBAR PROTRUSION. ALLOWABLE
 DAMBAR PROTRUSION SHALL BE 0.08 (0.003)
 TOTAL IN EXCESS OF THE LEAD WIDTH
 DIMENSION AT MAXIMUM MATERIAL CONDITION.
 DAMBAR CANNOT BE LOCATED ON THE LOWER DIMENSION AT MAXIMUM MATERIAL CONDITION.
 DAMBAR CANNOT BE LOCATED ON THE LOWER
 RADIUS OR THE FOOT. MINIMUM SPACE
 BETWEEN PROTRUSIONS AND ADJACENT LEAD
 TO BE 0.46 (0.018).

	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α		2.05		0.081	
A ₁	0.05	0.20	0.002	0.008	
b	0.35	0.50	0.014	0.020	
С	0.18	0.27	0.007	0.011	
D	12.35	12.80	0.486	0.504	
E	5.10	5.45	0.201	0.215	
е	1.27	BSC	0.050 BSC		
HE	7.40	8.20	0.291	0.323	
L	0.50	0.85	0.020	0.033	
LE	1.10	1.50	0.043	0.059	
M	0 °	10 °	0 °	10°	
Q_1	0.70	0.90	0.028	0.035	
Z		0.81		0.032	

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