DATA SHEET

PCX8598X-2 Family
1024 × 8-bit CMOS EEPROMS with I²C-bus interface

Product specification
Supersedes data of April 1992
File under Integrated Circuits, IC12

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Philips Semiconductors

PHILIPS

1024 × 8-bit CMOS EEPROMS with I²C-bus interface

PCX8598X-2 Family

FEATURES

- Low power CMOS
  - maximum active current 4.0 mA
  - maximum standby current 10 μA (at 6.0 V), typical 4 μA
- Non-volatile storage of 8-Kbits organized as four pages of 256 × 8-bits each
- Single supply with full operation down to 2.5 V
- On-chip voltage multiplier
- Serial input/output I²C-bus
- Write operations
  - byte write mode
  - 8-byte page write mode (minimizes total write time per byte)
- Write-protection input
- Read operations
  - sequential read
  - random read
- Internal timer for writing (no external components)
- Power-on reset
- High reliability by using a redundant storage code (single bit error correction)
- Endurance
  - >500 k E/W-cycles at T_{amb} = 22 °C
- 40 years non-volatile data retention time (typ.)
- Pin and address compatible to
  - PCX8582X-2 Family and PCX8594X-2 Family.

DESCRIPTION

The PCX8598X-2 is an 8-Kbit (1024 × 8-bit) floating gate electrically erasable programmable read only memory (EEPROM). By using an internal redundant storage code it is fault tolerant to single bit errors. This feature dramatically increases reliability compared to conventional EEPROM memories.

Power consumption is low due to the full CMOS technology used. The programming voltage is generated on-chip, using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient. Up to two PCX8598X-2 devices may be connected to the I²C-bus. Chip select is accomplished by one address input (A2).

Timing of the ERASE/WRITE cycle is carried out internally, thus no external components are required. Pin 7 (PTC) must be connected to either V_{DD} or left open-circuit.

There is an option of using an external clock for timing the length of an ERASE/WRITE cycle.

A write-protection input at pin 1 (WP) allows disable of write-commands from the master by a hardware signal. When pin 1 is HIGH and one of the upper 512 EEPROM cells is addressed, then the data bytes will not be acknowledged by the PCX8598X-2 and the EEPROM contents are not changed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		2.5	6.0	V
I_{DDR}	supply current READ	f_{SCL} = 100 kHz			
		V_{DD} = 3 V	–	60	μA
		V_{DD} = 6 V	–	200	μA
I_{DDW}	supply current ERASE/WRITE	f_{SCL} = 100 kHz			
		V_{DD} = 3 V	–	1.0	mA
		V_{DD} = 6 V	–	4.0	mA
I_{DDSB}	supply current STANDBY	V_{DD} = 3 V	–	3.5	μA
		V_{DD} = 6 V	–	10	μA

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			TEMPERATURE (°C)		SUPPLY (V)	
	NAME	DESCRIPTION	VERSION	MIN.	MAX.	MIN.	MAX.
PCF8598C-2P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1	–40	+85	2.5	6.0
PCD8598D-2P				–25	+70	3.0	6.0
PCF8598E-2P				–40	+85	4.5	5.5
PCA8598F-2P				–40	+125	4.5	5.5
PCF8598C-2T	SO8	plastic small outline package; 8 leads; body width 7.5 mm	SOT176-1	–40	+85	2.5	6.0
PCD8598D-2T				–25	+70	3.0	6.0
PCF8598E-2T				–40	+85	4.5	5.5
PCA8598F-2T				–40	+125	4.5	5.5

DEVICE SELECTION

Table 1 Device selection code

SELECTION	DEVICE CODE				CHIP ENABLE			R/$\overline{W}$
Bit	b7[1]	b6	b5	b4	b3	b2	b1	b0
Device	1	0	1	0	A2	MEM SEL	MEM SEL	R/$\overline{W}$

Note

1. The MSB b7 is sent first.

Table 2 Endurance and data retention guarantees

DEVICE	ENDURANCE E/W CYCLES	DATA RETENTION YEARS
PCF8598C-2; PCA8598F-2	500000[1]	40

Note

1. At the time of publication of this data sheet the statistical history was not yet sufficient to guarantee 1000000000 E/W cycle performance for these types.

BLOCK DIAGRAM

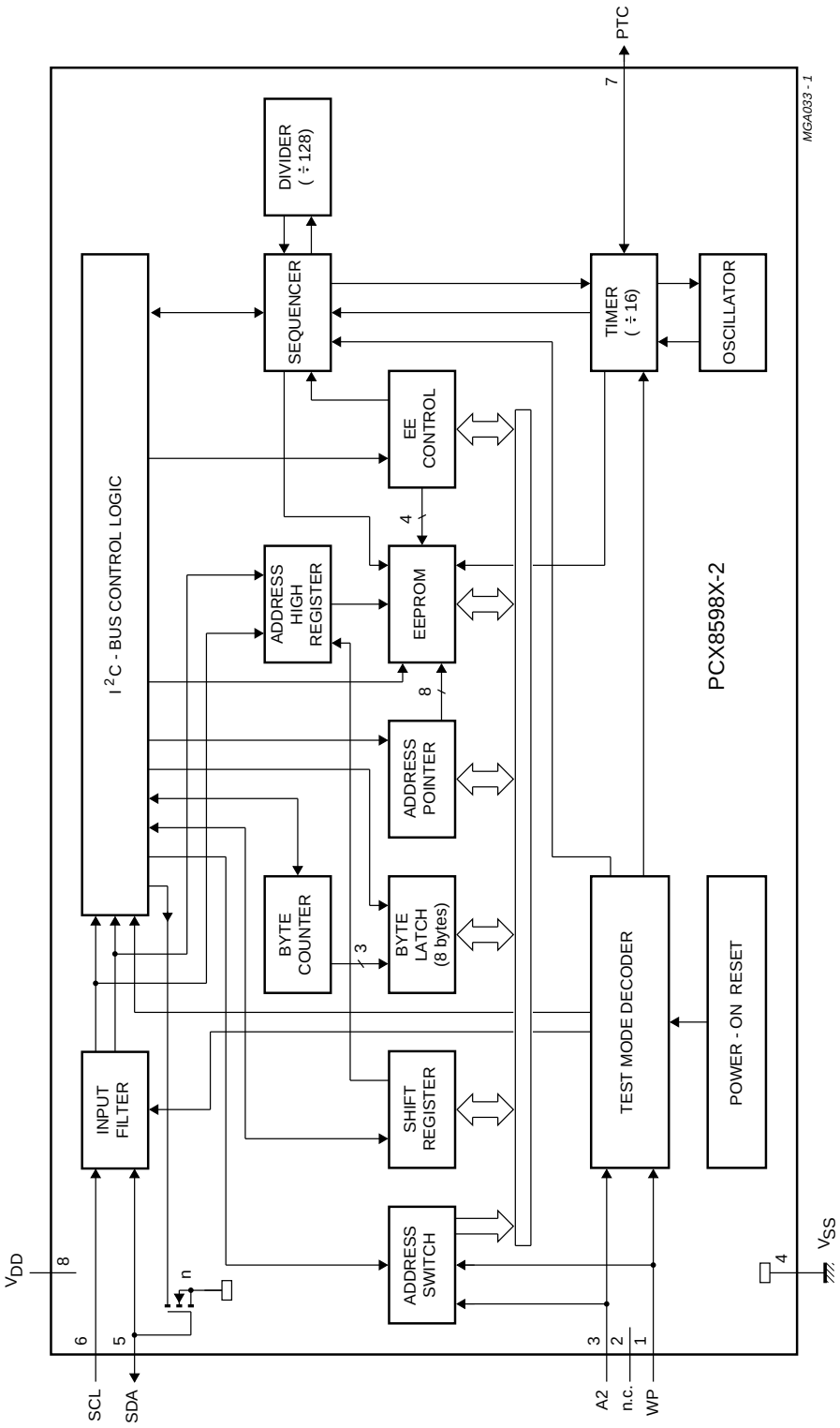


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
WP	1	write-protection input
n.c.	2	not connected
A2	3	address input 2
V_{SS}	4	negative supply voltage
SDA	5	serial data input/output (I²C-bus)
SCL	6	serial clock input (I²C-bus)
PTC	7	programming time control output
V_{DD}	8	positive supply voltage

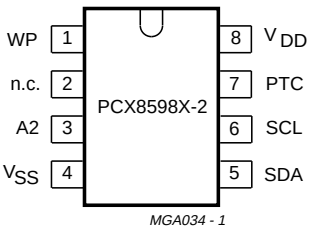


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–0.3	+7.0	V
V_I	voltage on any input pin	$\|Z_I\| > 500\ \Omega$	V_{SS} – 0.8	V_{DD} + 0.8	V
I_I	current on any input pin		–	1	mA
I_O	output current		–	10	mA
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	operating ambient temperature				
	PCF8598C-2; PCF8598E-2		–40	+85	°C
	PCD8598D-2		–25	+70	°C
	PCA8598F-2		–40	+125	°C

CHARACTERISTICS

PCF8598C-2: V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.
PCD8598D-2: V_{DD} = 3.0 to 6.0 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; unless otherwise specified.
PCF8598E-2: V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.
PCA8598F-2: V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +125 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supplies					
V_{DD}	supply voltage				
	PCF8598C-2		2.5	6.0	V
	PCD8598D-2		3.0	6.0	V
	PCF8598E-2; PCA8598F-2		4.5	5.5	V
I_{DDR}	supply current READ	f_{SCL} = 100 kHz			
	PCF8598C-2; PCD8598D-2	V_{DD} = 3.0 V	–	60	µA
		V_{DD} = 6.0 V	–	200	µA
	PCF8598E-2; PCA8598F-2	V_{DD} = 5.5 V	–	200	µA
I_{DDW}	supply current ERASE/WRITE	f_{SCL} = 100 kHz			
	PCF8598C-2; PCD8598D-2	V_{DD} = 3.0 V	–	1.0	mA
		V_{DD} = 6.0 V	–	4.0	mA
	PCF8598E-2; PCA8598F-2	V_{DD} = 5.5 V	–	4.0	mA
I_{DDSB}	supply current STANDBY	f_{SCL} = 100 kHz			
	PCF8598C-2; PCD8598D-2	V_{DD} = 3.0 V	–	3.5	µA
		V_{DD} = 6.0 V	–	10	µA
	PCF8598E-2; PCA8598F-2	V_{DD} = 5.5 V	–	10	µA
PTC input (pin 7)					
V_{IL}	LOW level input voltage		−0.8	$0.1V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.9V_{DD}$	V_{DD} + 0.8	V
SCL input (pin 6)					
V_{IL}	LOW level input voltage		−0.8	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	V_{DD} + 0.8	V
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	–	±1	µA
f_{SCL}	clock input frequency		0	100	kHz
C_I	input capacitance	$V_I = V_{SS}$	–	7	pF
SDA input/output (pin 5)					
V_{IL}	LOW level input voltage		−0.8	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	V_{DD} + 0.8	V
V_{OL}	LOW level output voltage	I_{OL} = 3 mA; $V_{DD(min)}$	–	0.4	V
I_{LO}	output leakage current	$V_{OH} = V_{DD}$	–	1	µA
C_I	input capacitance	$V_I = V_{SS}$	–	7	pF
Data retention time					
t_S	data retention time	T_{amb} = 55 °C	10	–	years

WRITE CYCLE LIMITS

The power-on reset circuit resets the I²C-bus logic with a set-up time of ≤10 µs.
Selection of the chip address is achieved by connecting the A2 input to either V_{SS} or V_{DD}.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ERASE/WRITE cycle timing						
$t_{E/W}$	ERASE/WRITE cycle time					
	internal oscillator		–	7	–	ms
	external clock		4	–	10	ms
Endurance						
$N_{E/W}$	ERASE/WRITE cycle per byte					
	PCF8598C-2	T_{amb} = 85 °C; $t_{E/W}$ = 4 to 10 ms	100000	–	–	cycles
		T_{amb} = 22 °C; $t_{E/W}$ = 5 ms	500000	–	–	cycles
	PCD8598D-2	T_{amb} = –25 to +70 °C; $t_{E/W}$ = 4 to 10 ms	10000	–	–	cycles
		T_{amb} = –25 to +40 °C; $t_{E/W}$ = 5 ms	100000	–	–	cycles
	PCF8598E-2	T_{amb} = –40 to +85 °C; $t_{E/W}$ = 4 to 10 ms	10000	–	–	cycles
		T_{amb} = 22 °C; $t_{E/W}$ = 5 ms	100000	–	–	cycles
	PCA8598F-2	T_{amb} = 125 °C; $t_{E/W}$ = 4 to 10 ms	50000	–	–	cycles
		T_{amb} = 85 °C; $t_{E/W}$ = 4 to 10 ms	100000	–	–	cycles
		T_{amb} = 22 °C; $t_{E/W}$ = 5 ms	500000	–	–	cycles
Programming						
f_p	programming frequency		25	–	60	kHz
t_{LOW}	LOW time		5	–	–	µs
t_{HIGH}	HIGH time		5	–	–	µs
t_r	rise time		–	–	300	ns
t_f	fall time		–	–	300	ns
t_d	delay time		0	–	t_{LOW}	µs

I²C-BUS PROTOCOL

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The serial bus consists of two bidirectional lines: one for data signals (SDA), and one for clock signals (SCL).

Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The following bus conditions have been defined:

- **Bus not busy:** both data and clock lines remain HIGH.

  Start data transfer: a change in the state of the data line, from HIGH-to-LOW, while the clock is HIGH, defines the start condition.
- **Stop data transfer:** a change in the state of the data line, from LOW-to-HIGH, while the clock is HIGH, defines the stop condition.
- **Data valid:** the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transferred between the start and stop conditions is limited to seven bytes in the ERASE/WRITE mode and eight bytes in the PAGE ERASE/WRITE mode. Data transfer is unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I²C-bus specifications a low-speed mode (2 kHz clock rate) and a high speed mode (100 kHz clock rate) are defined.

The PCX8598X-2 operates in both modes.

By definition a device that sends a signal is called a ‘transmitter’, and the device which receives the signal is called a ‘receive’. The device which controls the signal is called the ‘master’. The devices that are controlled by the master are called ‘slaves’.

Each byte is followed by one acknowledge bit. This acknowledge bit is a HIGH level, put on the bus by the transmitter. The master generates an extra acknowledge related clock pulse. The slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.

The master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse.

Set-up and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

DEVICE ADDRESSING

Following a start condition the bus master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see Fig.3). For the PCX8598X-2 this is fixed as 1010.

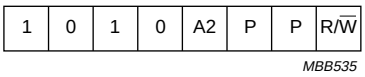


Fig.3 Slave address.

The next significant bit (A2) addresses a particular device. A system could have up to two PCX8598X-2 devices on the bus. The two addresses are defined by the state of the A2 input.

The next two significant bits of the slave address field are the page selection bits. It is used by the host to select one out of four pages (page = 256 bytes of memory). These are, in effect, the two most significant bits of the word address.

The last bit of the slave address defines the operation to be performed. When set to logic 1 a read operation is selected.

Address bit A2 must be connected to either V_{DD} or V_{SS}.

WRITE OPERATIONS

Byte/word write

For a write operation the PCX8598X-2 requires a second address field. This address field is a word address providing access to any one of the four 256 words of memory. Upon receipt of the word address the PCX8598X-2 responds with an acknowledge and awaits the next eight bits of data, again responding with an acknowledge. Word address is automatically incremented. The master can now terminate the transfer by generating a stop condition or transmit up to six more bytes of data and then terminate by generating a stop condition.

After this stop condition the ERASE/WRITE cycle starts and the bus is free for another transmission. Its duration is 7 ms (typ.) per byte.

During the ERASE/WRITE cycle the slave receiver does not send an acknowledge bit if addressed via the I²C-bus.

PAGE WRITE

The PCX8598X-2 is capable of an eight-byte page write operation. It is initiated in the same manner as the byte write operation. The master can transmit eight data bytes within one transmission. After receipt of each byte the PCX8598X-2 will respond with an acknowledge. The typical ERASE/WRITE time in this mode is 9×7 ms = 63 ms.

After the receipt of each data byte the three low order bits of the word address are internally incremented. The high order five bits of the address remain unchanged. If the master transmits more than eight bytes prior to generating the stop condition, no acknowledge will be given on the ninth (and following) data bytes and the whole transmission will be ignored. As in the byte write operation, all inputs are disabled until completion of the internal write cycles.

Remark

A write to the EEPROM is always performed if the pin WP is LOW. If WP is HIGH, then the upper half of the EEPROM is write-protected and no acknowledge will be given by the PCX8598X-2 when one of the upper 512 EEPROM bytes is addressed. However, an acknowledge will be given after the slave address and the word address.

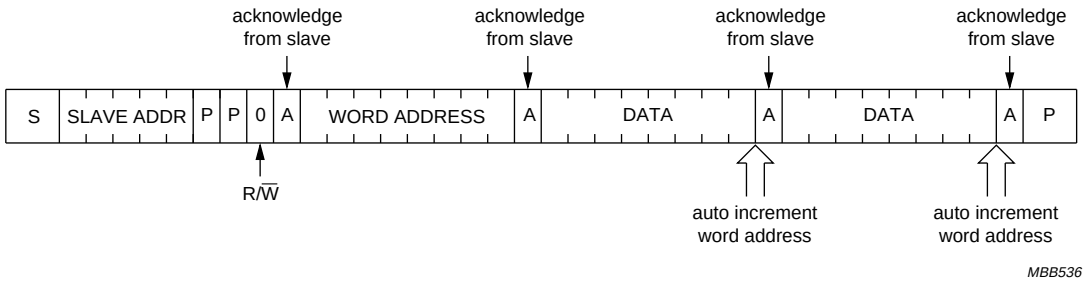


Fig.4 Auto increment memory word address; two byte write.

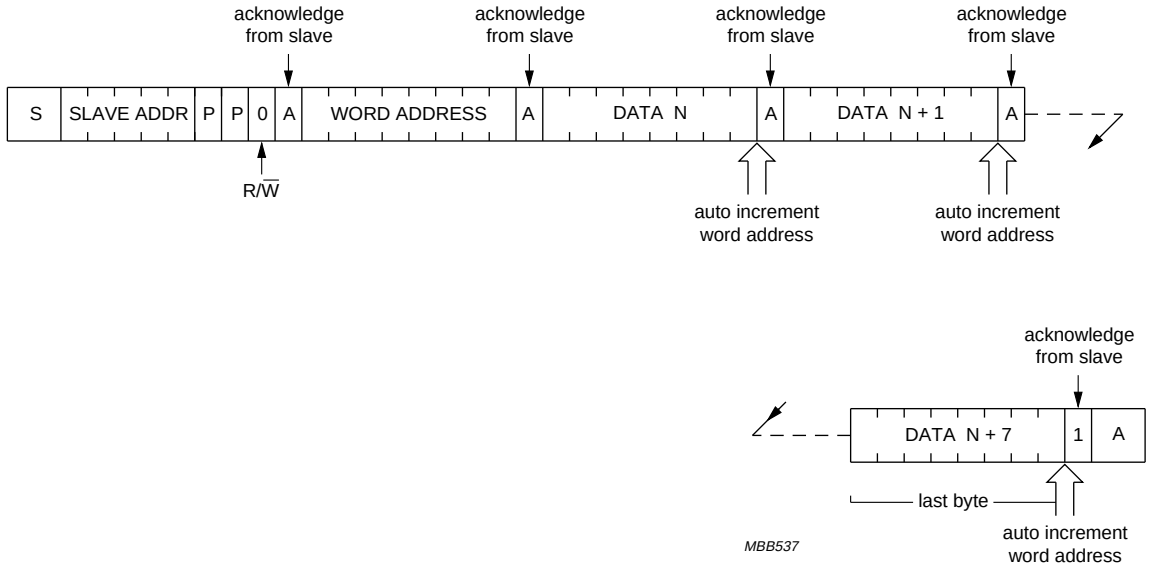


Fig.5 Page write operation; eight byte.

READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the LSB of the slave address is set to logic 1. There are three basic read operations; current address read, random read and sequential read.

Remark

The lower 8-bits of the word address are incremented after each transmission of a data byte (read or write). The MSB of the word address, which is defined in the slave address, is not changed when the word address count overflows. Thus, the word address overflows from 255 to 0, from 511 to 256, from 767 to 512 and from 1023 to 768.

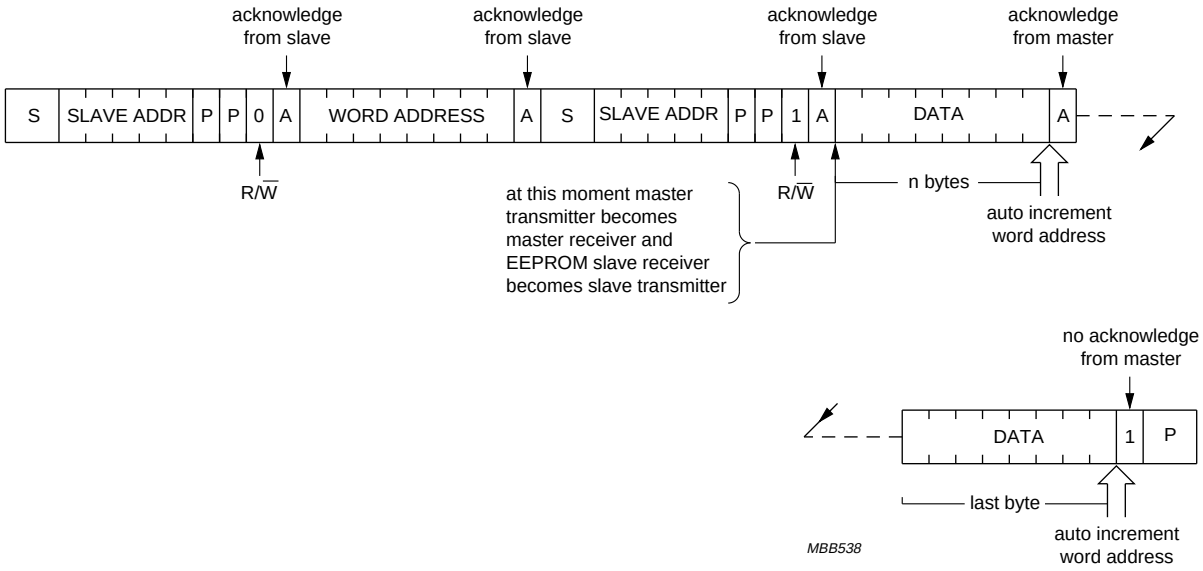


Fig.6 Master reads PCX8598X-2 slave after setting word address (WRITE word address; READ data).

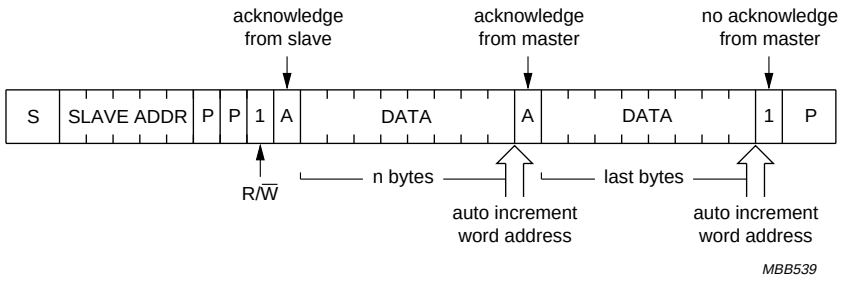


Fig.7 Master reads PCX8598X-2 immediately after first byte (READ mode).

I²C-BUS TIMING

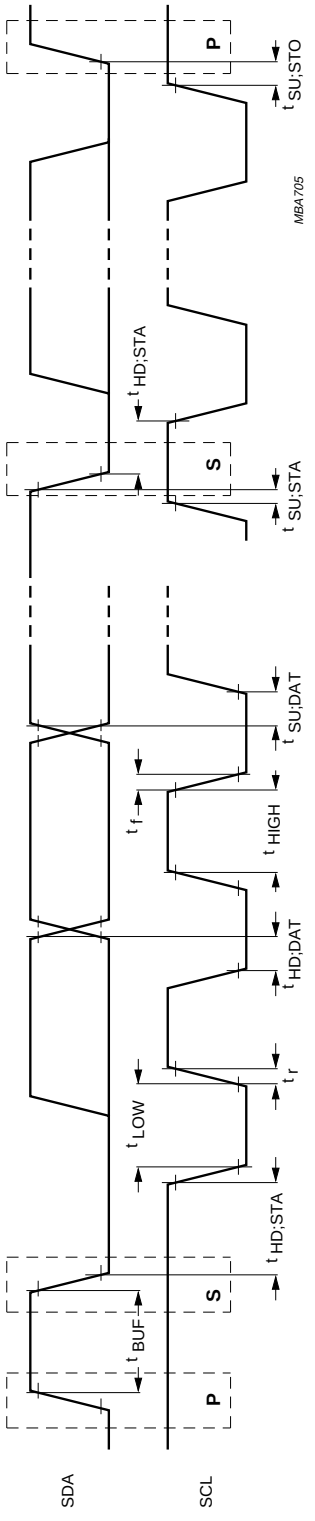


Fig.8 Timing requirements for the I²C-bus.

I²C-BUS CHARACTERISTICS

All of the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing from V_{SS} to V_{DD}.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
f_{SCL}	clock frequency		0	100	kHz
t_{BUF}	time the bus must be free before new transmission can start		4.7	–	µs
$t_{HD;STA}$	start condition hold time after which first clock pulse is generated		4.0	–	µs
t_{LOW}	LOW level clock period		4.7	–	µs
t_{HIGH}	HIGH level clock period		4.0	–	µs
$t_{SU;STA}$	set-up time for start condition	repeated start	4.7	–	µs
$t_{HD;DAT}$	data hold time for bus compatible masters		5	–	µs
$t_{HD;DAT}$	data hold time for bus devices	note 1	0	–	ns
$t_{SU;DAT}$	data set-up time		250	–	ns
t_r	SDA and SCL rise time		–	1	µs
t_f	SDA and SCL fall time		–	300	ns
$t_{SU;STO}$	set-up time for stop condition		4.7	–	µs

Note

1. The hold time required (not greater than 300 ns) to bridge the undefined region of the falling edge of SCL must be internally provided by a transmitter.1

EXTERNAL CLOCK TIMING

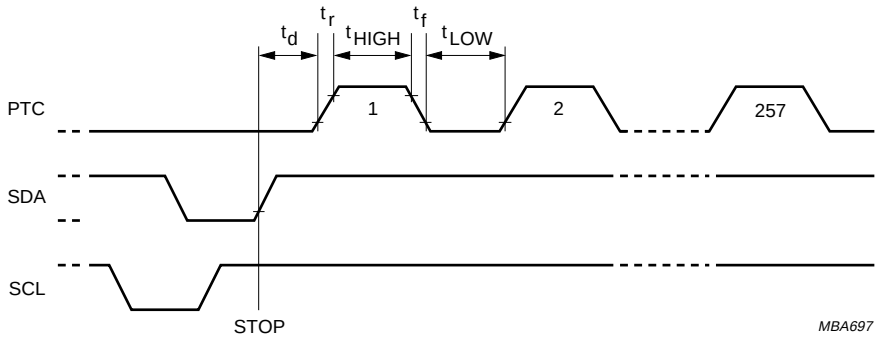


Fig.9 One byte ERASE/WRITE cycle.

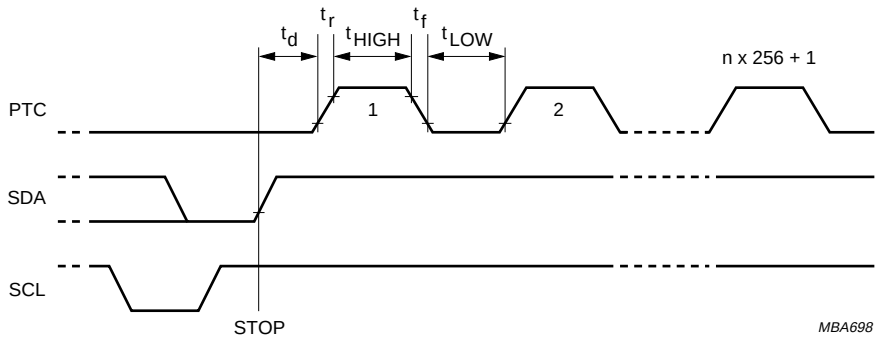


Fig.10 n byte ERASE/WRITE cycle (n = 2 to 7).

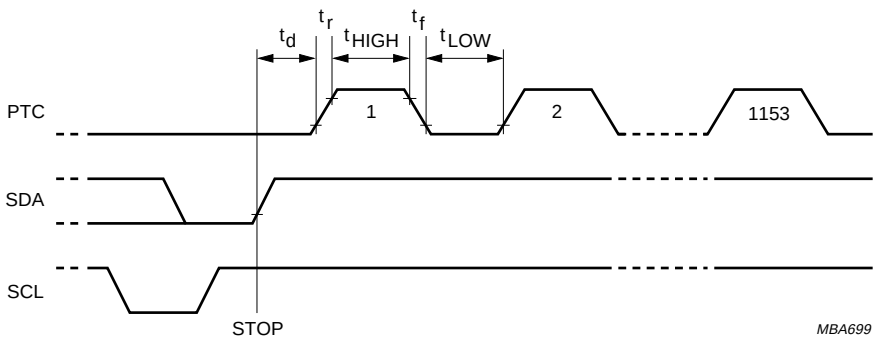
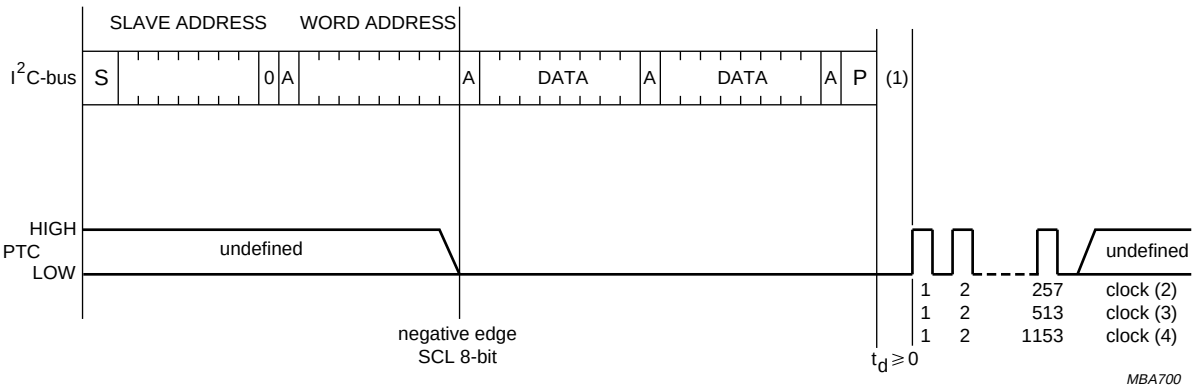


Fig.11 Page mode.



(1) If an external clock is chosen, this information is latched internally by setting pin 7 (PTC) LOW after transmission of the eighth bit of the word address (negative edge of SCL). Thus the state of pin 7 may be previously undefined. Leaving pin 7 LOW causes a higher standby current.

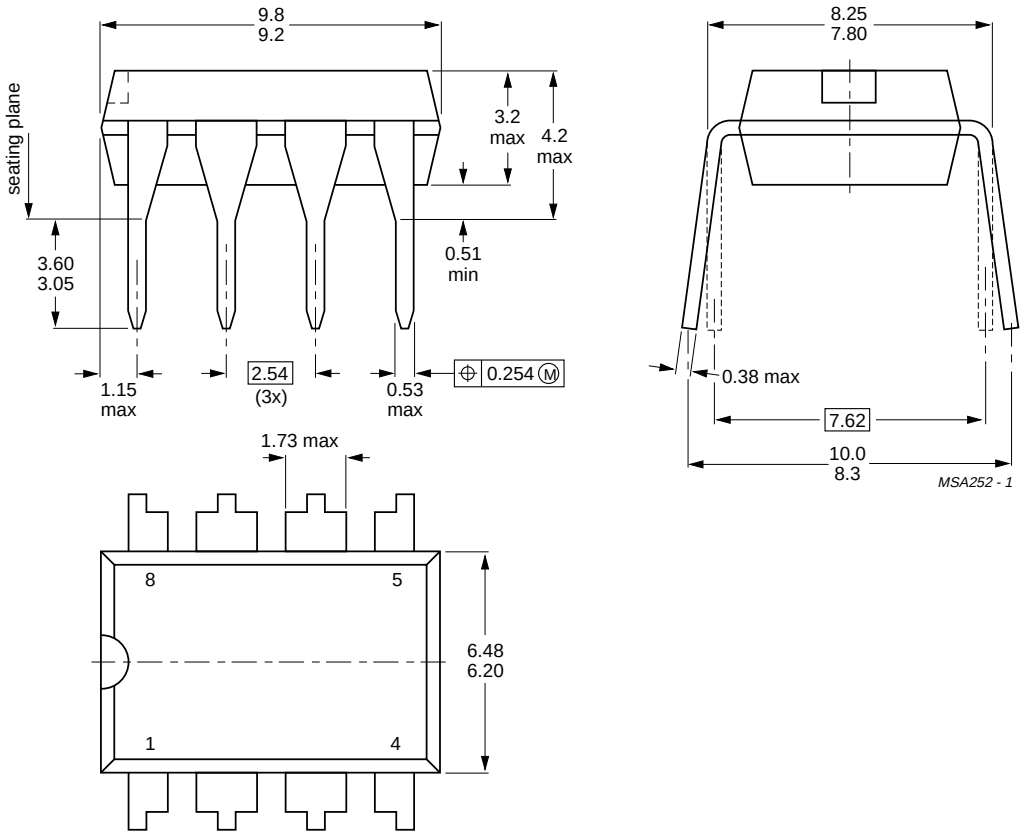
(2) 1-byte programming.

(3) 2-byte programming.

(4) One page (8 byte) programming.

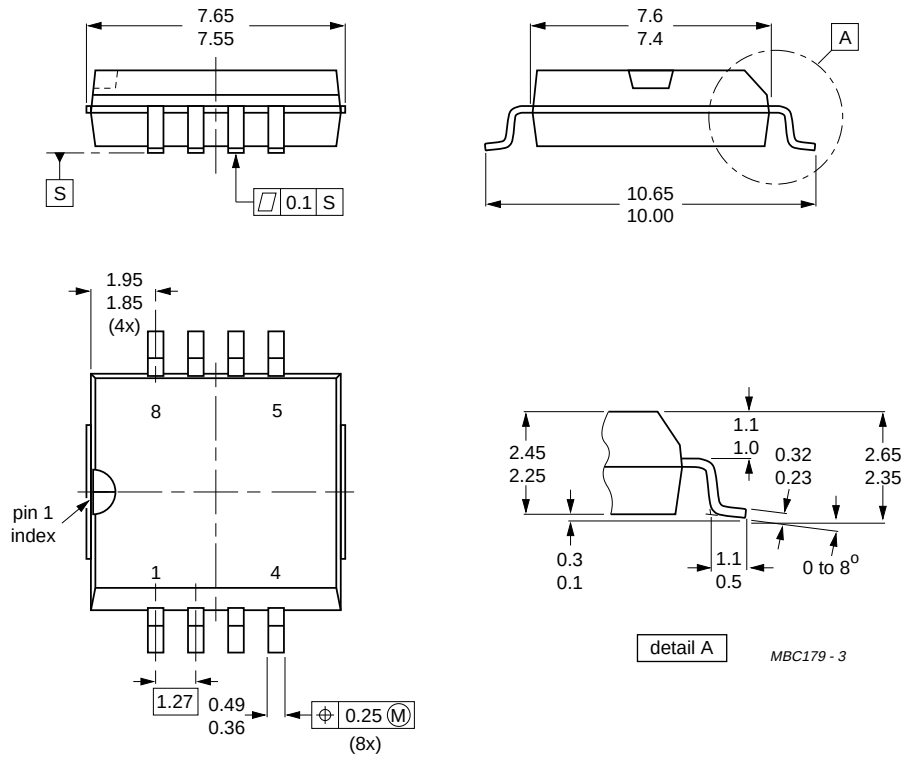
Fig.12 External clock.

PACKAGE OUTLINES



Dimensions in mm.

Fig.13 Plastic dual in-line package; 8 leads (300 mil) DIP8; SOT97-1.



Dimensions in mm.

Fig.14 Plastic small outline package; 8 leads; body width 7.5 mm (SO8L; SOT176-1).

SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

Plastic small-outline packages

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Philips Semiconductors – a worldwide company

Argentina: IEROD, Av. Juramento 1992 - 14.b, (1428)
BUENOS AIRES, Tel. (541)786 7633, Fax. (541)786 9367

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
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Brazil: Rua do Rocio 220 - 5th floor, Suite 51,
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Germany: P.O. Box 10 63 23, 20043 HAMBURG,
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Greece: No. 15, 25th March Street, GR 17778 TAVROS,
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Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
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Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
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Bangkok 10260, THAILAND,
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Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. (0212)279 2770, Fax. (0212)269 3094

United Kingdom: Philips Semiconductors LTD.,
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Tel. (081)730-5000, Fax. (081)754-8421

United States: 811 East Arques Avenue, SUNNYVALE,
CA 94088-3409, Tel. (800)234-7381, Fax. (708)296-8556

Uruguay: Coronel Mora 433, MONTEVIDEO,
Tel. (02)70-4044, Fax. (02)92 0601

For all other countries apply to: Philips Semiconductors,
International Marketing and Sales, Building BE-p,
P.O. Box 218, 5600 MD, EINDHOVEN, The Netherlands,
Telex 35000 phtcnl, Fax. +31-40-724825

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