SAMSUNG SEMICONDUCTOR

KM29N16000

2M x 8 Bit NAND Flash Memory

PRELIMINARY - June 1994

FEATURES

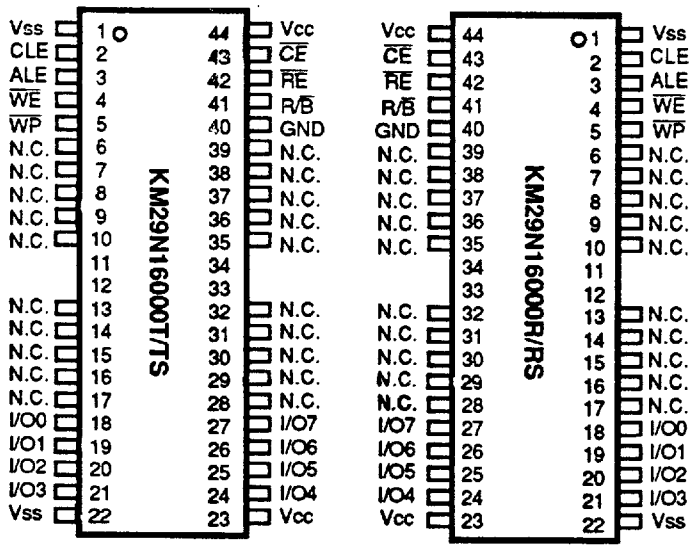
- Single 5 - volt Supply
- Organization
  - Memory Cell Array : (2M +64K) x 8
  - Data Register : (256 + 8) x 8
- Automatic Program and Erase
  - Page Program : (256 + 8)Byte
  - Block Erase : (4K +128)Byte
  - Multi-Block Erase
  - Status Register
- 264 - Byte Page Read Operation
  - Random Access : 20 µs
  - Sequential Page Access : 80 ns
- System Performance Enhancement
  - Erase Suspend / Resume Capability
  - Ready/Busy Status Output
- Command/Addresses/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance :10^6 Program/Erase Cycles (Target)
  - Data Retention : 10 years
- Command Register Operation
- Package
  - KM29N16000T/TS: 44(40)-TSOP2-400F
  - KM29N16000R/RS: 44(40)-TSOP2-400R

GENERAL DESCRIPTION

The KM29N16000 is a 2M(2,097,152)x8 bit NAND Flash memory with a spare 64K(65,536)x8 bits. Its NAND cell provides the most cost-effective solution for the mass solid state storage market. A program operation programs the 264-byte page in typically 300µs and an erase operation can be performed in typically 6ms on either a 4K-byte block or multiple blocks. Data in the page can be read out at 80ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command inputs. The on-chip write controller automates all program and erase system functions, including pulse repetition, where required, and internal verify and margining of data. Even write-intensive systems can take advantage of the KM29N16000's extended reliability of one million program/erase cycles. The spare eight bytes of a page combined with the other 256 bytes can be utilized by system-level Error Checking and Correction to further improve the endurance to well over 1,000,000 cycles.

The KM29N16000 is an optimum solution for large nonvolatile storage applications such as solid state storage, digital voice recorder, digital still camera and other portable applications requiring nonvolatility.

PIN CONFIGURATION



44(40) TSOP (II) STANDARD TYPE

44(40) TSOP (II) REVERSE TYPE

Pin Name	Pin Function
I/O0 ~ I/O7	Data Input/Outputs
CLE	Command Latch Enable
ALE	Address Latch Enable
$\overline{CE}$	Chip Enable
$\overline{RE}$	Read Enable
$\overline{WE}$	Write Enable
$\overline{WP}$	Write Protect
R/$\overline{B}$	Ready/Busy output
GND	Ground Input
Vcc	Power
Vss	Ground
N.C.	No Connection

Notes : Connect all Vcc and Vss pins of each device to common power supply outputs.
Do NOT leave Vcc, Vss or GND inputs disconnected.

Figure 1. FUNCTIONAL BLOCK DIAGRAM

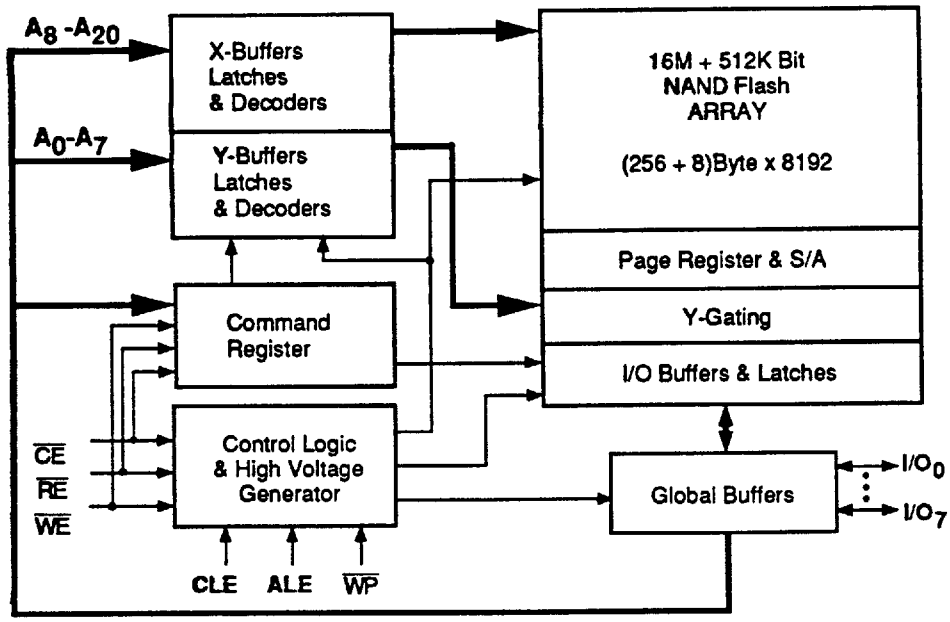
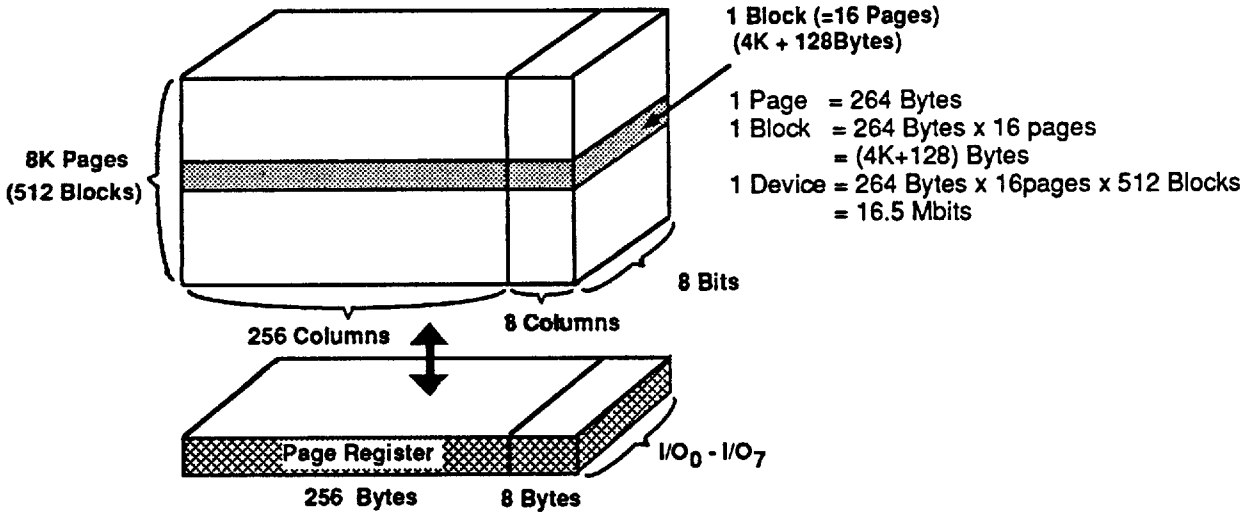


Figure 2. ARRAY ORGANIZATION



	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7	
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	Column Address (A0-A7)
2nd Cycle	A8	A9	A10	A11	A12	A13	A14	A15	Page Address (A8-A11)
3rd Cycle	A16	A17	A18	A19	A20	*X	*X	*X	Block Address (A12-A20)

*: X can be V_{IL} or V_{IH}.

PRODUCT INTRODUCTION

The KM29N16000 is a 16.5M bit(17,301,504 bit) memory organized as 8192 rows by 264 columns. A spare eight columns are located from column addresses 256 to 263. A 264-bit data register is connected to the memory cell arrays accommodating data transfer between the I/O buffers and memory during page read and page program operations. The memory array is made up of 8 cells that are serially connected to form a NAND structure. Each of the 8 cells reside in a different page. A block consists of the 16 pages formed by two neighboring NAND structures, totaling 528 NAND structures of 8 bits. The array organization is shown in Figure 2. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 512 separately grouped erasable 4K-byte blocks.

The KM29N16000 has addresses multiplexed into 8 I/O's. This scheme dramatically reduces pin counts and allows system upgrades to future higher densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Data is latched on the *rising edge* of $\overline{WE}$. Command Latch Enable (CLE) and Address Latch Enable (ALE) are used to multiplex command and address, respectively, via the I/O pins. All commands require one bus cycle except for Block Erase which requires two cycles: a cycle for erase-setup and another for erase-confirm after block address loading. The 2M byte physical space requires 21 addresses, thereby requiring three cycles for byte-level addressing: column address, low row address and high row address, in that order. Page Read and Page Program need the same three address cycles following the required command input. In Block Erase and Multi-Block Erase operation, however, only the two row address cycles are used.

Device operations are selected by writing specific commands into the command register. Table1 defines the specific commands of the KM29N16000.

Table 1. COMMAND SETS

Function	1st. Cycle	2nd. Cycle	Acceptable Command during Busy State
Serial Data Input	80H	-	
Read 1	00H	-	
Read 2	50H	-	
Read ID	90H		
Reset	FFH	-	
Page Program	10H	-	√
Block Erase	60H	D0H	
Multi-Block Erase	60H - - - 60H	D0H	
Erase Suspend	B0H	-	√
Erase Resume	D0H	-	
Read Status	70H	-	√
Read Register	E0H	-	

PIN DESCRIPTION

Command Latch Enable (CLE)

The CLE input controls the path activation for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the $\overline{WE}$ signal.

Address Latch Enable (ALE)

The ALE input controls the path activation for address and input data to the internal address/data registers. Addresses are latched on the rising edge of $\overline{WE}$ with ALE high , and input data is latched when ALE is low. When the device is in the busy state during program or erase, $\overline{CE}$ high does not return the device to standby mode.

Chip Enable ($\overline{CE}$)

The $\overline{CE}$ input is the device selection control. When $\overline{CE}$ goes high during a read operation the device is returned to standby mode. However, when the device is in the busy state during program or erase, $\overline{CE}$ high is ignored, and does not return the device to standby mode.

Write Enable ($\overline{WE}$)

The $\overline{WE}$ input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the $\overline{WE}$ pulse.

Read Enable ($\overline{RE}$)

The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid t_{REA} after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.

I/O Port : I/O_0 - I/O_7

The I/O pins are used to input commands, address and data, and to output data during read operations. The I/O pins float to high-Z when the chip is deselected or the outputs are disabled.

Write Protect ($\overline{WP}$)

The $\overline{WP}$ pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low.

Ready / Busy(R/$\overline{B}$)

The R/$\overline{B}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to a high state upon completion. It is an open drain output and does not float to a tri-state condition when the chip is deselected or outputs are disabled.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_{IN}	-0.6 to +7.0	V
Temperature Under Bias	T_{bias}	-10 to +125	°C
Storage Temperature	T_{stg}	-65 to +150	°C
Short Circuit Output Current	I_{os}	5	mA

* Notes

1. Minimum DC voltage is -0.3V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns. Maximum DC voltage on input/output pins is Vcc +0.5V which, during transitions, may overshoot to Vcc +2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to GND, Ta = 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Supply Voltage	Vss	0	0	0	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Test Conditions		Min	Typ	Max	Unit
Operating Current	Serial Read	Icc1	tcycle=80ns	$\overline{CE}$=VIL, Iout = 0 mA	-	15	30	mA
		Icc2	tcycle=1 us		-	5	10	mA
	Command, Address Input	Icc3	tcycle=80ns			10	20	mA
	Data Input	Icc4	-		-	20	40	mA
	Register Read	Icc5	tcycle=80ns	Iout = 0 mA	-	15	30	mA
	Program	Icc6	-		-	15	30	mA
	Erase	Icc7	-		-	25	40	mA
Stand-by Current (TTL)		ISB1	$\overline{CE}$=VIH		-	-	1	mA
Stand-by Current (CMOS)		ISB2	$\overline{CE}$=Vcc-0.2, $\overline{WP}$=0V/Vcc		-	-	100	µA
Input Leakage Current		ILI	VIN =0 to 5.5 V		-	-	10	µA
Output Leakage Current		ILO	VOUT =0 to 5.5 V		-	-	10	µA
Input High Voltage, All inputs		VIH	-		2.0	-	Vcc+0.5	V
Input Low Voltage, All inputs		VIL	-		-0.3	-	0.8	V
Output High Voltage Level		VOH	IOH= -400 µA		2.4	-	-	V
Output Low Voltage Level		VOL	IOL= 2.1 mA		-	-	0.4	V
Output Low Current (R/$\overline{B}$)		IOL(R/$\overline{B}$)	VOL =0.4 V		8	10	-	mA

VALID BLOCK

Symbol	Parameter	Min	Typ	Max	Unit
N_{VB}	Valid Block Number	502	508	512	Blocks

Note : The KM29N16000 may include unusable blocks. Do not try to access these blocks for program and erase. A bad block does not affect the performance of good blocks. (Refer to technical note)

AC TEST CONDITION (Ta = 0°C to + 70°C, Vcc = 5V±10%, unless otherwise noted.)

Parameter	Value
Input Pulse Levels	0.4V to 2.6V
Input Rise and Fall Times	5 ns
Input and Output Timing Levels	0.8V and 2.0V
Output Load	1 TTL GATE and C_L = 100 pF

CAPACITANCE (Ta = 25°C , Vcc = 5V, f = 1.0 MHz)

Item	Symbol	Condition	Min	Max	Unit
Input / Output Capacitance	$C_{I/O}$	V_{IL} = 0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	-	10	pF

Note : Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	Mode	I/O	Power
H	L	L	⌐↓	H	X	Command Input	Din	Active
L	H	L	⌐↓	H	X	Address Input (3clocks)	Din	Active
L	H	L	H	↓⌐	X	Address Output (3clocks)	Dout	Active
L	L	L	⌐↓	H	X	Data Input	Din	Active
L	L	L	H	↓⌐	X	Serial Read & Data Output	Dout	Active
X	X	X	X	X	H	During Program	High-Z	Active
X	X	X	X	X	H	During Erase	High-Z	Active
X	X	X	X	X	H	During Busy State	High-Z	Active
X	X[(1)]	X	X	X	L	Write Protect	High-Z	Active
X	X	H	X	X	0V/Vcc[(2)]	Stand-by	High-Z	Stand-by

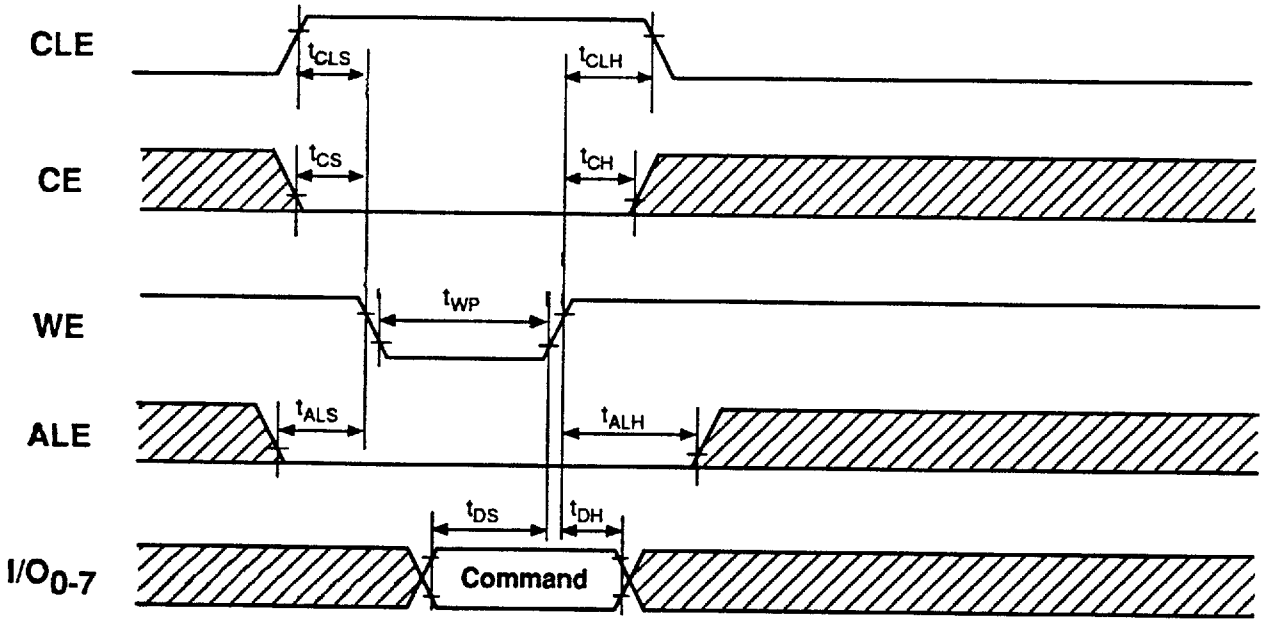
Notes : 1. X can be VIL or VIH

2. $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.

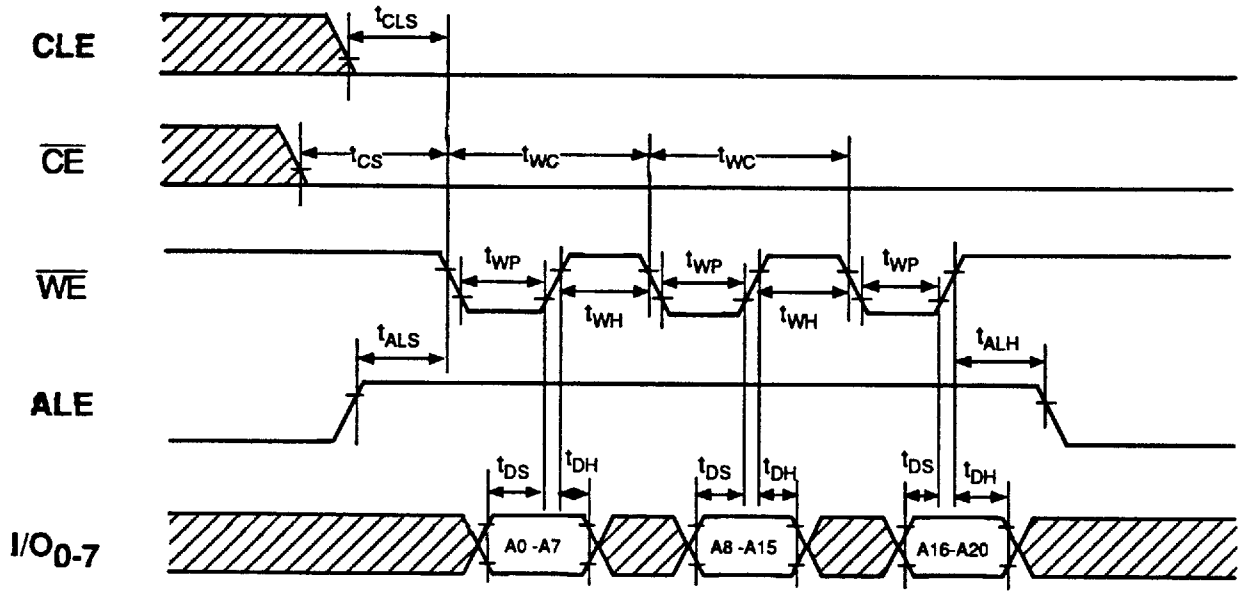
A.C. Characteristics for Command/Address/Data Input

Parameter	Symbol	Min	Max	Unit
CLE Set-up Time	t_{CLS}	20	-	ns
CLE Hold Time	t_{CLH}	40	-	ns
$\overline{CE}$ Setup Time	t_{CS}	20	-	ns
$\overline{CE}$ Hold Time	t_{CH}	40	-	ns
$\overline{WE}$ Pulse Width	t_{WP}	40	-	ns
ALE Set-up Time	t_{ALS}	20	-	ns
ALE Hold Time	t_{ALH}	40	-	ns
Data Set-up Time	t_{DS}	30	-	ns
Data Hold Time	t_{DH}	20	-	ns
Write Cycle Time	t_{WC}	80	-	ns
$\overline{WE}$ High Hold Time	t_{WH}	20	-	ns

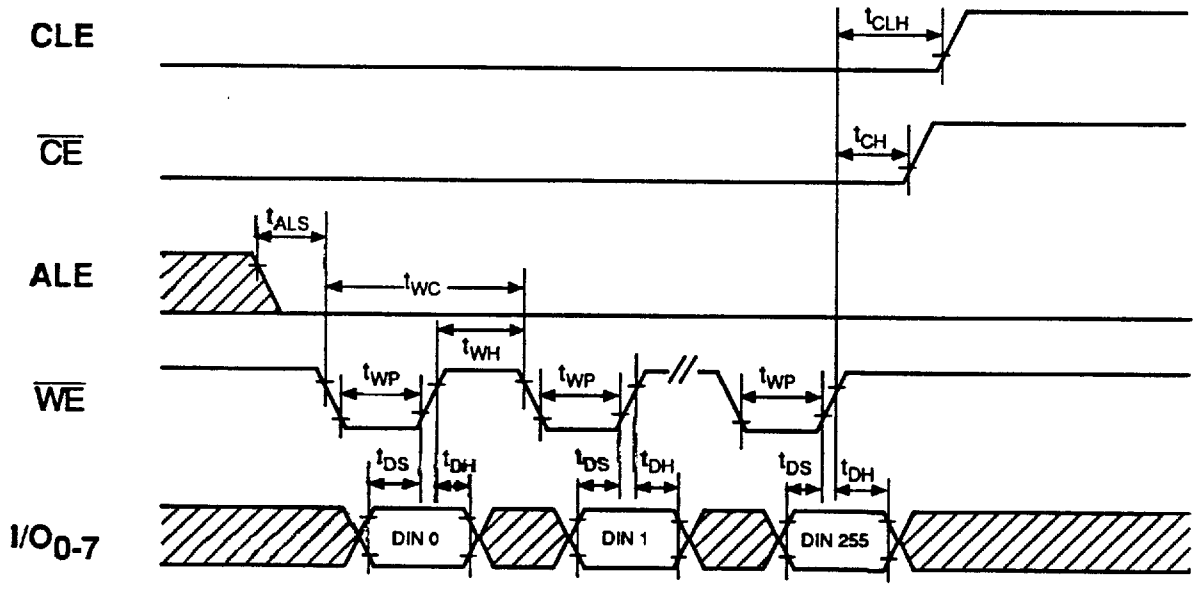
* Command Latch Cycle



* Address Latch Cycle



* Input Data Latch Cycle



A.C. Characteristics for Operation

Parameter	Symbol	Min	Max	Unit
Data Transfer from Cell to Register	t_R	-	20	µs
ALE to $\overline{RE}$ Delay	t_{AR}	150	-	ns
$\overline{CE}$ low to $\overline{RE}$ low (add. register read, ID read)	t_{CR}	200	-	ns
Ready to $\overline{RE}$ Low	t_{RR}	20	-	ns
$\overline{WE}$ High to Busy	t_{WB}	-	200	ns
Read Cycle Time	t_{RC}	80	-	ns
$\overline{RE}$ Access Time	t_{REA}	-	45	ns
$\overline{RE}$ High to Output Hi-Z	t_{RHZ}	5	20	ns
$\overline{CE}$ High to Output Hi-Z	t_{CHZ}	-	30	ns
$\overline{RE}$ High Hold Time	t_{REH}	20	-	ns
Output Hi-Z to $\overline{RE}$ Low	t_{IR}	0	-	ns
Last $\overline{RE}$ High to Busy (at sequential read)	t_{RB}	-	200	ns
$\overline{CE}$ High to Ready (in case of interception by $\overline{CE}$ at read)(1)	t_{CRY}	-	100 + tr(R/$\overline{B}$)(2)	ns
$\overline{CE}$ High Hold Time (at the last serial read) (3)	t_{CEH}	250	-	ns
$\overline{RE}$ Low to Status Output	t_{RSTO}	-	45	ns
$\overline{CE}$ Low to Status Output	t_{CSTO}	-	55	ns
$\overline{RE}$ High to $\overline{WE}$ Low	t_{RHW}	0	-	ns
$\overline{WE}$ High to $\overline{CE}$ Low	t_{WHC}	50	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low	t_{WHR}	50	-	ns
Erase Suspend Input to Ready	t_{SR}	-	1	ms
Device Resetting Time (Read/Program/Erase/after erase suspend)	t_{RST}	-	5/10/500/5	µs

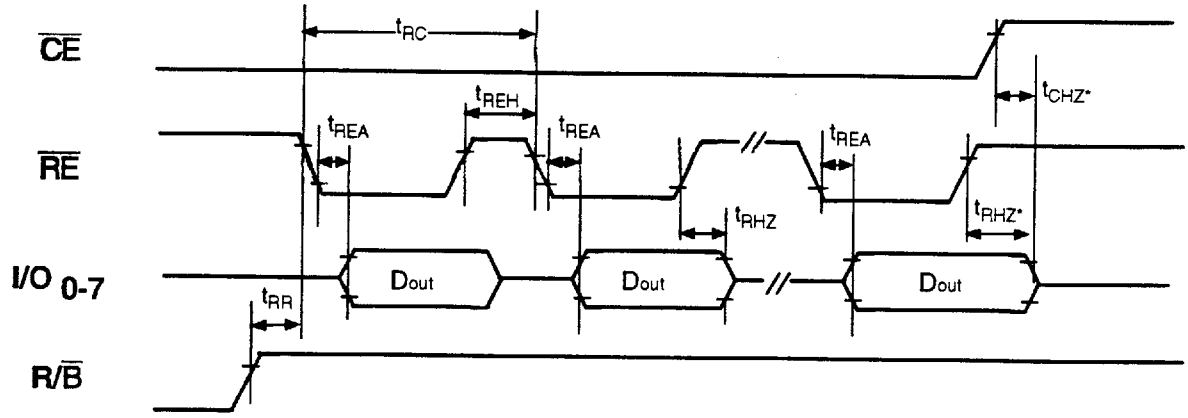
Note:
1. If $\overline{CE}$ goes high within 30ns after the rising edge of the last $\overline{RE}$, R/$\overline{B}$ will not transition to VOL.
2. The time to Ready depends on the value of the pull-up resistor tied to R/$\overline{B}$ pin.
3. To break the sequential read cycle, $\overline{CE}$ must be held high for longer than t_{CEH}

Program/Erase Characteristics

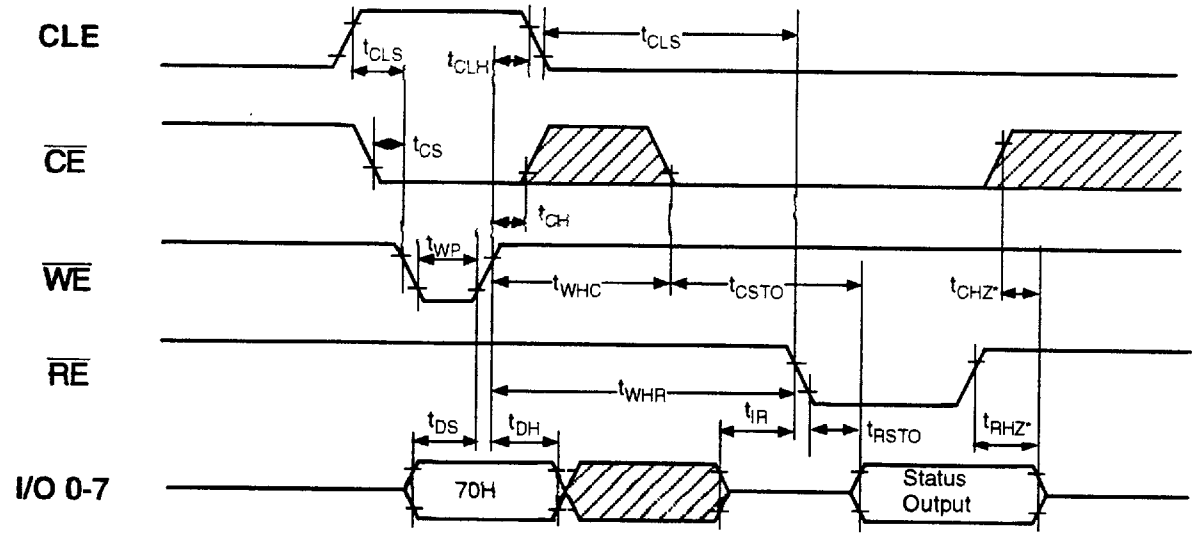
Parameter	Symbol	Min	Typ	Max	Unit
Program Time	t_{PROG}	-	0.3	2	ms
Number of Partial Program Cycles in the Same Page	Nop	-	-	10	cycles
Block Erase Time	t_{BERS}	-	6	100	ms
Multi-Block Erase Time	t_{MBERS}	-	(1)	130	ms

Note : 1. Depends on the number of blocks to be erased.

* Serial Out Cycle after Read (CLE, ALE = L, $\overline{WE}$ = H)

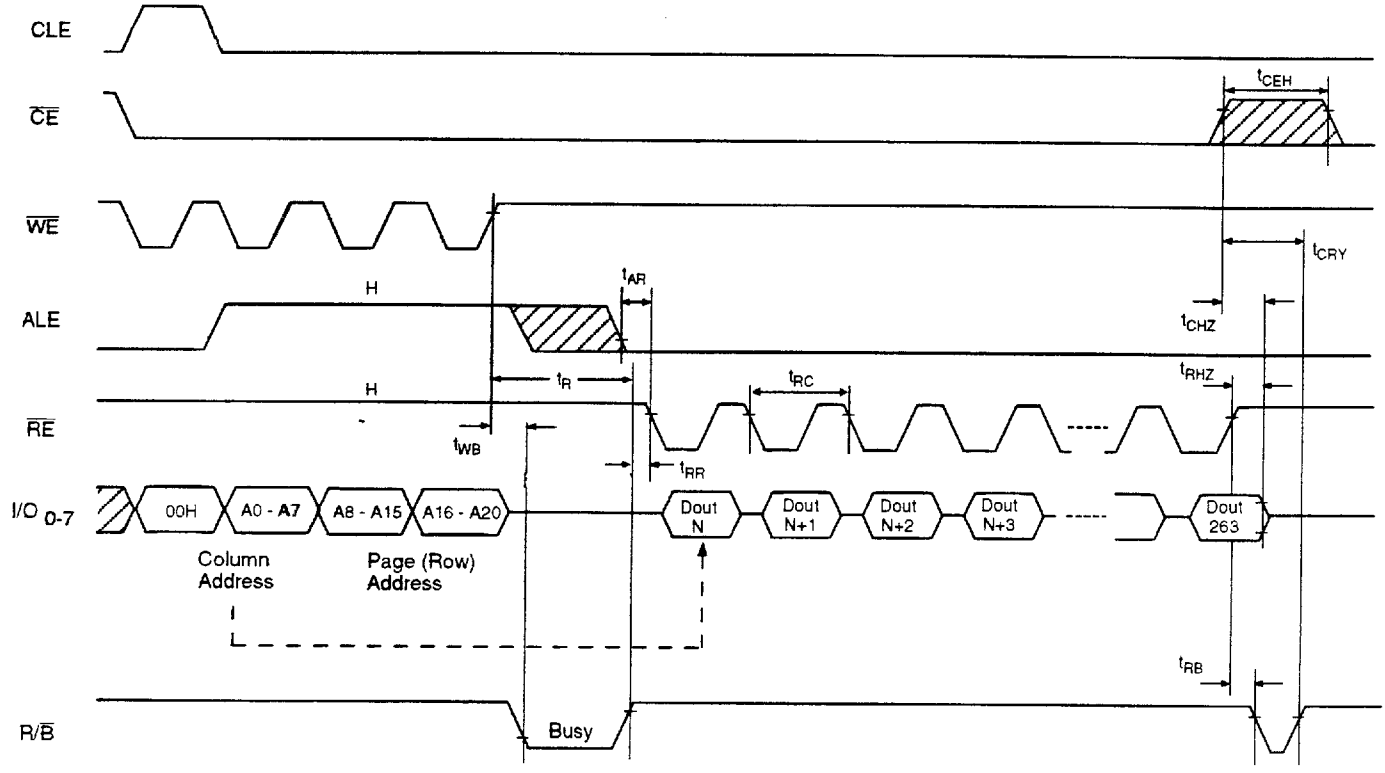


* Status Read Cycle

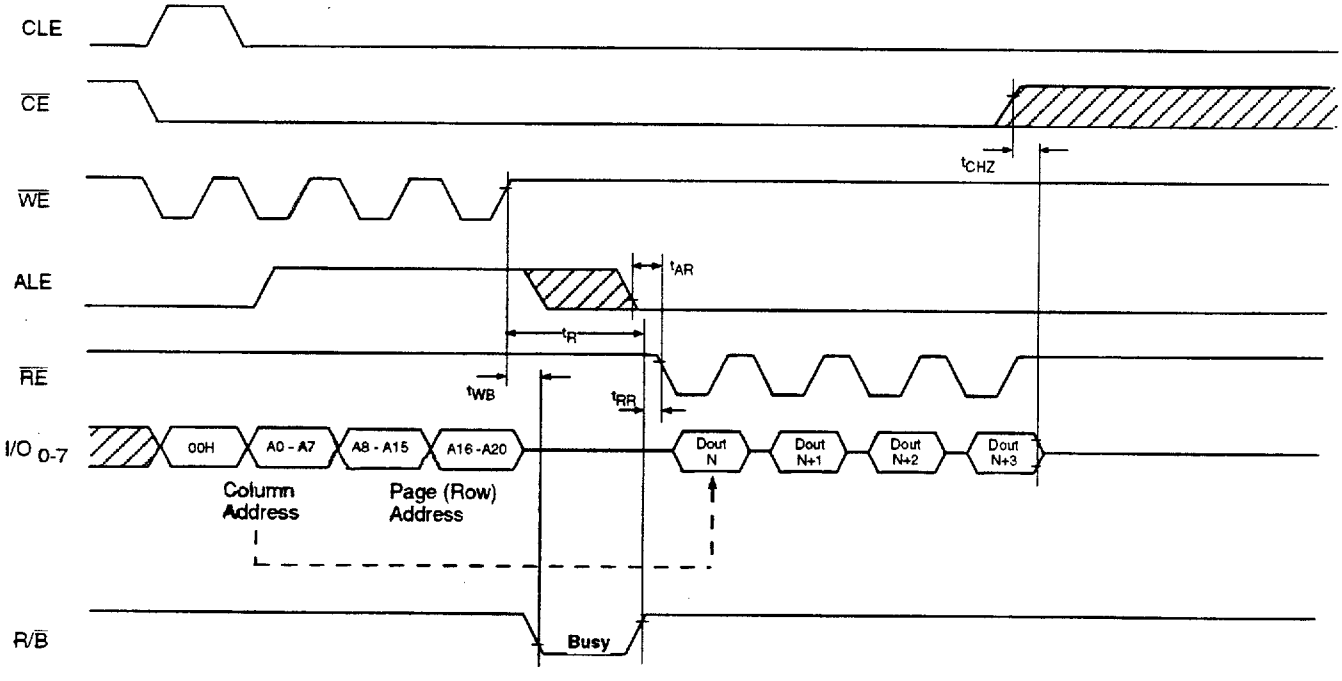


Note : Transition is measured ± 200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.

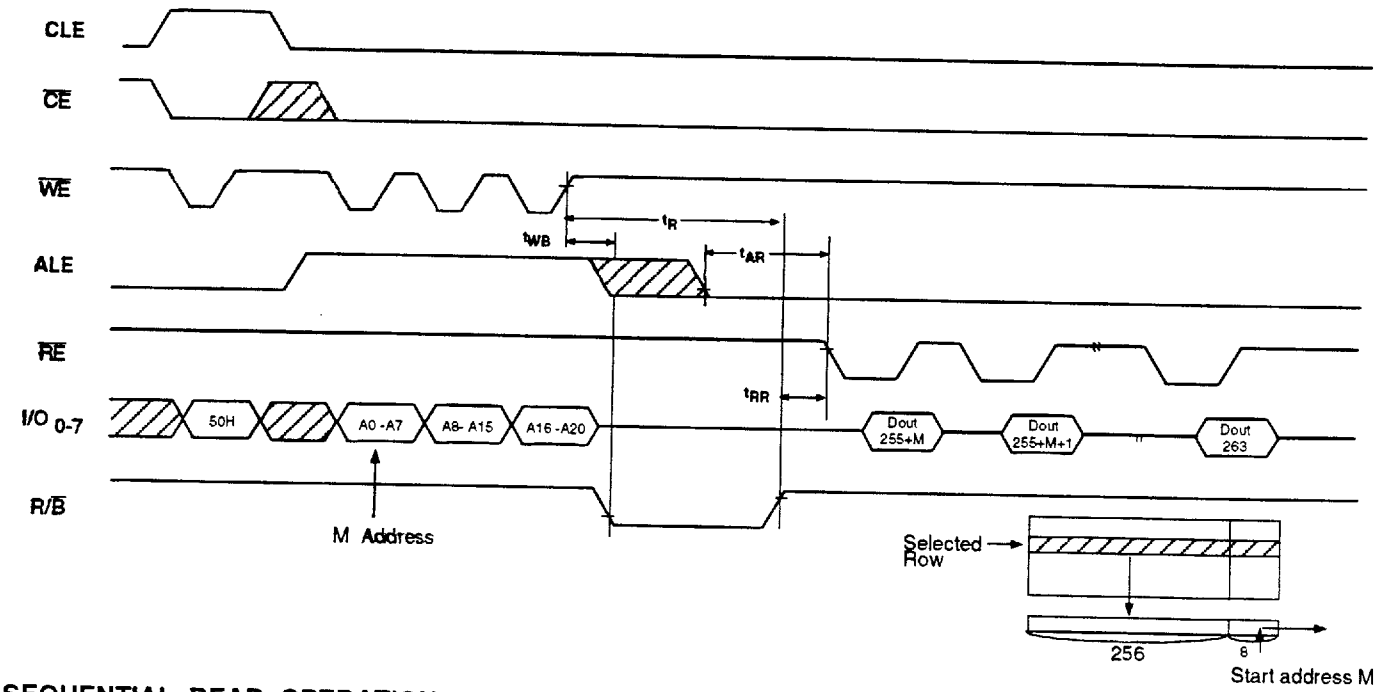
READ1 OPERATION (READ ONE PAGE)



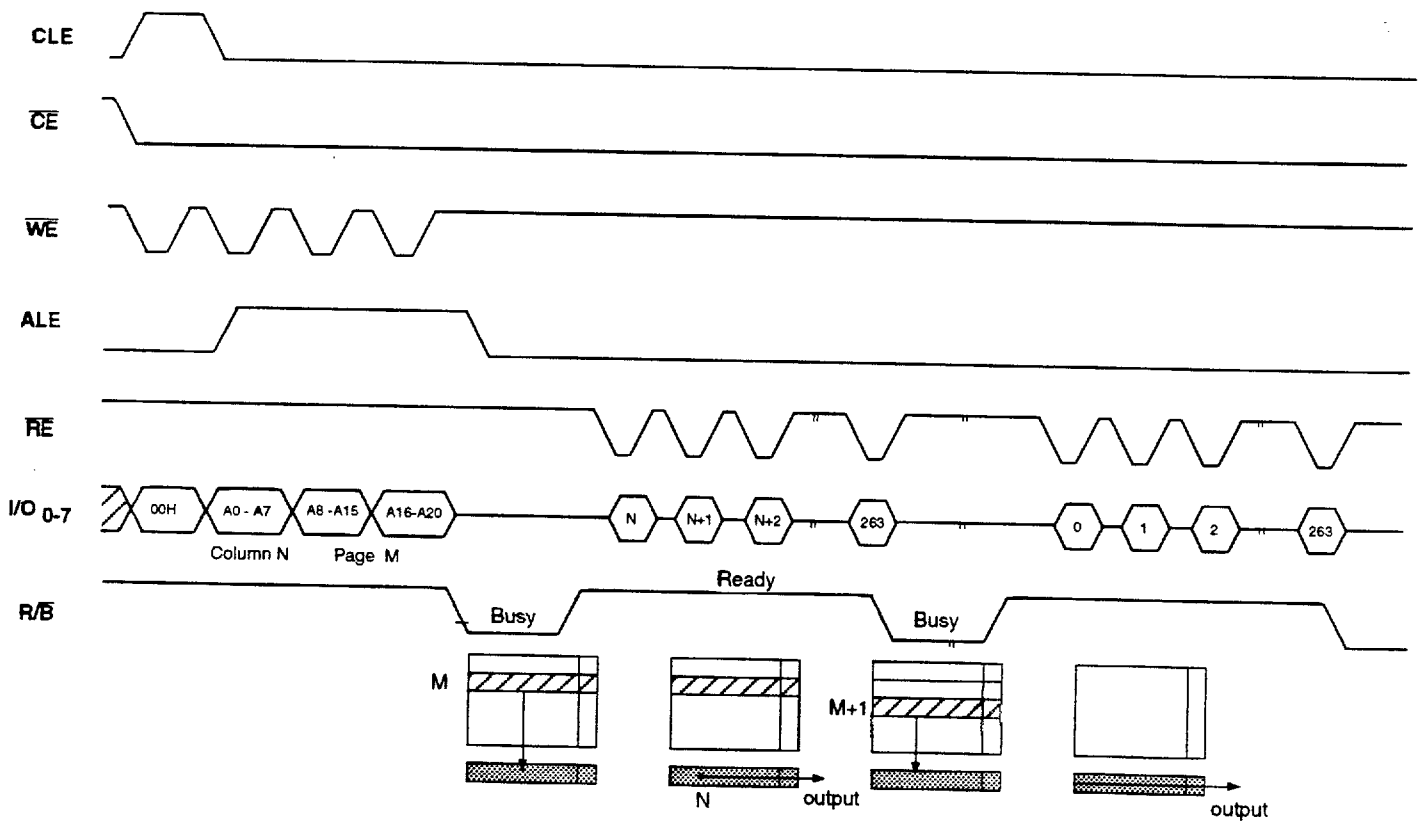
READ1 OPERATION (INTERCEPTED BY CE)



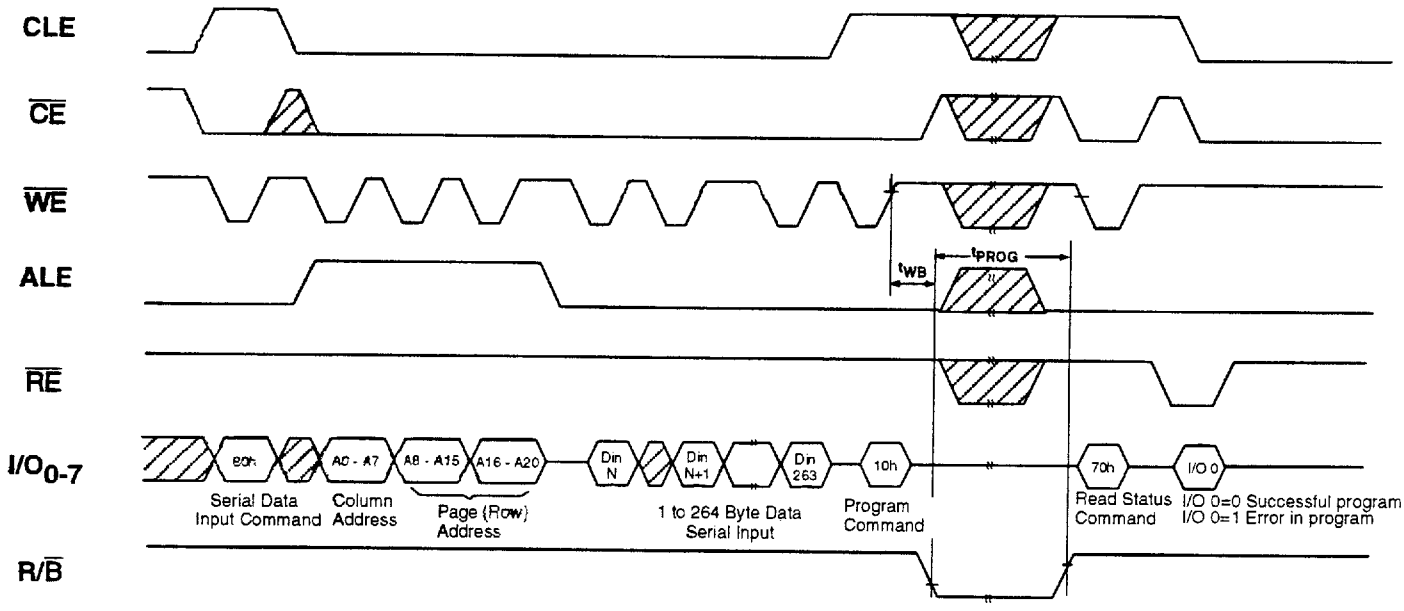
READ2 OPERATION (READ SPARE AREA)



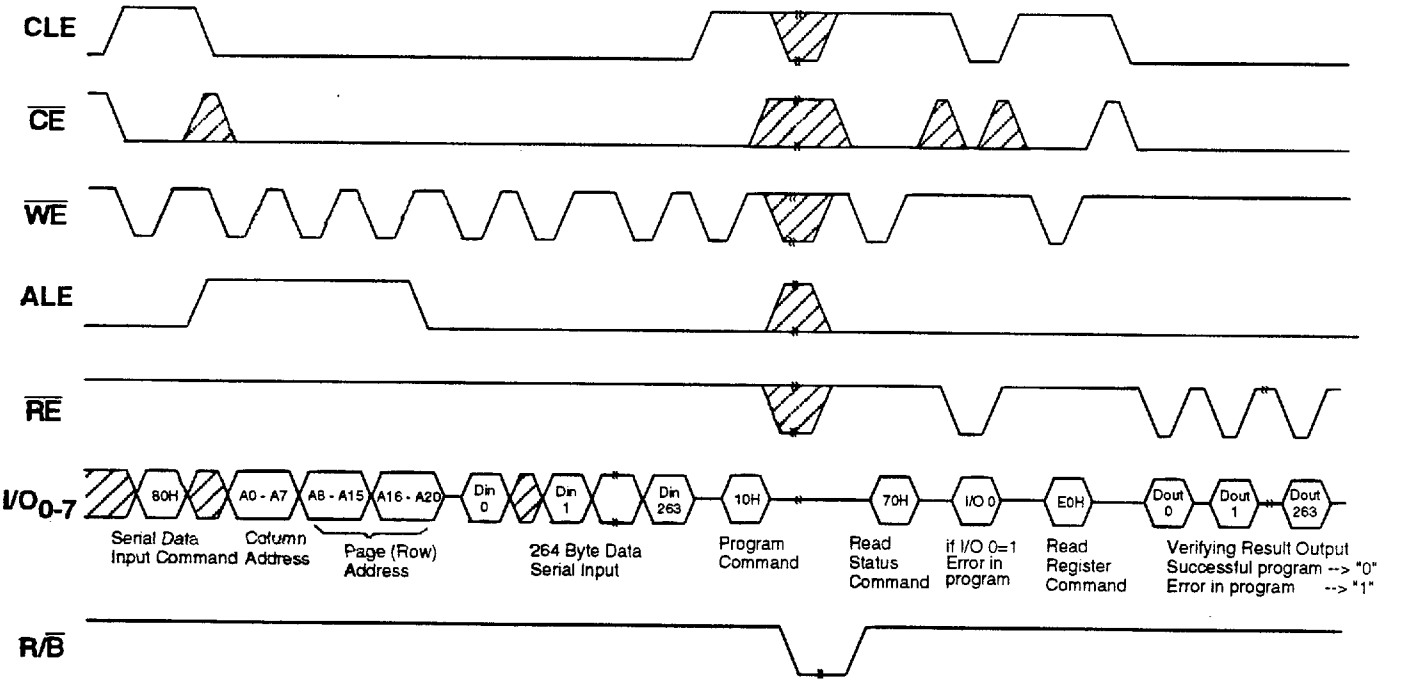
SEQUENTIAL READ OPERATION



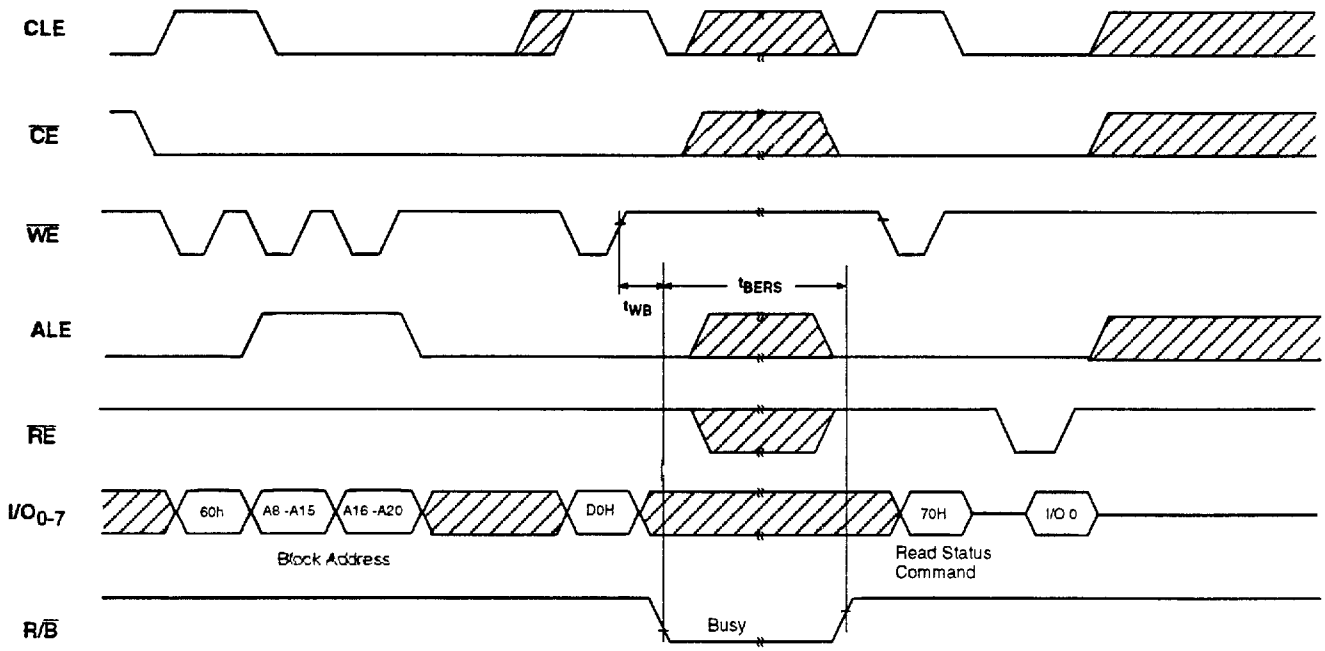
PAGE PROGRAM OPERATION



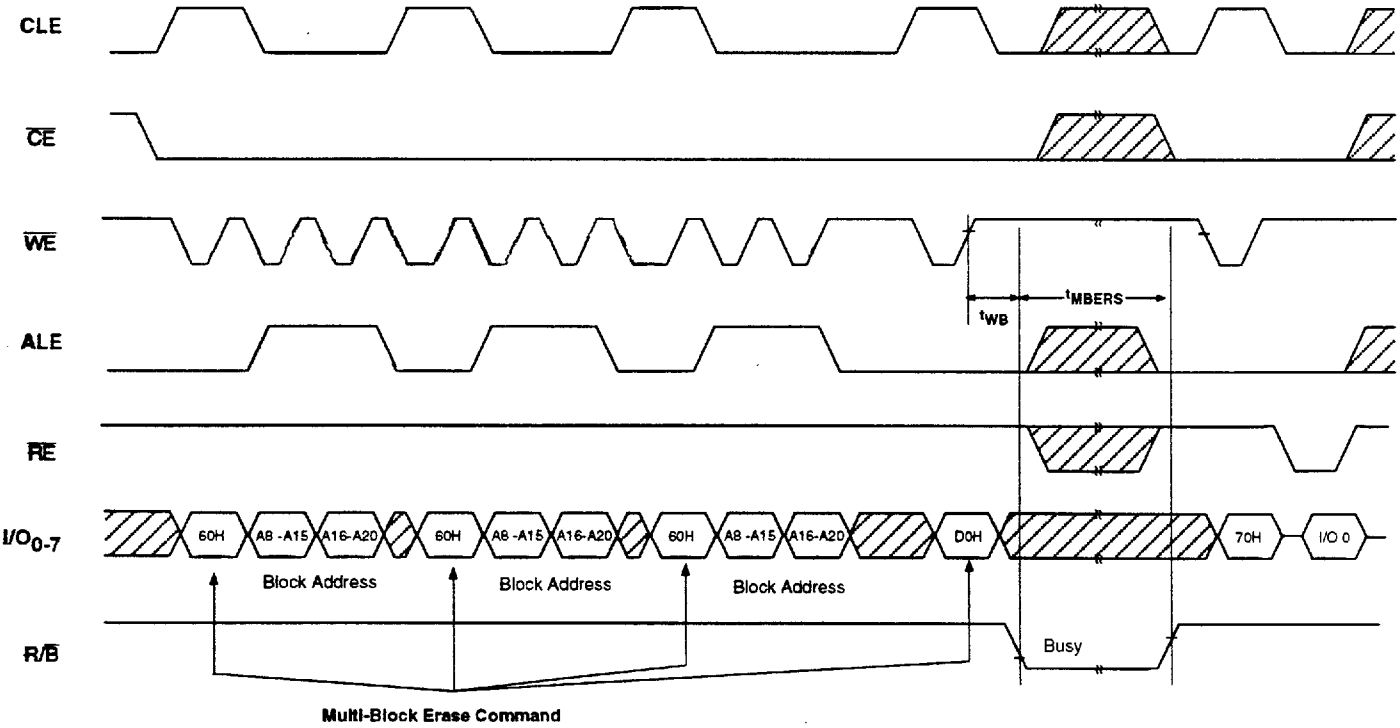
PAGE PROGRAM & READ DATA REGISTER OPERATION



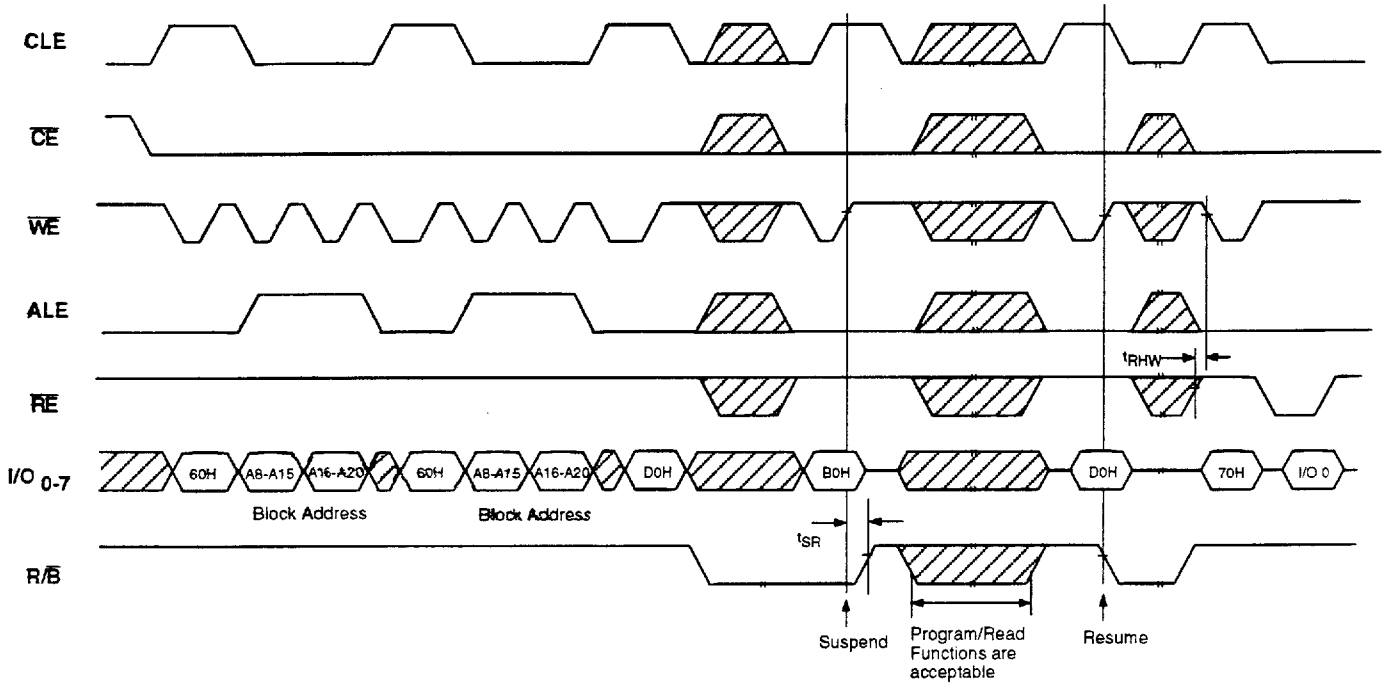
BLOCK ERASE OPERATION (ERASE ONE BLOCK)



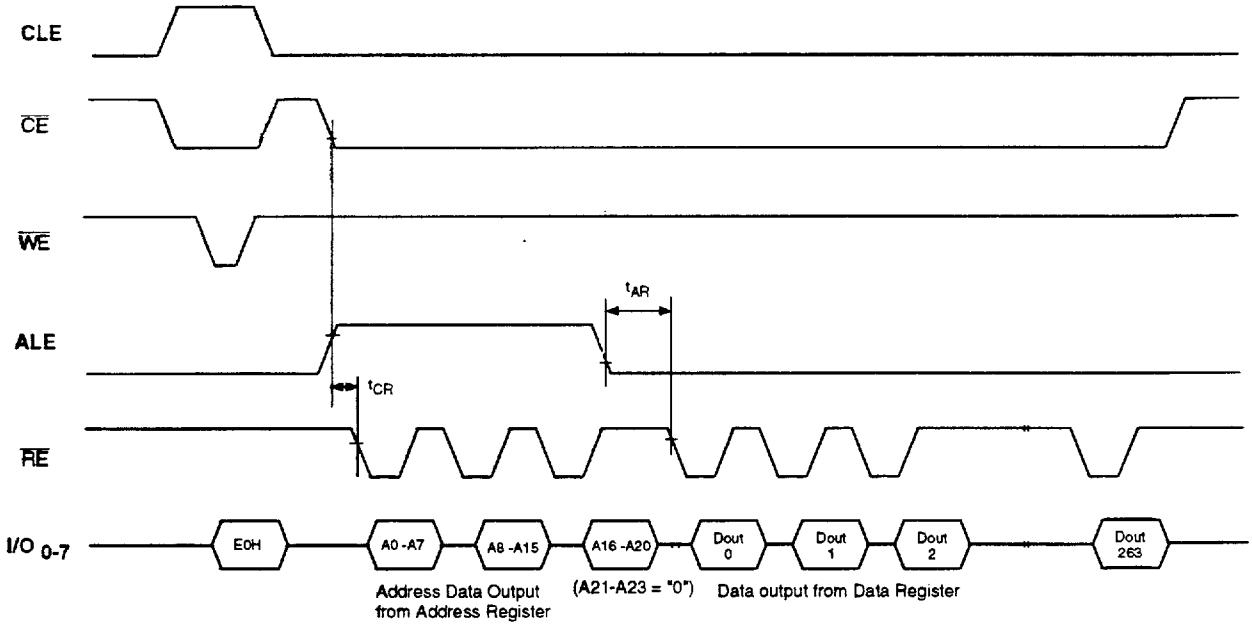
MULTI-BLOCK ERASE OPERATION (512 max. BLOCK)



SUSPEND & RESUME OPERATION DURING MULTI-BLOCK ERASE OPERATION



READ REGISTER OPERATION



DEVICE OPERATION

PAGE READ

Upon initial device power up, the KM29N16000 defaults to the Read1 mode. This operation is also initiated by writing 00H to the command register along with three address cycles. Once the command is latched, it does not need to be written for the following page read operation. Three types of operations are available: random read, serial page read and sequential read.

The random read mode is enabled when the page address is changed or $\overline{CE}$ is clocked. 264 bytes of data within the selected page are transferred to the data registers in less than 20μs (tR). The CPU can detect the completion of this data transfer (tR) by analyzing the output of the Ready/Busy pin. Once the data in a page is loaded into the registers, they may be read out in 80 ns cycle time by sequentially pulsing $\overline{RE}$ with $\overline{CE}$ staying low. High to low transitions of the $\overline{RE}$ clock output the data starting from the selected column address up to the last column address (column 264). After the data of the last column address is clocked out, the next page is automatically selected for sequential read. Waiting 20μs again allows for reading of the selected page. The sequential read operation is terminated by bringing $\overline{CE}$ high. The way the Read1 and Read2 commands work is like a pointer set to either the main area or the spare area. The spare area of bytes 256 to 263 may be selectively accessed by writing the Read2 command. Address A0 to A2 set the starting address of the spare area while addresses A3 to A7 are ignored. Unless the operation is aborted, the page address is automatically incremented for sequential read as in Read1 operation and the spare eight bytes of each page may be serially read. The Read1 command (00H) is needed to move the pointer to the main area. Figures 3 thru 6 show typical sequences and timing for each read operation.

Figure 3. Read 1 Operation (Page Read)

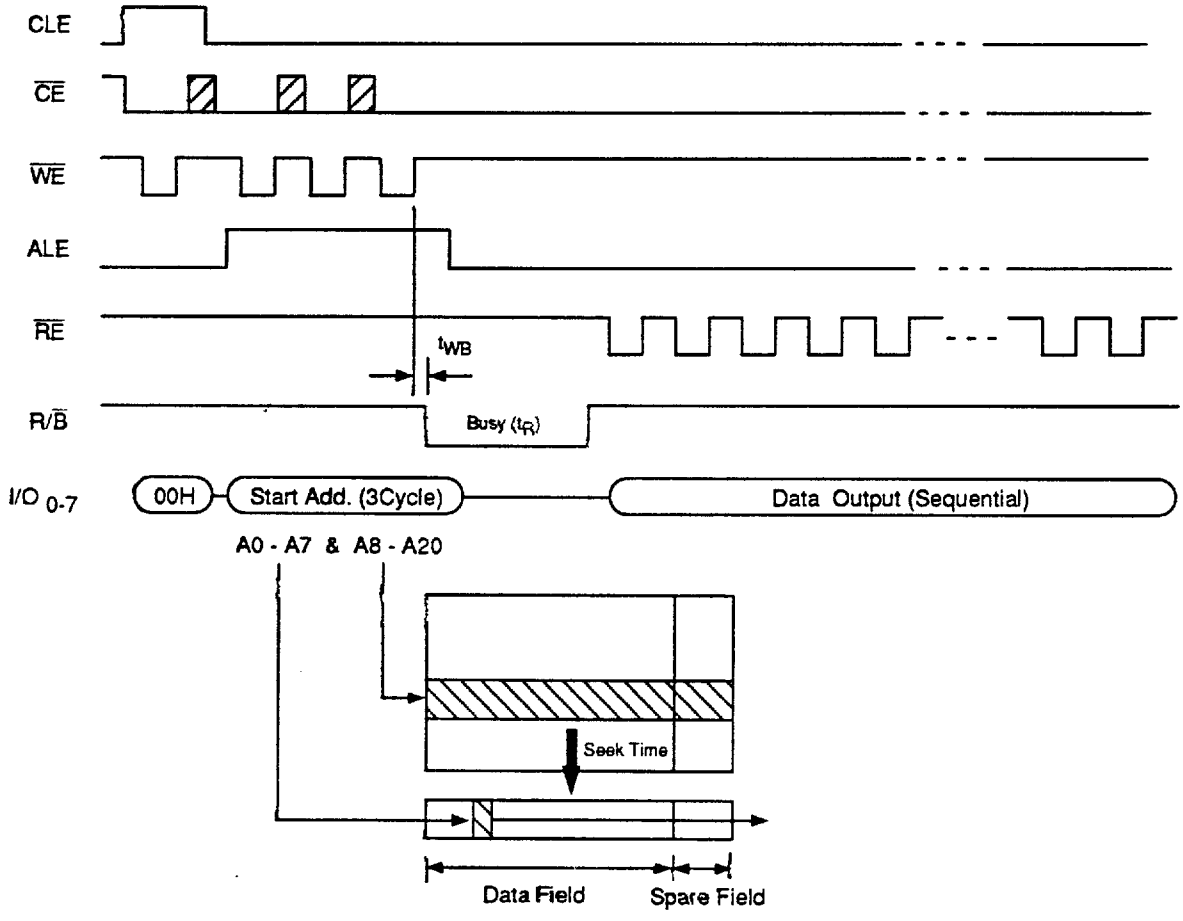


Figure 4. Read 2 Operation (Spare field)

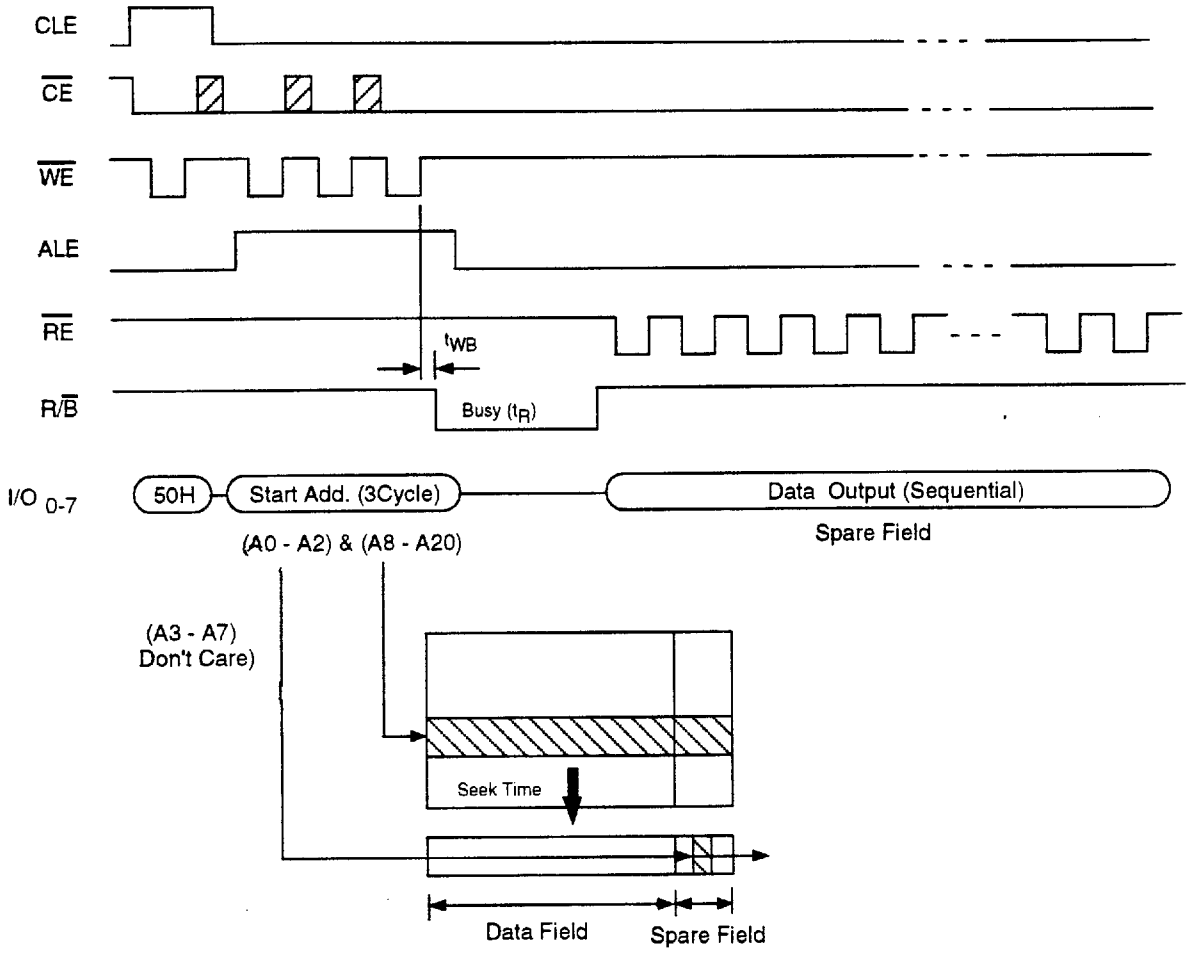


Figure 5. Sequential Read 1 Operation

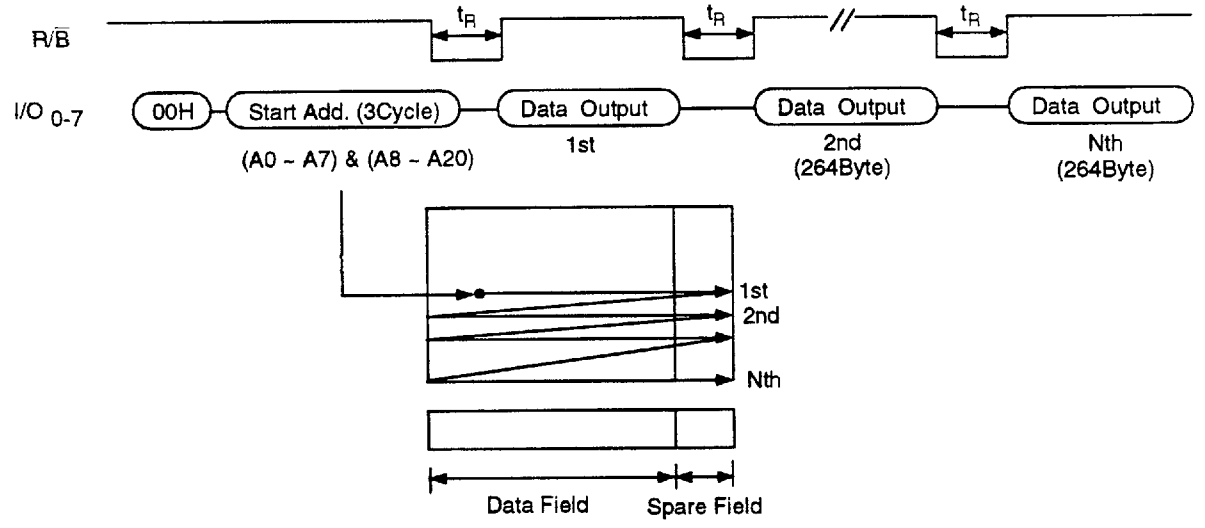
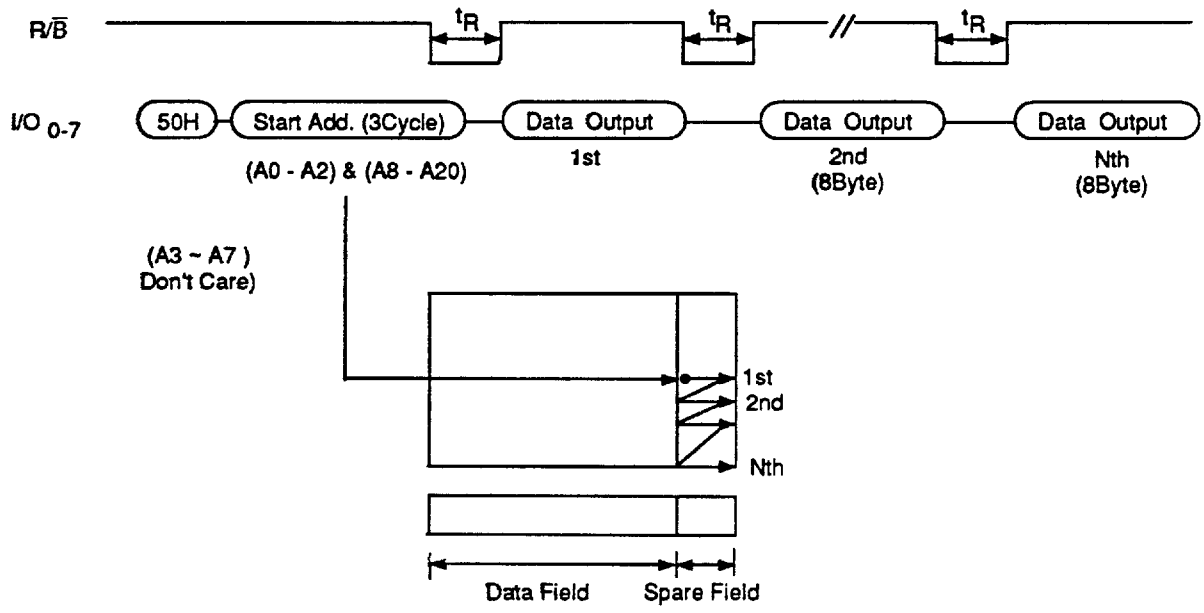


Figure 6. Sequential Read 2 Operation



PAGE PROGRAM

The device is programmed basically on a page basis, but does allow partial page programming of a byte or consecutive bytes up to 264, in a single page program cycle. The number of consecutive partial page programming operations within the same page without an intervening erase operation must not exceed ten. The addressing may be done in random order in a block. A page program cycle consists of a serial data loading period in which up to 264 bytes of data may be loaded into the page register, followed by a nonvolatile programming period where the loaded data is programmed into the appropriate cell.

The serial data loading period begins by inputting the Serial Data Input command (80H), followed by the three cycle address input and then serial data loading. The bytes other than those to be programmed do not need to be loaded. To program the bytes in the spare columns (256 to 263), the pointer should be set to the spare area by writing the Read 2 command (50H) to the command register. The pointer remains in the spare area unless the Read1 command (00H) is entered returning it to the main area. The Page Program confirm command (10H) initiates the programming process. Writing 10H alone without previously entering the serial data will not initiate the programming process. The internal write controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the CPU for other tasks. Once the program process starts, the Read Status Register command may be entered, with $\overline{RE}$ and $\overline{CE}$ low, to read the status register.

The CPU can detect the completion of a program cycle by monitoring the Ready/Busy output, or the Status bit(I/O_6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Programming is complete, the Write Status Bit (I/O_0) may be checked (Figure 7). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register. The data register may be read by writing the Read Register command (E0H) to determine the column address at which the error has been detected. The registers in error will have "1"s while the registers of successfully programmed bits will have "0"s (Figure 8).

Figure 7. Program & Read Status Operation

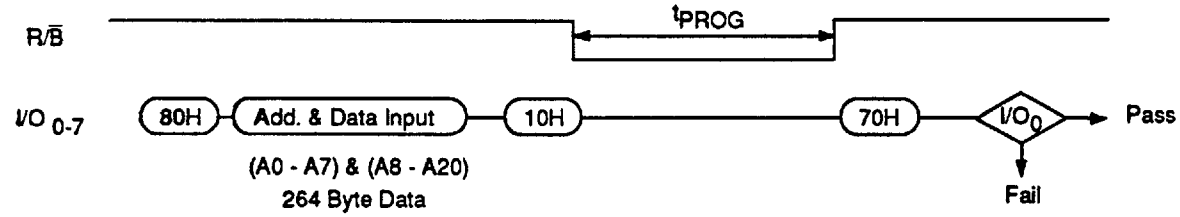
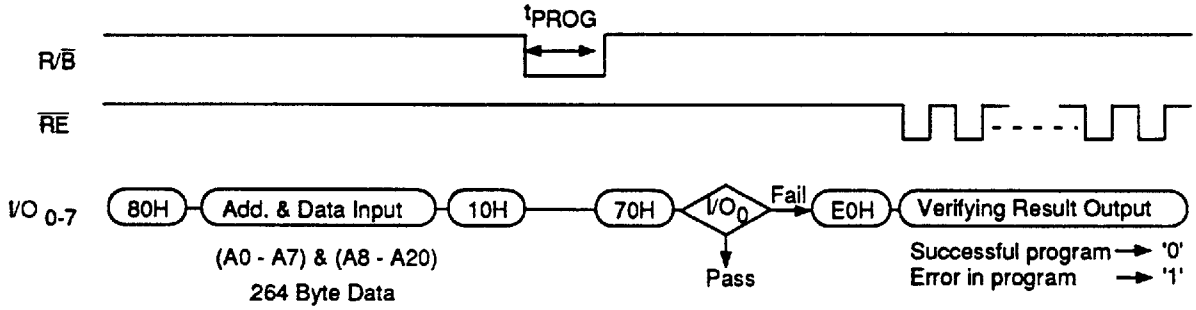


Figure 8. Program & Read Data Register Operation



BLOCK ERASE/MULTI BLOCK ERASE

The Erase operation can erase up to 512 blocks at a time, and consists of a block address loading period and an erase period. Block address loading is accomplished in two cycles initiated by an Erase Setup command (60H). Only addresses A_{12} to A_{20} are valid while A_8 to A_{11} are ignored. For Multi Block Erase, the erase setup command (60H) must precede each block address loading. The addresses of the blocks to be erased to FFH need not be loaded in sequential order and can be reloaded within a loading period. The Erase Confirm command (D0H) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution ensures that the memory contents are not accidentally erased due to external noise conditions.

At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase, erase-verify and pulse repetition where required. The time to erase multiple blocks (t_{MBERS}) depends on the number of blocks to be erased. While the actual erasing operation is simultaneously done for the loaded blocks, the internal verify after erase is sequentially processed block by block. If an erase operation error is detected, the internal verify is halted and the erase operation is terminated. All subsequent blocks are not verified. When the erase operation is complete, the Write Status Bit (I/O 0) can be checked. Figure 9 and 10 detail the sequence.

Figure 9. Block Erase Operation

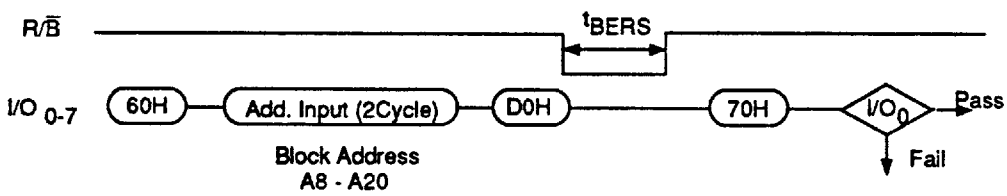
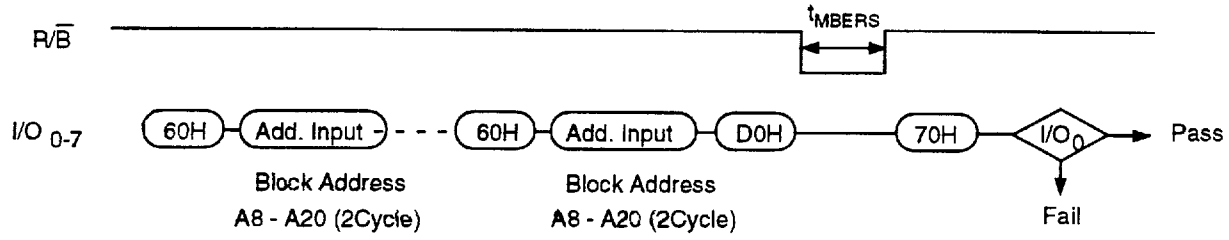


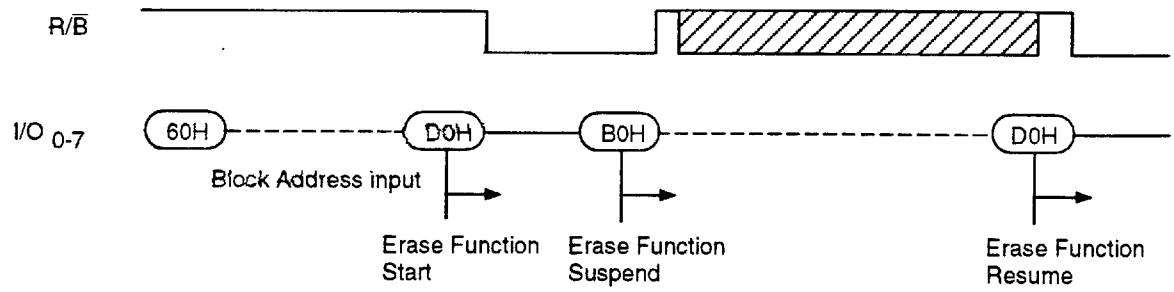
Figure 10. Multi-Block Erase Operation



ERASE SUSPEND/ERASE RESUME

The Erase Suspend allows interruption during any erase operation in order to read or program data to or from another block of memory. Once an erase operation begins, writing the Erase Suspend command (B0H) to the command register suspends the internal erase process, and the Ready/Busy signal returns to "1". The Erase Suspend Status bit will also be set to "1" when the Status Register is read. During this time, blocks other than the suspended block can only be read or programmed. The Status Register and Ready/Busy operations will function as usual. After the Erase Resume command is sent, the erase process will restart from the beginning and the Erase Suspend Status bit and Ready/Busy signal will return to "0". Refer to Figure 11 for operation sequence.

Figure 11. Erase Suspend & Erase Resume Operation



READ STATUS

The KM29N16000 contains a Status Register used to monitor the Ready/Busy status of the device, to show pass/fail conditions of a program or erase operation and to determine if the device is in a protect or suspend mode. After writing the 70H command to the command register, a read cycle outputs the contents of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to table 2 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the Status Register is read during a random read cycle, the required Read command (00H or 50H) should be sent before the serial page read cycle.

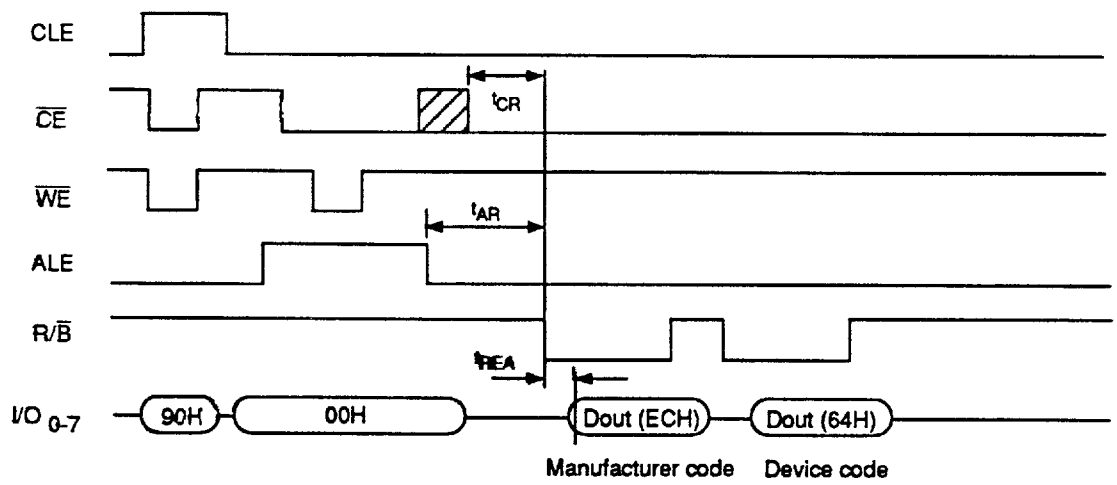
Table 2. STATUS REGISTER DEFINITION

SR Bit	Status	Definition
I/O 0	Program / Erase	"0" : Successful Program/Erase
		"1" : Error in Program/Erase
I/O 1	Reserved for Future Use	"0"
I/O 2		"0"
I/O 3		"0"
I/O 4		"0"
I/O 5	Erase Suspend	"0" : Erase in Progress/Completed
		"1" : Suspended
I/O 6	Device Operation	"0" : Busy "1" : Ready
I/O 7	Write Protect	"0" : Protected "1" : Not Protected

READ ID

The KM29N16000 contains a product identification mode, initiated by writing 90H to the command register, followed by an address input of 00H. Two read cycles sequentially output the manufacturer code (ECH), and the device code (64H) respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 12 shows the operation sequence.

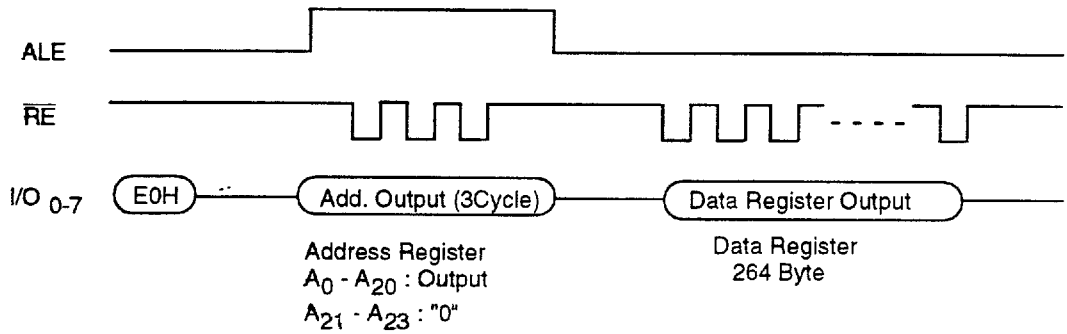
Figure 12. Read ID Operation



READ REGISTER

The KM29N16000 has 264 data registers and 3 address registers which may be read by writing E0H to the command register. Toggling $\overline{RE}$ with ALE high will output the contents of the address registers on the I/O pins. Toggling $\overline{RE}$ with ALE low drives the contents of the data registers sequentially beginning with data register 0. The Read Register mode can be used in conjunction with the Page Program operation to identify the bits in programming error by reading the data registers. Figure 13 shows the timing sequence.

Figure 13. Read Address and Data Register Operation



RESET

The KM29N16000 offers a reset feature, executed by writing FFH to the command register. When the device is in the Busy state during a random read, program or erase mode, the reset command will abort these operations. The content of the memory cells being altered are no longer valid, as the data will be partially programmed or erased. Internal address registers are cleared to "0"s and data registers to "1"s. The command register is cleared to wait for the next command and the Status Register is cleared to a value of C0H when $\overline{WP}$ is high. Refer to table 3 for device status after reset operation. If the device is already in the reset state, a new reset command will not be accepted by the command register. The Ready/Busy pin transitions to low for t_{RST} after the Reset command is written. Sending a Reset command is not necessary for normal device operation. Refer to Figure 14 below.

Figure 14. RESET Operation

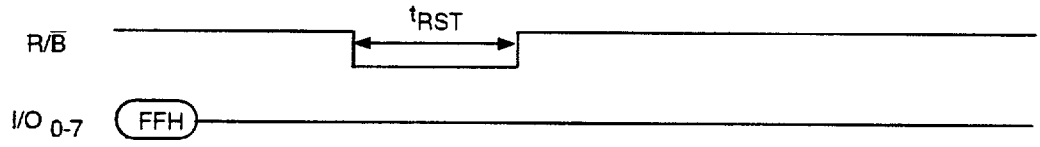


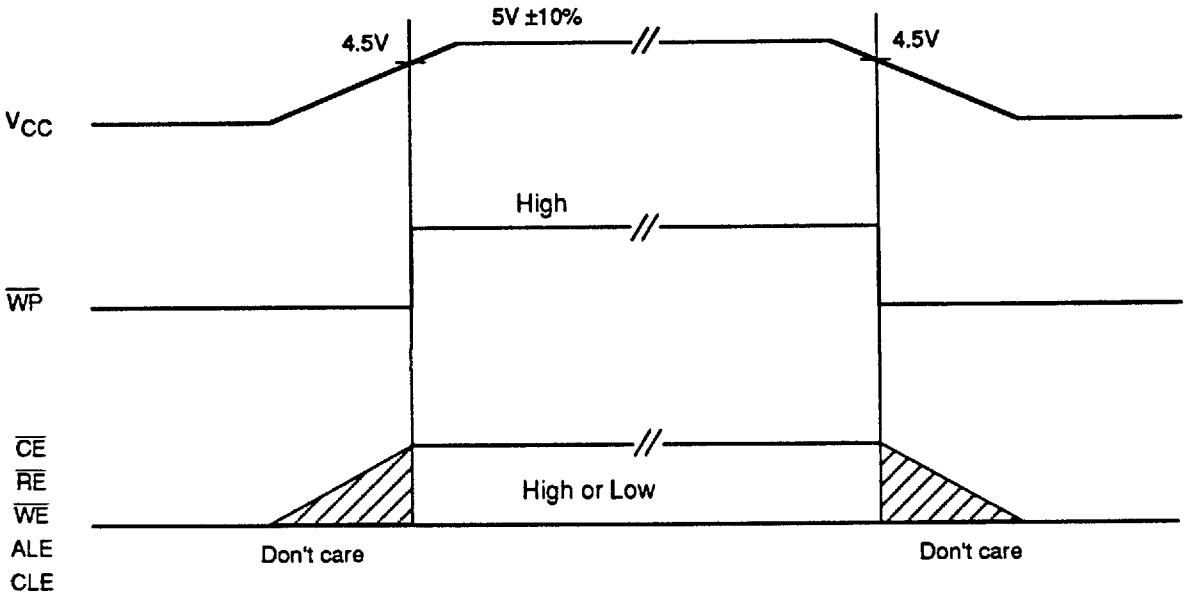
Table 3. DEVICE STATUS

	After Power-up	After Reset
Address Register	All "0"	All "0"
Data Register	All "1"	All "1"
Operation Mode	Read 1	Waiting for next command

DATA PROTECTION

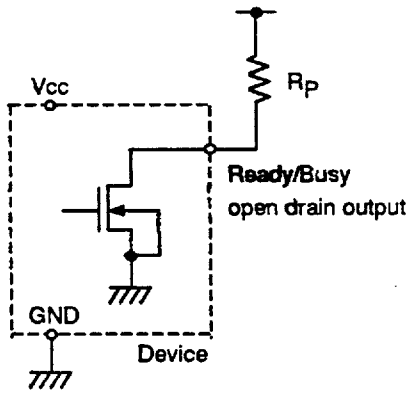
The KM29N16000 has a write protect pin ($\overline{WP}$) to provide protection from any involuntary write operation during power transitions. During device powerup, the $\overline{WP}$ pin should be at V_{IL} until V_{CC} reaches approximately 4.5V, and during power down should be at V_{IL} when V_{CC} falls below 4.5V. Refer to Figure15 below.

Figure 15. AC WAVEFORMS for POWER TRANSITIONS



READY/BUSY

The KM29N16000 has a Ready/Busy output that provides a hardware method of indicating the completion of a page program, erase or random read operation. The R/ $\overline{B}$ pin is normally high but transitions to a low after a program or erase command is written to the command register or a random read is begun after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more Ready/Busy outputs to be Or-tied. An appropriate pull-up resistor is required for proper operation and the value may be calculated by the following equation.



$$Rp = \frac{Vcc(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{5.1V}{8mA + \Sigma I_L}$$

where I_L is the sum of the input currents of all devices tied to the Ready/Busy pin.

KM29N16000 Technical Notes

INVALID BLOCKS

Typically, the KM29N16000 Flash device contains 512 usable blocks. Due to the nature of the device architecture, the device can also be screened and tested for partial invalid blocks for selected systems that can utilize the devices. These devices will have the same quality levels as devices with all valid blocks and will meet all AC and DC characteristics. The system design must be able to mask out the partial block(s) from address mapping. An invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor.

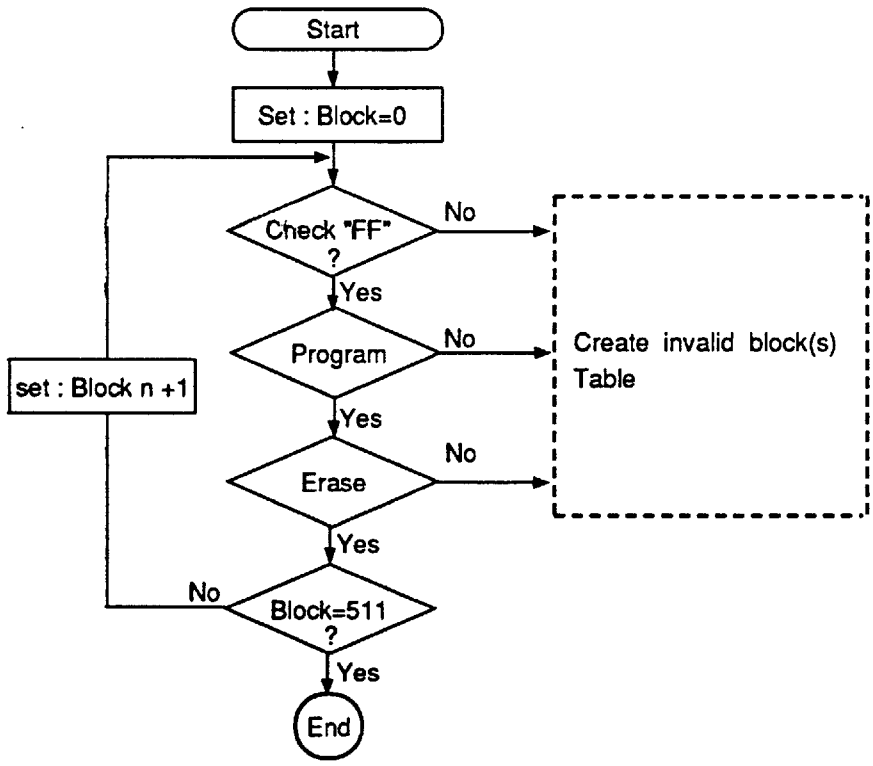
Ordering part numbers and respective valid blocks

	KM29N16000T / R		KM29N16000TS / RS	Units
	Min.	Max.		
Valid Block Number	502	511	512	Blocks

Identifying Invalid Block(s) in the KM29N16000T / R

All device locations are erased (FFH) prior to shipping. Devices with invalid Block(s) will be randomly written with 00H data within a page in the invalid Block(s). This page may or may not contain the invalid cell(s). The 00H data marks the block(s) that contain the invalid cell(s). A system that can utilize these devices must be able to recognize invalid block(s) via the following suggested flow chart (Figure 1).

Figure 1 Flow chart to create invalid block table.

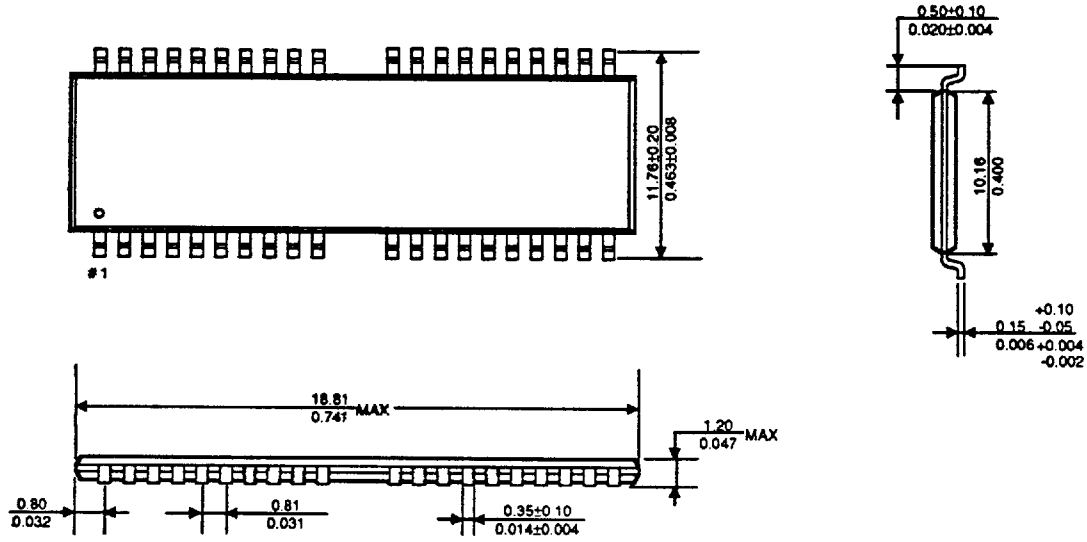


PACKAGE DIMENSION

44 (40) LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II)

Unit : mm/inch

44(40)-TSOP2-400F



44(40)-TSOP2-400R