256-Bit Serial Electrically Erasable PROM

FEATURES

- **Operating temperature range**
  - **KM93C06: Commercial**
  - **KM93C06I: Industrial**
- **16 x 16 serial read/write memory**
- **High performance advanced CMOS technology**
- **Reliable floating gate technology**
  - **Endurance : 100,000 cycle/byte**
  - **Data retention: 10 years**
- **Single 5 Volt supply**
- **Low power dissipation**
  - **Standby current: 250μA (TTL)**
  - **Active current: 3 mA (TTL)**
- **TTL compatible**
- **Available in plastic DIP and SOP**

GENERAL DESCRIPTION

The KM93C06 is a CMOS 5V Only 256 bit non-volatile, sequential EEPROM. It is fabricated with the well defined floating gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

The KM93C06 is organized as 16 registers of 16 bits each, which can be read/written serially by a microprocessor.

The KM93C06 is designed for applications up to 100,000 erase/write cycles per word and over 10 years of data retention.

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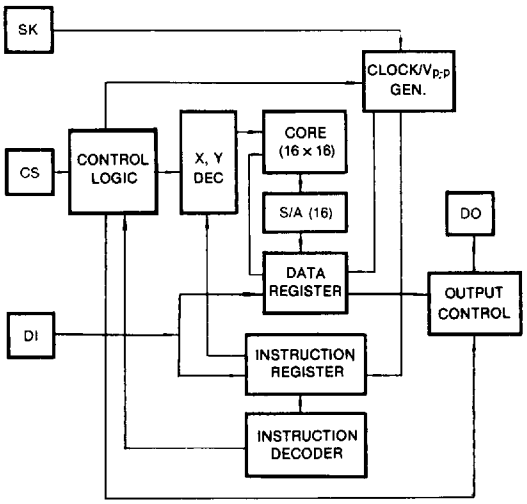
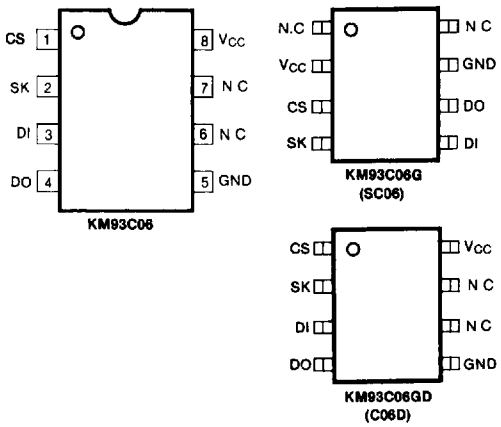
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin Name	Pin Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
N.C.	No Connection
V_{CC}	Power Supply
GND	Ground

ABSOLUTE MAXIMUM RATINGS*

Item		Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}	−0.3 to 7.0	V
Temperature Under Bias	Commercial	T_{bias}	−10 to +125	°C
	Industrial		−65 to +150	
Storage Temperature		T_{stg}	−65 to +150	°C

*Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of the data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

KM93C06: $T_A = 0°C$ to $70°C$, Voltages referenced to V_{SS}
KM93C06I: $T_A = -40°C$ to $85°C$, Voltages referenced to V_{SS}

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Voltage	V_{CC}		4.5	5.5	V
Operating Current (DC)	I_{CC1}	$V_{CC} = 5.5V$, CS = 2.0V, SK = 2.0V		1	mA
Operating Current (AC)	I_{CC2}	$V_{CC} = 5.5V$, $f_{SK} = 1MHz$		3	mA
Standby Current (TTL)	I_{SB1}	$V_{CC} = 5.5V$, CS = 0.8V		250	μA
Standby Current (CMOS)	I_{SB2}	$V_{CC} = 5.5V$, CS = 0V		100	μA
Input Voltage Levels	V_{IL} V_{IH}		−0.3 2.0	0.8 $V_{CC}+0.3$	V V
Output Voltage Levels	V_{OL} V_{OH}	$I_{OL} = 2.1mA$ $I_{OH} = -400\mu A$	 2.4	0.4	V V
Input Leakage Current	I_{LI}	$V_{IN} = 5.5V$		10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 5.5V$, CS = 0V		10	μA

INSTRUCTION SET FOR MODE SELECTION

Instruction	SB	OP Code	Address	Data	Comment
READ	1	10XX	A3A2A1A0	D_{OUT}	Read register A3A2A1A0
WRITE	1	01XX	A3A2A1A0	D15-D0	Write register A3A2A1A0
ERASE	1	11XX	A3A2A1A0	—	Erase register A3A2A1A0
EWEN	1	0011	xxxx	—	Erase/Write enable
EWDS	1	0000	xxxx	—	Erase/Write disable
ERAL	1	0010	xxxx	—	Erase all registers
WRAL	1	0001	xxxx	D15-D0	Write all registers

The KM93C06 provides 7 instructions as shown. Note that all the instructions start with a logic "1" start bit, and the next 8 bits carry the 4-bit OP code and the 4-bit address for 1 of 16, 16-bit registers.

AC TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	20ns
Input and Output Timing measurement Levels	0.8V and 2.0V
Output Load	1 TTL Gate and C_L=100pF

AC OPERATING CHARACTERISTICS

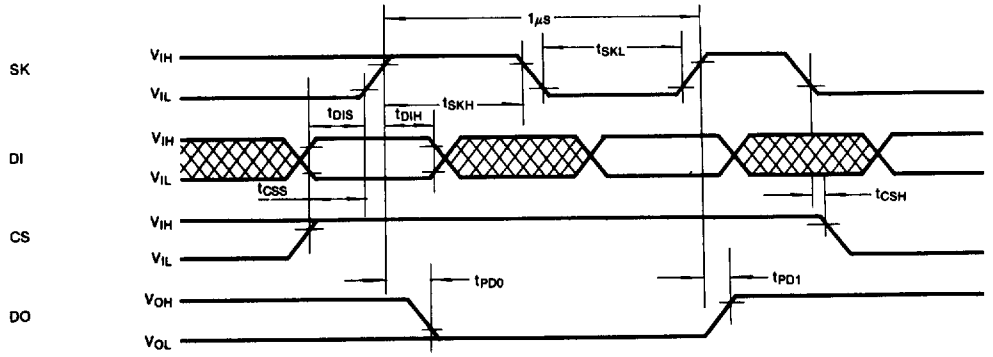
KM93C06: T_A=0°C to 70°C, V_{CC}=5V±10%, unless otherwise noted.
KM93C06I: T_A= −40°C to 85°C, V_{CC}=5V±10%, unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Max	Unit
SK Frequency	f_{SK}		—	1.0	MHz
SK High Time	t_{SKH}	(Note 1)	500		ns
SK Low Time	t_{SKL}	(Note 1)	250		ns
Chip Select Setup Time	t_{CSS}		50		ns
Chip Select Hold Time	t_{CSH}		0		ns
Data Setup Time	t_{DIS}		150		ns
Data Hold Time	t_{DIH}		150		ns
Output High Delay Time	t_{PD1}	V_{OL}=0.8V, V_{OH}=2.0V V_{IL}=0.45V, V_{IH}=2.4V		500	ns
Output Low Delay Time	t_{PD0}			500	ns
Program Cycle Time	$t_{E/W}$		10	30	ms
Falling Edge of CS to D_{OUT} High-Z	t_{OH}, t_{IH}			100	ns

Note 1: The SK frequency spec, specifies a minimum SK clock period of 1μs, therefore in a SK clock cycle $t_{SKH}+t_{SKL}$ must be greater than or equal to 1μs.
e.g., if t_{SKL}=250ns then the minimum t_{SKH}=750ns in order to meet the SK frequency specification.

TIMING DIAGRAMS

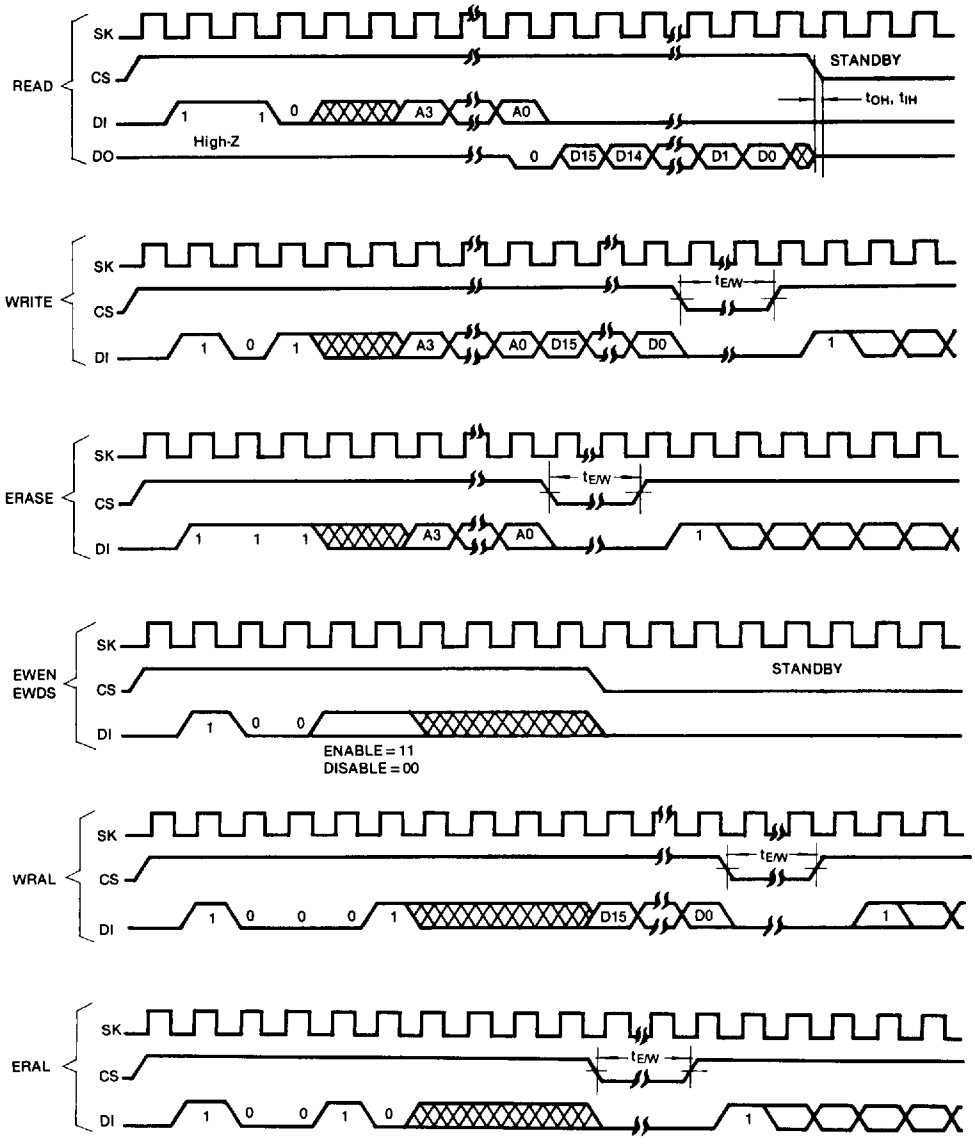
SYNCHRONOUS DATA TIMING



DON'T CARE

TIMING DIAGRAMS (Continued)

INSTRUCTION TIMING



DEVICE OPERATION

The KM93C06 is a 256 bit CMOS serial I/O EEPROM used with microcontrollers for nonvolatile memory applications. The on-chip programming voltage generator allows user to use a single 5V power supply. All the operations of the chip are preceded by an instruction set, consisting of a start bit and two OP code bits, facilitating inherent protection against false writes. The DO pin is in high-Z except for the read period to eliminate bus contention.

READ

After a read instruction and address set is received, low to high transition of the SK clock produces output data at DO pin. A dummy bit (logical "0") preceds the 16 bit data output string.

EWEN / EWDS

The KM93C06 is at the erase/write disable (EWDS) state during the power-up period to protect against accidental disturbance. After the power up period, the erase/write operation must be preceded by an erase/write enable (EWEN) operation. The erase/write enable (EWEN) mode is maintained until an erase/write disable (EWDS) operation is executed or V_{CC} is removed from the part. Execution of the READ operation is independent of both EWEN and EWDS instructions.

ERASE

Before a write cycle, an erase cycle need to be operated to reset the EEPROM cells to the "erase" state. A chip starts an erase cycle by dropping CS low after an erase instruction and address set is input. The erase cycle is ended by raising CS input high after the program cycle time (t_{EW}) is satisfied.

WRITE

The write operation is started by sequentially loading its instruction, address, and data set. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the write cycle. Like the erase operation, the write cycle is completed by the rising edge of the CS input.

ERAL (chip erase)

Entire memory array is erased, i.e., logical "1" state, by this chip erase (ERAL) operation. The chip erase cycle is identical to the erase cycle except for different OP code.

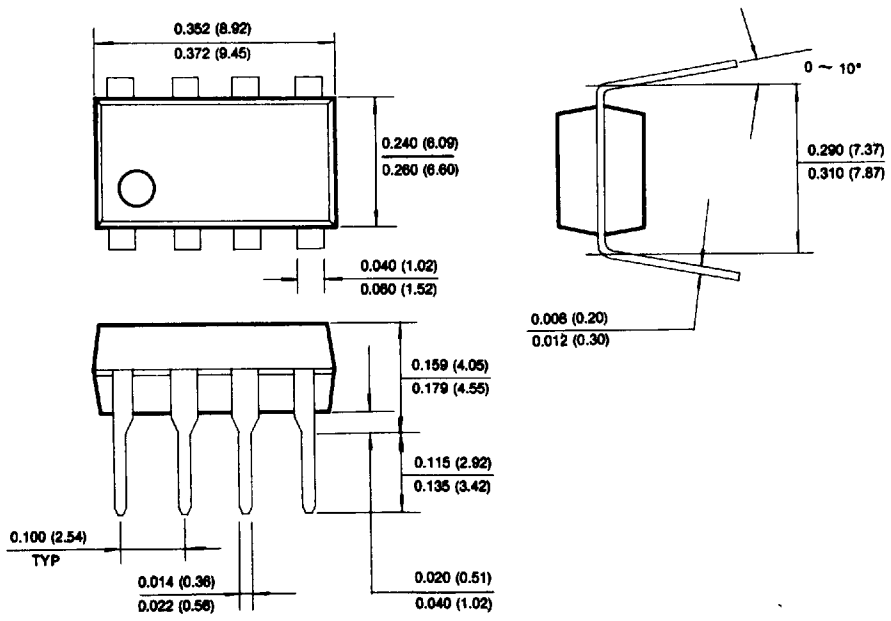
WRAL (chip write)

The entire array need to be erased before this chip write mode operation. Data given during this mode are written to all cells in the corresponding column simultaneously.

PACKAGE DIMENSIONS

8 PIN PLASTIC DUAL IN LINE PACKAGE

unit: inches (millimeters)



8 PIN PLASTIC SMALL OUT LINE PACKAGE