SED1345F$_{OA}$

CMOS VIDEO-LCD INTERFACE (VLI)

S-MOS Systems, Inc.

October, 1996

Version 1.0 (Preliminary)

THIS PAGE INTENTIONALLY BLANK

Table of Contents

Table of Contents

1.0 GENERAL DESCRIPTION

1.1 DESCRIPTION

The SED1345 is a video-LCD interface (VLI) developed for a dot matrix LCD display system. It converts separate video signals for CRT display into signals for LCD.

The SED1345 can use a conventional LCD driver to display data at eight gradation levels corresponding to digital video signal data I, R, G and B. The on-chip color pallet for gradation display allows setting of any gradation level for each of the 16 colors on the CRT display.

A 640 × 480 dot panel with eight gradation levels can be driven using only 256K bits of frame buffer memory. This leads to a significant reduction in system memory cost.

With the SED1345, the user can select not only a display size but a display area to configure a display panel of flexible size from 640 × 200 dots to 640 × 480 dots (maximum). These LCD display sizes are compatible with various display modes such as CGA® and EGA®.

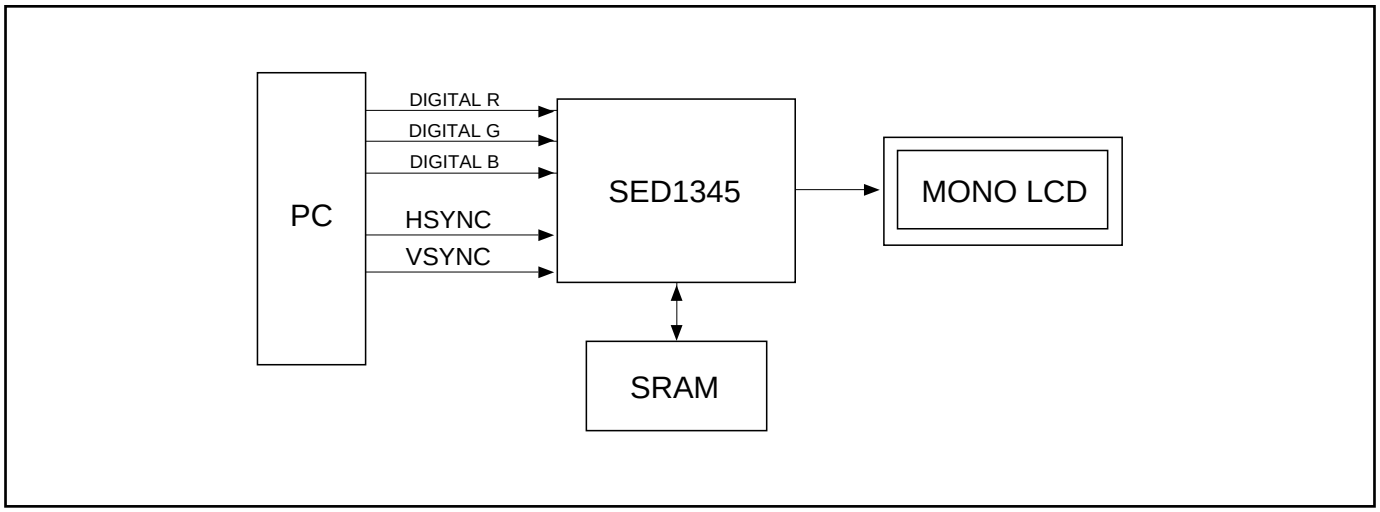
1.2 FEATURES

- Low-power CMOS technology
- TTL-compatible signal input
- LCD display size:
  - Horizontal . . . . . 640 dots
  - Vertical . . . . . 200, 350, 400, 480 lines
- Supports 8 levels of gray shade
- Supports single panel and dual panel
- LCD driver interface . . . . 4 bits bus and 4 bits × 2 bus
- Register programming by 4 bits
- Maximum dot clock . . . . 30 MHz
- Supports 40KB SRAM frame buffer
- Duty cycle . . . . . 1/200 to 1/480
- Power-on clear function
- Single power supply . . . . 5V ± 5%
- Package . . . . . QFP5-80 pin (FOA)

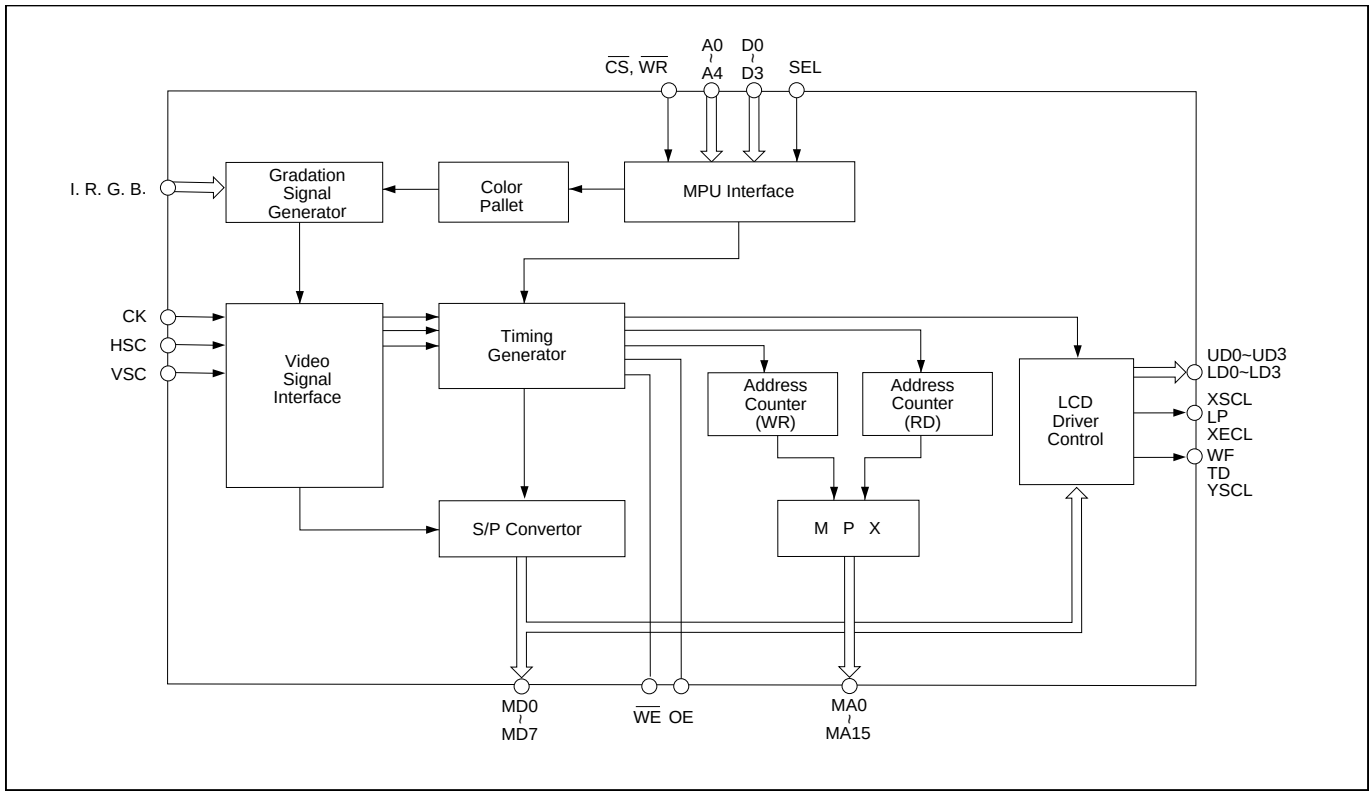
THIS PAGE INTENTIONALLY BLANK

2.0 BLOCK DIAGRAMS

2.1 SYSTEM BLOCK DIAGRAM



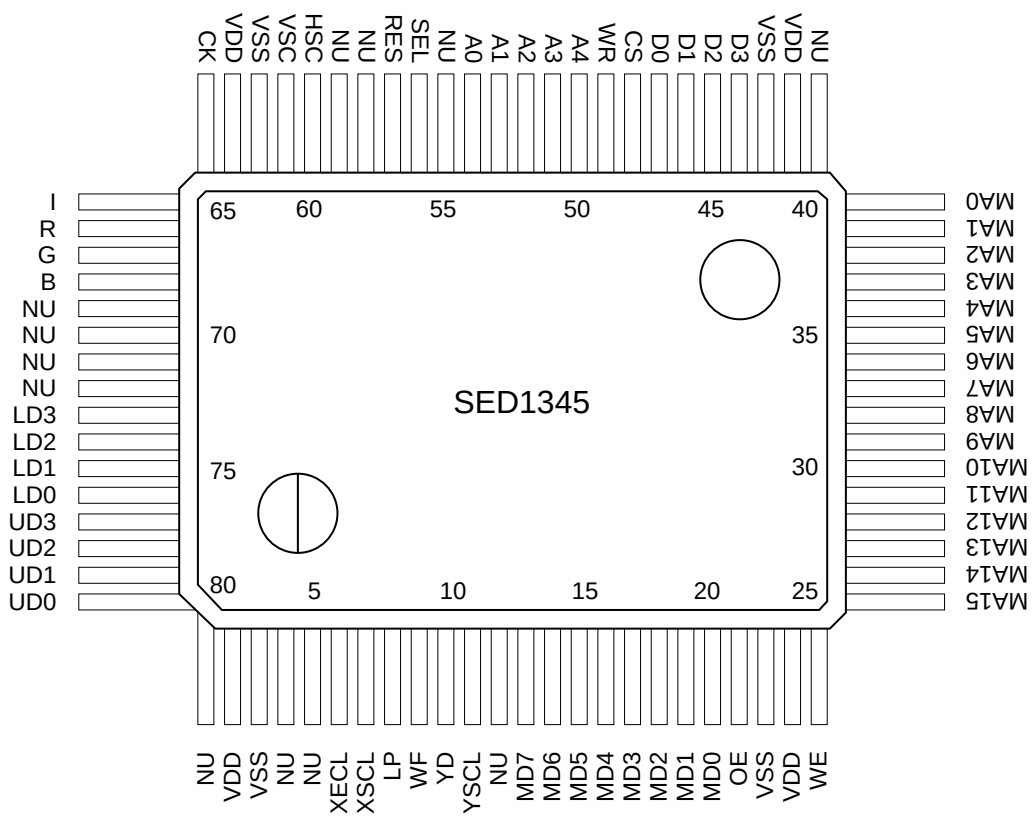
2.2 BLOCK DIAGRAM



THIS PAGE INTENTIONALLY BLANK

3.0 PIN CONFIGURATION

3.1 PIN CONFIGURATION



No.	Name	No.	Name	No.	Name	No.	Name
1	NU	21	$\overline{OE}$	41	NU	61	VSC
2	VDD	22	VSS	42	VDD	62	VSS
3	VSS	23	VDD	43	VSS	63	VDD
4	NU	24	$\overline{WE}$	44	D3	64	CK
5	NU	25	MA15	45	D2	65	I
6	XECL	26	MA14	46	D1	66	R
7	XSCL	27	MA13	47	D0	67	G
8	LP	28	MA12	48	$\overline{CS}$	68	B
9	WF	29	MA11	49	$\overline{WR}$	69	NU
10	YD	30	MA10	50	A4	70	NU
11	YSCL	31	MA9	51	A3	71	NU
12	NU	32	MA8	52	A2	72	NU
13	MD7	33	MA7	53	A1	73	LD3
14	MD6	34	MA6	54	A0	74	LD2
15	MD5	35	MA5	55	NU	75	LD1
16	MD4	36	MA4	56	SEL	76	LD0
17	MD3	37	MA3	57	$\overline{RES}$	77	UD3
18	MD2	38	MA2	58	NU	78	UD2
19	MD1	39	MA1	59	NU	79	UD1
20	MD0	40	MA0	60	HSC	80	UD0

Note: NU = Pin is Not Used

The NU pin is wired to the IC chip inside the package, and must be held open.

3.2 PIN DESCRIPTION

Pin Name	Pin No.	Function
V_{DD}	2, 23, 42, 63	+5V power
V_{SS}	3, 22, 43, 62	GND
UD0 to UD3	80 to 77	Data bus output to X–driver
LD0 to LD3	76 to 73	Data bus output to X–driver
XSCL	7	Shift clock output to X–driver
LP	8	Latch pulse output
XECL	6	Enable shift clock output to X–driver
WF	9	LCD AC signal output
YD	10	Scanning start data output to Y–driver
YSCL	11	Shift clock output to Y–driver
I, R, G, B	65 to 68	Video data input
CK	64	Dot clock input
HSC	60	Horizontal sync signal input
VSC	61	Vertical sync signal input
MA0 to MA15	40 to 25	Address bus output to frame buffer memory
MD0 to MD7	20 to 13	Data bus input/output to frame buffer memory
$\overline{WE}$	24	Write enable signal output
$\overline{OE}$	21	Output enable signal output
D0 to D3	47 to 44	Data bus input for writing registers
A0 to A4	54 to 50	Address bus input/output for writing registers
$\overline{CS}$	48	Chip select signal input
$\overline{WR}$	49	Write signal input
SEL	56	Register write mode selection input (ROM/MPU)
$\overline{RES}$	57	Reset signal input

THIS PAGE INTENTIONALLY BLANK

4.0 FUNCTIONAL DESCRIPTION

4.1 MPU INTERFACE

An operation mode (such as the panel size, display position or LCD interface) of the SED1345F is selected by writing data into internal registers. The SEL pin is used for ROM/MPU selection as specified in Table 4.1. If the ROM write mode is selected, A0 to A4 work as address output pins. (See section 5.4.4.2)

Table 4.1 Register Write Mode Selection

SEL = "H"	SEL = "L"
Write data using ROM ($\overline{CS}$ = "L", $\overline{WR}$ = "H" or "L" <fixed>)	Write data using MPU (Write at rising edge of $\overline{WR}$)

4.1.1 Internal Registers (Mode Selection)

Table 4.2 lists the internal registers used to select a mode.

Table 4.2 Internal Registers

Register address					Register		Data			
A4	A3	A2	A1	A0	No.	Name	D3	D2	D1	D0
0	0	0	0	0	R0	Horizontal back porch register (low byte)	K3	K2	K1	K0
	0	0	0	1	R1	Horizontal back porch register (high byte)	K7	K6	K5	K4
	0	0	1	0	R2	Vertical back porch register (low byte)	L3	L2	L1	L0
	0	0	1	1	R3	Vertical back porch register (high byte)	—	L6	L5	L4
	0	1	0	0	R4	—				
	0	1	0	1	R5	—				
0	0	1	1	0	R6	—				
	0	1	1	1	R7	—				
	1	0	0	0	R8	LCD operation mode select register	S3	S2	S1	S0
	1	0	0	1	R9	LCD interface register	S7	S6	S5	S4
	1	0	1	0	R10	Video signal polarity select register	P3	P2	P1	P0
	1	0	1	1	R11	Display area select register	—	M2	M1	M0
	1	1	0	0	R12	—				
	1	1	0	1	R13	—				
	1	1	1	0	R14	—				
	1	1	1	1	R15	—				

4.1.2 Internal Register (Gradation Display Color Pallet)

Table 4.3 Gray Mode Display Color Pallet

Register address						Gradation data (preset)				
A4	A3	A2	A1	A0	Corrresponding CRT color	Color pallet				Gradation level No.
	I	R	G	B		D3	D2	D1	D0	
1	0	0	0	0	Black	—	0	0	0	0
	0	0	0	1	Blue	—	0	0	1	1
	0	0	1	0	Green	—	1	0	0	4
	0	0	1	1	Cyan	—	1	0	1	5
	0	1	0	0	Red	—	0	1	0	2
	0	1	0	1	Magenta	—	0	1	1	3
	0	1	1	0	Brown	—	1	1	0	6
	0	1	1	1	Light Gray	—	1	1	1	7
	1	0	0	0	Dark Gray	—	0	0	0	0
	1	0	0	1	Light Blue	—	0	0	1	1
	1	0	1	0	Light Green	—	1	0	0	4
	1	0	1	1	Light Cyan	—	1	0	1	5
	1	1	0	0	Light Red	—	0	1	0	2
	1	1	0	1	Light Magenta	—	0	1	1	3
	1	1	1	0	Yellow	—	1	1	0	6
	1	1	1	1	White	—	1	1	1	7

A gradation level number can be assigned to any of the 16 colors represented by I, R, G and B by changing the color pallet data (D0 to D2). At power-on, the preset values listed in Table 4.3 are valid. Table 4.4 shows assignment of data to gradation level numbers.

Table 4.4 Data Assignment to Gradation Level Numbers

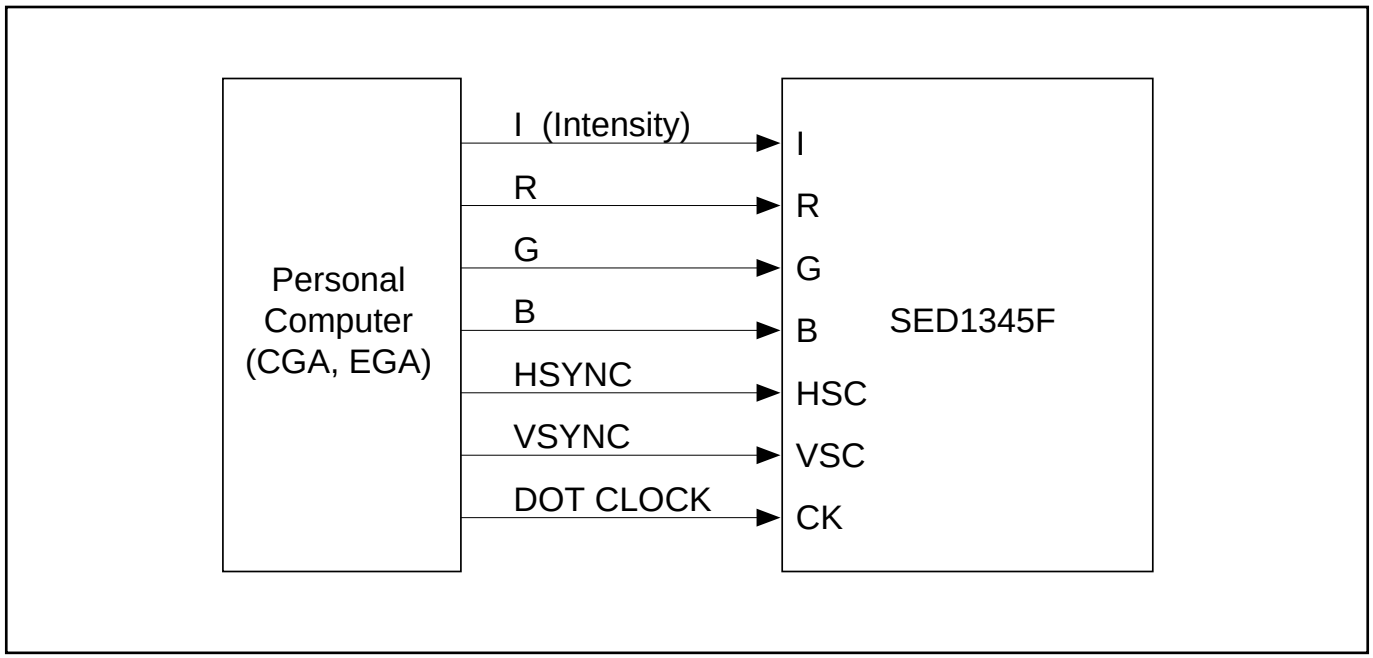
D2	D1	D0	Gradation No.	
0	0	0	0	Off
0	0	1	1	Halftone
0	1	0	2	Halftone
0	1	1	3	Halftone
1	0	0	4	Halftone
1	0	1	5	Halftone
1	1	0	6	Halftone
1	1	1	7	On

4.2 VIDEO SIGNAL INTERFACE

4.2.1 Video Signal Input

Separate video signals (TTL level digital) are input into the SED1345F.

4.2.1.1 Video Signal Input



4.2.2 Gray Mode Display

The SED1345F can use an existing LCD panel to provide an eight gradation level display. As display data is turned on/off on a frame basis, the following requirements are to be satisfied:

(a) The video signal input must be synchronized to the LCD data output. (The duration of one frame for a video signal must equal that for LCD data).

(b) A frame frequency of 70 to 80 Hz is recommended (to prevent flickering).

(c) Line inversion drive signals within the LCD module are recommended for use as AC conversion of liquid crystals (to prevent flickering).

Implementing the above (a) and (b) requires a change in the blanking period of a video signal. (This means that simultaneous display of data on the CRT and LCD is not allowed).

Fig. 4.2.2.1 shows one frame of a video signal. If one frame on the CRT corresponds to that on the LCD (e.g., 640 x 480 dots), the frame frequency fFR can be given by the following equation:

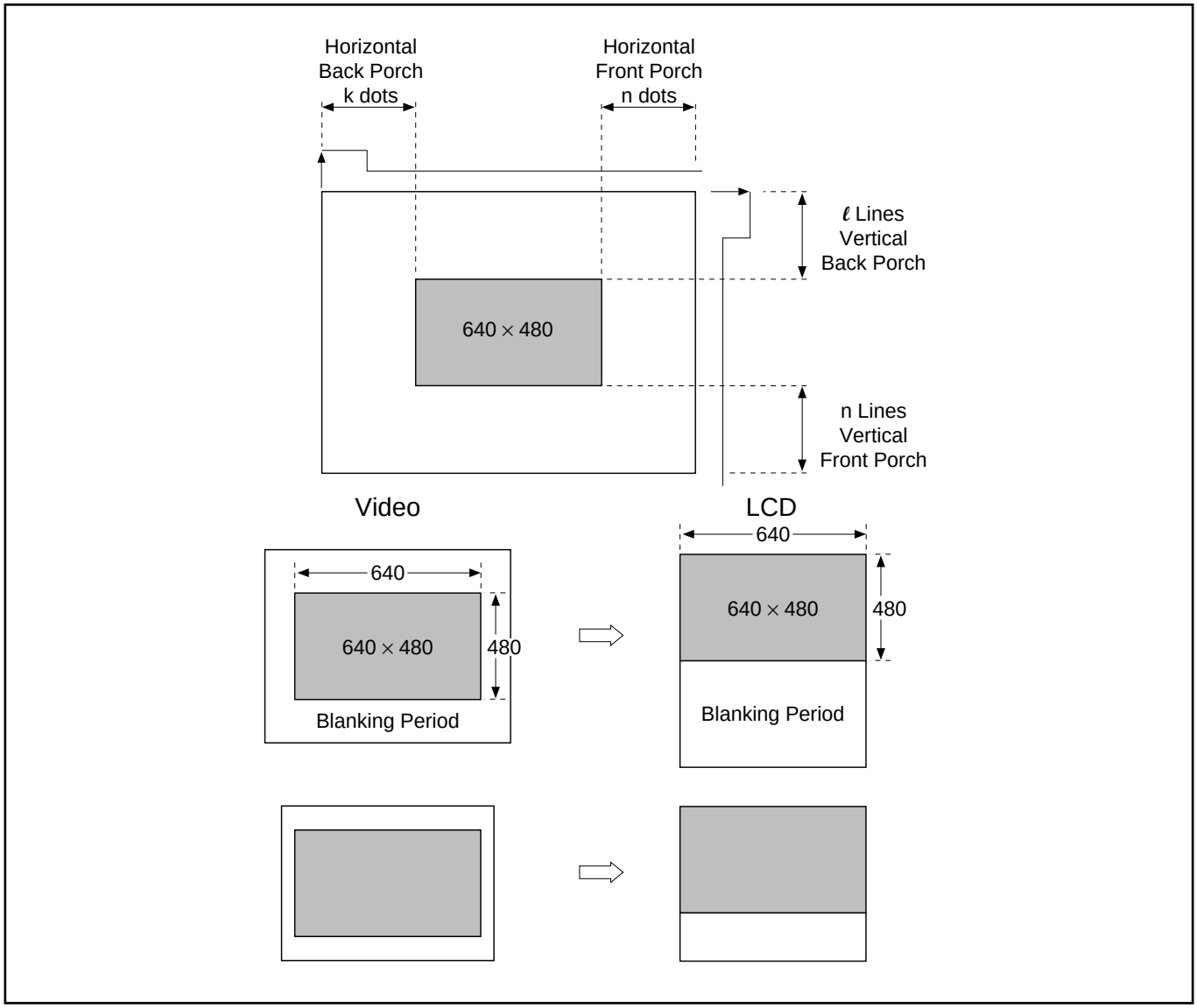
$$fFR = \frac{fCK}{(640 + k + m) \times (480 + \ell + n)}$$

where fCK is the dot clock frequency. The LCD driving duty ratio is given by:

$$\frac{1}{\frac{(640 + k + m) \times (480 + \ell + n)}{640} \times \frac{1}{2}} \quad \text{duty}$$

(for double panel drive mode)

4.2.2.1 One Frame of Video Signal



It is possible that, if the blanking period of Video signal is large, the blanking period of an LCD is large, and LCD driving duty ratio is small.

The duty ratio should be as large as possible in order to increase the LCD display quality. In addition, fFR should be as high as possible (70 to 80 Hz) for the prevention of flickering. For example,

if $\ell + n = 4$, $k + m = 4$ and
fCK = 24MHz,
then fFR = 77MHz and
LCD driving duty ratio = 1/244.

The SED1345F contains a color pallet for gray mode display as shown in Table 4.3. Which of the eight gradation levels should be assigned to each of the 16 colors represented by video signals I, R, G and B can be determined by changing the data set in the pallet. With the power-on clear function, the data shown in Table 4.3 is preset at power-on.

4.2.3 Dot Clock

The dot clock CK is supplied to the SED1345F from the system. Combined with the LCD display size and the blanking period, the dot clock frequency fCK gives the frame frequency fFR. If the blanking period is 0, a maximum frame frequency can be obtained and given by

$$fFR\ MAX = \frac{fCK}{640 \times 480}$$

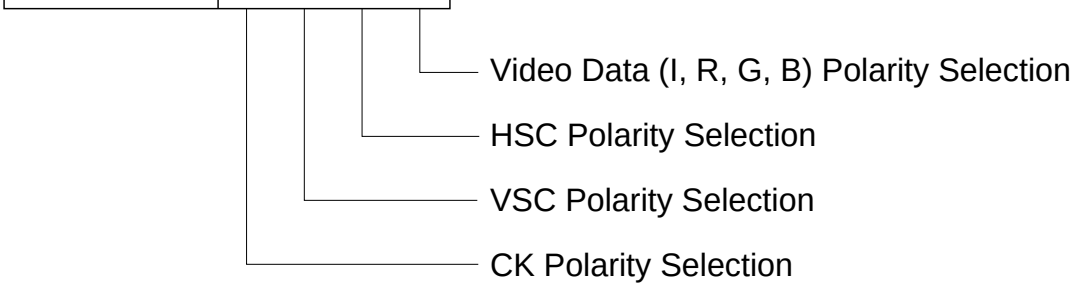
Thus the fFR max. depends on the display size and fCK. Inversely, fCK must be greater than 21.5 MHz if fFR > 70 Hz is required for the 640 x 480 dot panel. For details, see section 4.3.3.

4.2.4 Polarity Selection

The polarity of a video signal can be changed by writing data into the video signal polarity select register (R10). Table 4.5 shows the function of this register.

Table 4.5 Video Signal Polarity Select Register (R10)

Address	Data
0 1 0 1 0	P3 P2 P1 P0



Data	Function	
	Data = 0	Data = 1
P0	Inversion	Forwarding (“H” level video data to be transferred as “H” level LCD data)
P1	Negative logic	Positive logic
P2	Negative logic	Positive logic
P3	Data taken in at positive edge	Data taken in at negative edge

4.2.5 Display Position on LCD Panel

The video data has a horizontal back/front porch period and a vertical back/front porch period (see Fig. 4.2.2.1). These periods take certain values which depend on fFR and the display size. During each period, invalid (blank) data is being output. Values k and ℓ (specified in Fig. 4.2.2.1) must be set in the SED1345F (more specifically, in the horizontal back porch registers R0, R1 and the vertical back porch registers R2, R3; see Table 4.2) in order to transfer valid data to the LCD panel.

The relation between write data and back porch values is shown in Tables 4.6 and 4.7.

Table 4.6 Relation between Horizontal Back Porch (k) and Write Data Unit: dots

Write data									Horizontal back porch k
K7	K6	K5	K4	K3	K2	K1	K0		
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	1	2
0	0	0	0	0	0	1	0	2	3
				—				—	—
				—				—	—
1	1	1	1	1	1	1	1	255	256

(K7, K6, ..., K0) = (Horizontal back porch k) – 1 *

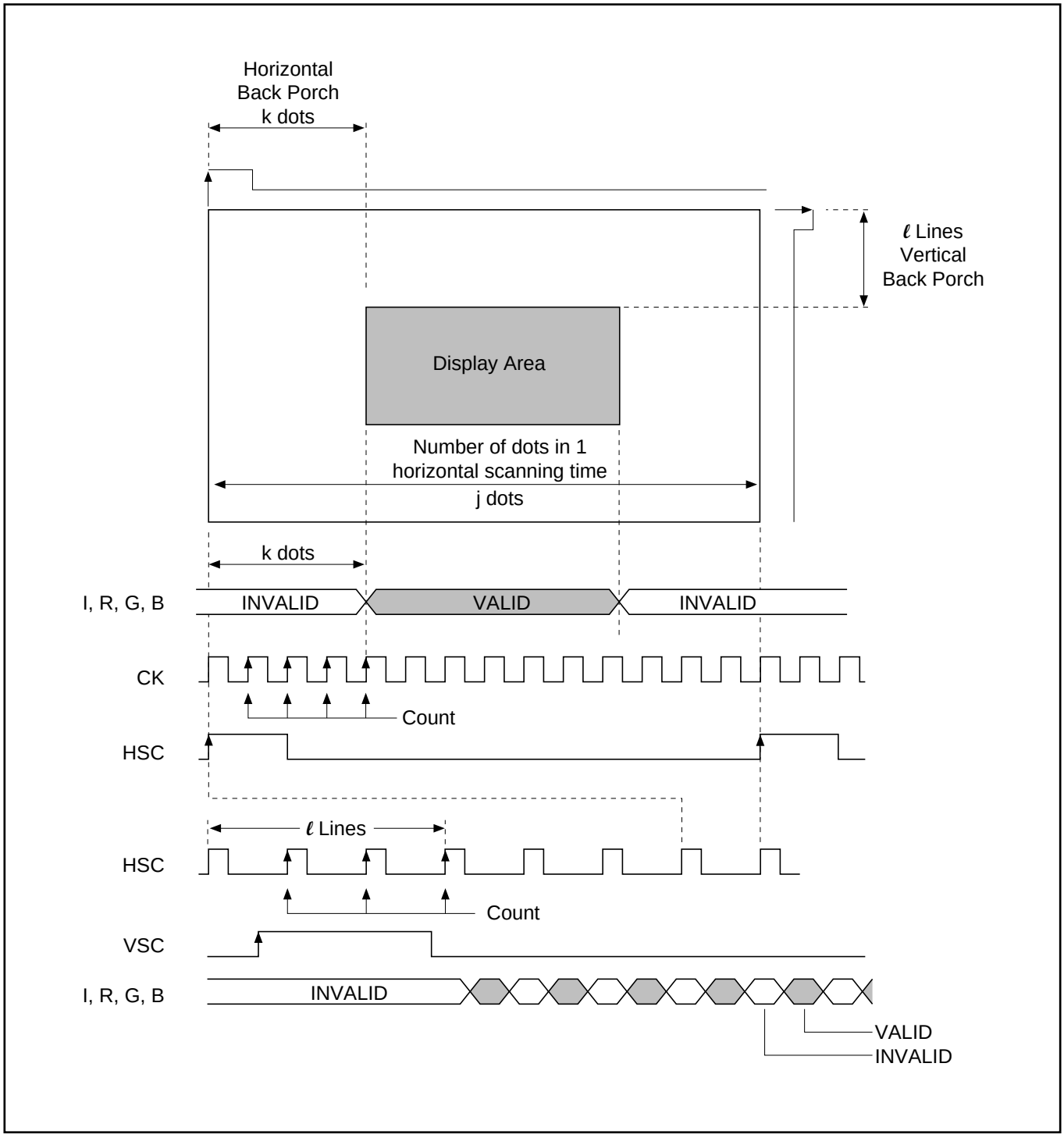
Table 4.7 Relation between Vertical Back Porch (ℓ) and Write Data Unit: dots

Write data								Vertical back porch ℓ
L6	L5	L4	L3	L2	L1	L0		
0	0	0	0	0	0	0	0	2
0	0	0	0	0	0	1	1	3
0	0	0	0	0	1	0	2	4
			—				—	—
			—				—	—
1	1	1	1	1	1	1	127	129

(L6, L5, ..., L0) = (Vertical back porch ℓ) – 2 *

* The VLI is triggered by the leading edge of the HSC or VSC signals. Therefore, horizontal back porch k or vertical back porch ℓ is equal to the back porch period defined by the CRT controller, plus the pulse width of H-SYNC or V-SYNC. (See the timing chart below.)

4.2.5.1 Horizontal Back Porch k, Vertical Back Porch ℓ, and Number of Dots j in One Horizontal Scanning Period



Example: Horizontal back porch k = 4 (dots)
Vertical back porch ℓ = 3 (lines)

Write (K7, K6, ..., K0) = 3 and (L6, L5, ..., L0) = 1.

The k-counter in the SED1345F is enabled when triggered by the HSC Input and the ℓ-counter by the VSC input. Thus these counters start to count the horizontal and vertical back porch periods. Upon completion of the counting, shifting-in of valid display data begins.

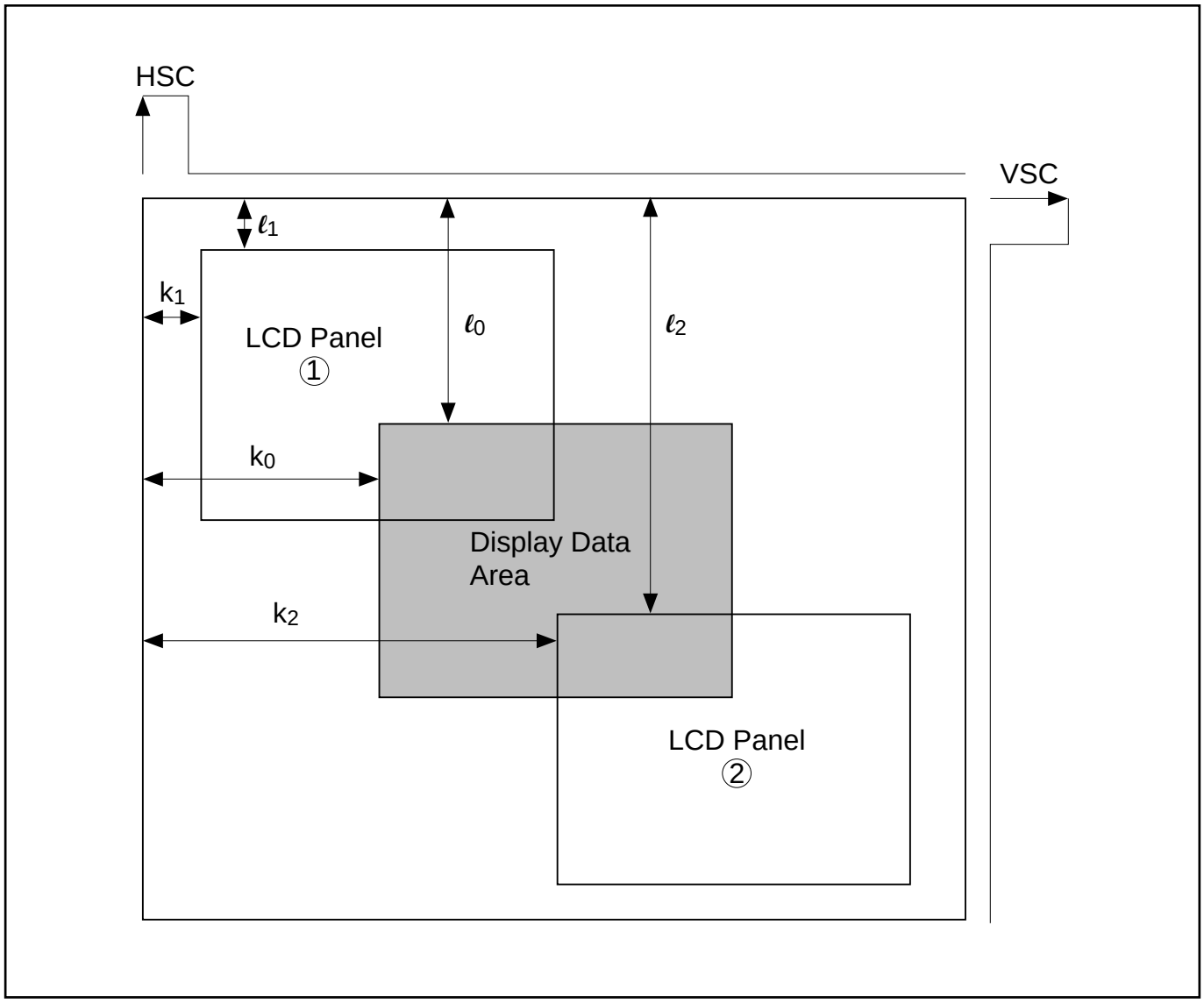
4.2.5.2 Scrolling Display Position

The display on the LCD panel moves horizontally or vertically when the value in the horizontal back porch register or the vertical back porch register is changed. Table 4.8 shows the increase/decrease of register values and the direction of movement of horizontal and vertical display positions.

Table 4.8 Register Values and Display Position Movement

Register values	Horizontal movement	Vertical movement
Increase	To left (k: increases)	Up (ℓ: increases)
Decrease	To right (k: decreases)	Down (ℓ: increases)

4.2.5.3 Register Values and Display Positions



k0: Horizontal back porch ℓ0: Vertical back porch

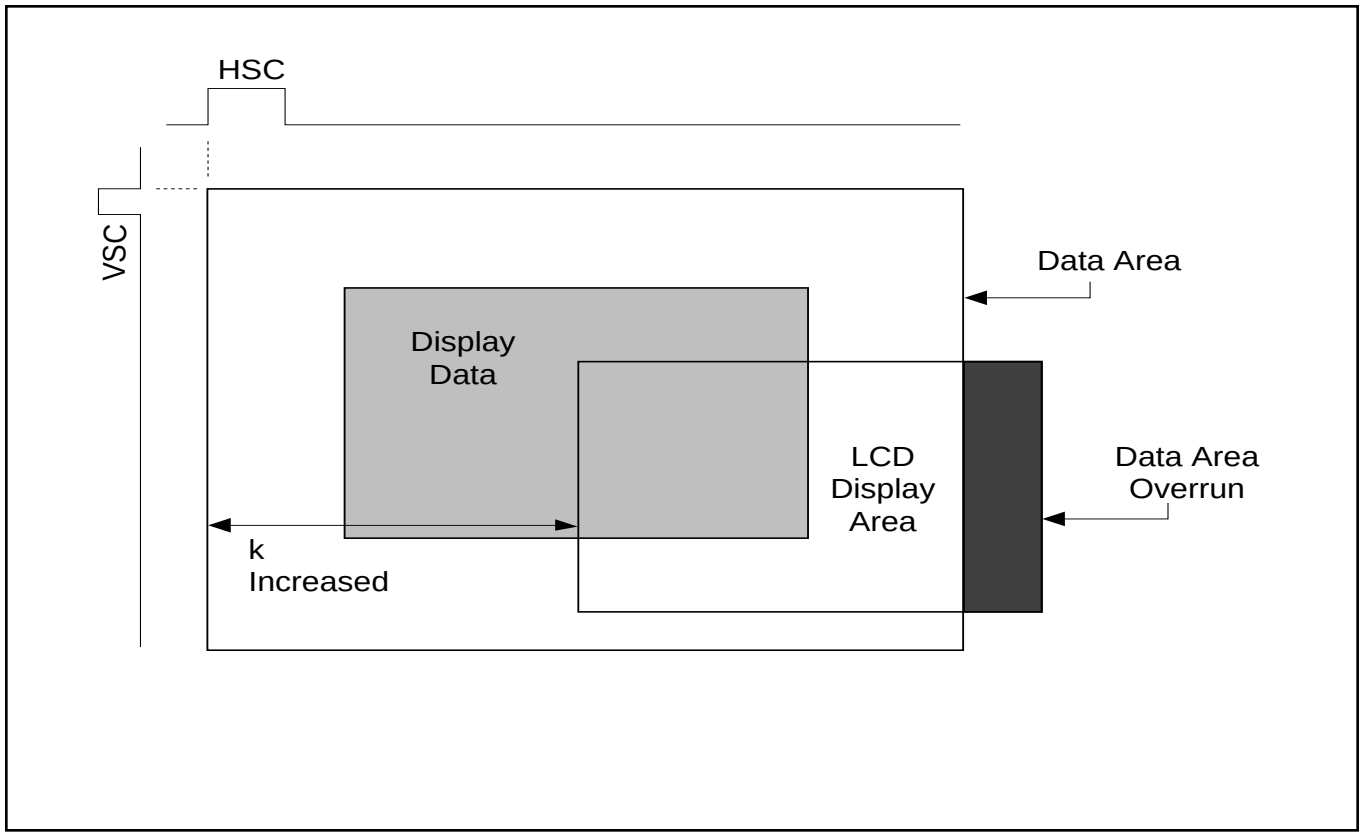
LCD panel ①: Both the horizontal and vertical back porch register values k1 and ℓ1 are small.

LCD panel ②: Both the horizontal and vertical back porch register values k2 and ℓ2 are large.

If the horizontal or vertical back porch register value changes between 00H and FFH or between 00H and 7FH, respectively, the back porch setting will change at random resulting in a random jump of the LCD display position.

It is possible that, if the value k of the horizontal back porch register is increased, the LCD display can go abnormal. This is because the area the SED1345F attempts to get for data display over-runs the video data area formed by HSC and VSC. Normal display can be restored by setting a proper k-value.

4.2.5.4 Video Data Area Overrun



4.3 LCD INTERFACE

4.3.1 Shift Clock Frequency and Frame Frequency

As stated in 4.2.2, the LCD frame frequency is equal to the frame frequency of a video signal. The shift clock of the X-driver is produced by dividing the dot clock CK. Therefore, the shift clock frequency fXSCL can be either of the following depending on the configuration of the data bus to the LCD panel:

$f_{XSCL} = 1/4 f_{CK}$ (4–bit bus)

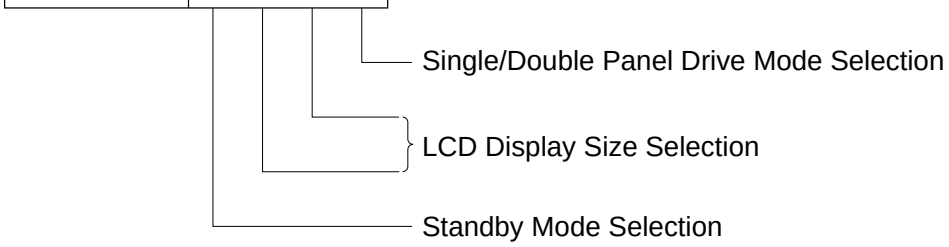
$f_{XSCL} = 1/8 f_{CK}$ (4–bit bus $\times$ 2 panels)

4.3.2 Operation Modes

Tables 4.9 and 4.10 show the functions of the operation mode select register (R8) and the LCD interface register (R9).

Table 4.9 LCD Operation Mode Select Register (R8)

Address	Data
0 1 0 0 0	S3 S2 S1 S0



Data	Function	
	Data = 0	**Data = 1**
S0	Double panel drive	Single panel drive

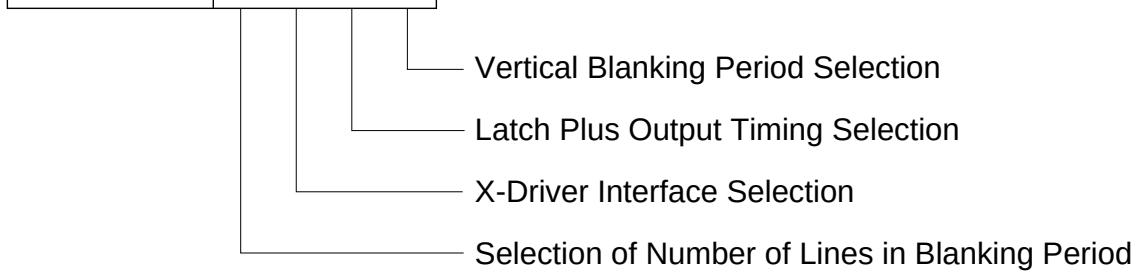
S1	**S2**	
	0	**1**
0	640 x 400	640 x 480
1	640 x 200	640 x 350

	0	**1**
S3	Normal mode (standby reset)	Standby mode

S3: The standby mode can be selected by setting S3 to “1”. In the standby mode, the dot clock CK is forced to stop and lower current dissipation will result. As setting S3 to “1” also causes the LCD output signal to stop, it is necessary to turn off the LCD power supply before starting the standby mode. The mode can be reset by setting S3 to “0” or making $\overline{RES}$ go low.

Table 4.10 LCD Interface Register (R9)

Address	Data
0 1 0 0 1	S7 S6 S5 S4



Data	Function	
	Data = 0	**Data = 1**
S4	Vertical blanking period present	Vertical blanking period absent*
S5	Level (PDP)	Edge (LCD)
S6	4-bit bus × 2	4-bit bus
S7	2 lines, 4 lines	8 lines*, 16 lines*

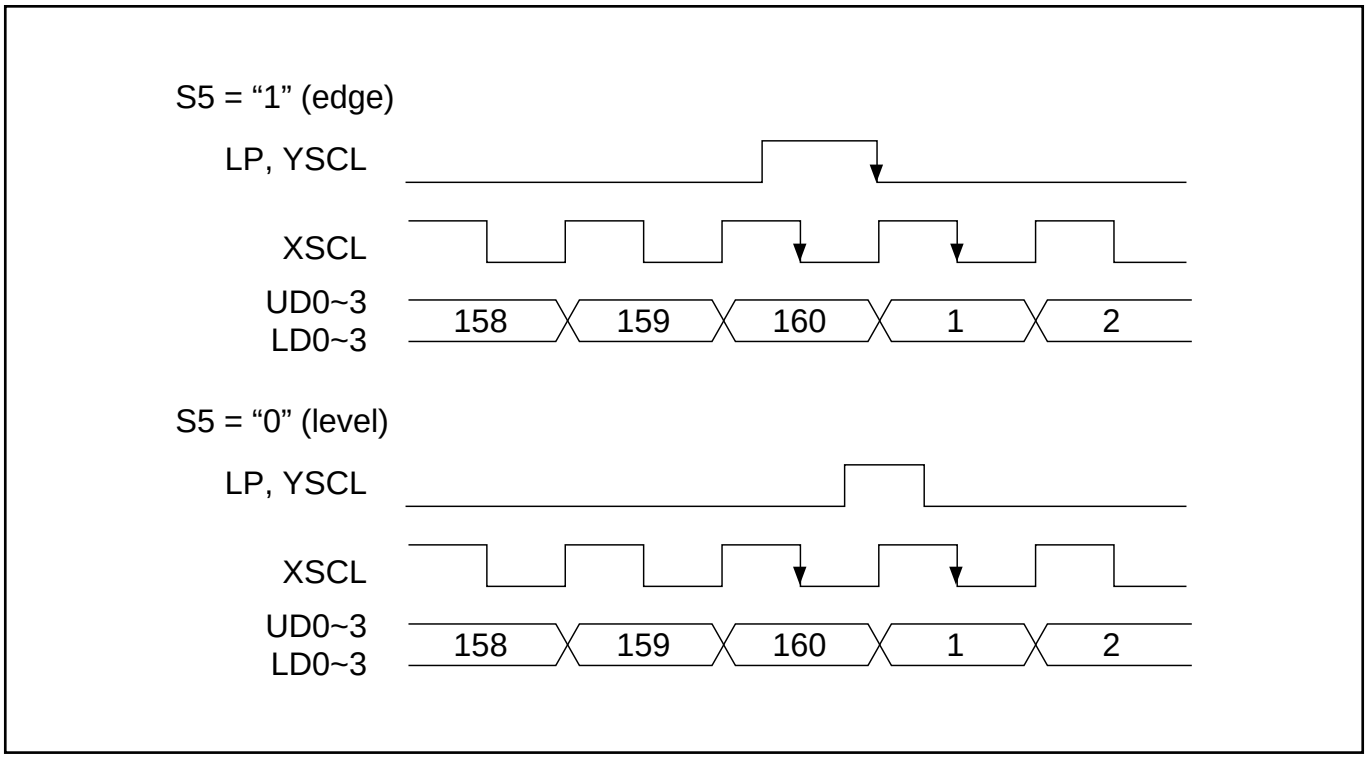
* S4 and S7 cannot have the value “1”. (They are fixed at “0”.)

S5: S5 can select the output timing for latch pulses LP and YSCL. This enables the X-driver latch input to be interfaced for edge type or level type, whichever is desired. Figure 4.3.2.1 shows the timing for S5.

Set S5 to “1” or “0” depending on the X-driver used:

- SED1180 or SED1600FS5 = “1” (edge)
- SED2032FS5 = “0” (level)

4.3.2.1 Timing Chart for S5



S6: The combination of S6 and S0 provides four different modes of interfacing between display data and the X-driver.

Table 4.11 Interface with X-driver

S6 \ S0	0	1
0	UD0 ~ 3 — 4 → LCD LD0 ~ 3 — 4 →	UD0 ~ 3 — 8 → LCD LD0 ~ 3 *
1	UD0 ~ 3 — 4 → LCD	UD0 ~ 3 — 4 → LCD

* If S0 = 1 (panel drive) and S6 = 0, 8–bit data transfer (LD0 to LD3: high-order 4 bits) will result.

4.3.3 Display Area Selection

The SED1345F can generate four different display areas from a single LCD panel. For example, a display area of 640 x 400 dots can be implemented from a 640 x 480 dot LCD panel, as shown in Fig. 4.3.3.1. A display area is selected by writing data into the display area select register (R11). Table 4.12 shows the function of R11.

4.3.3.1 Display Area

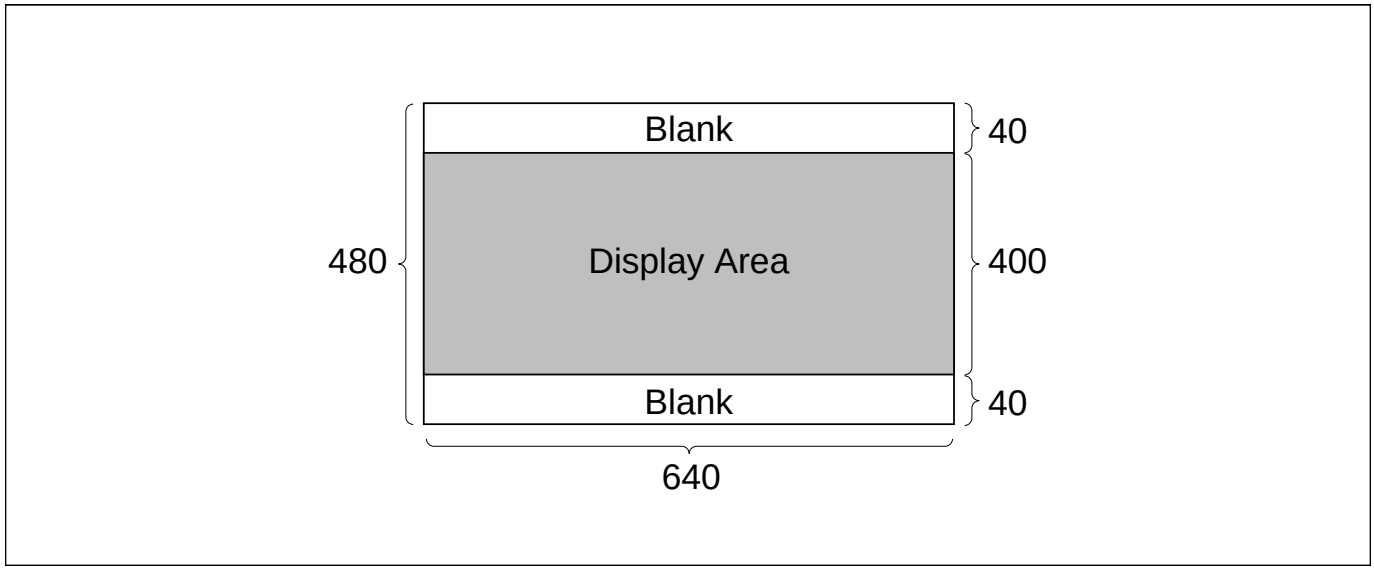
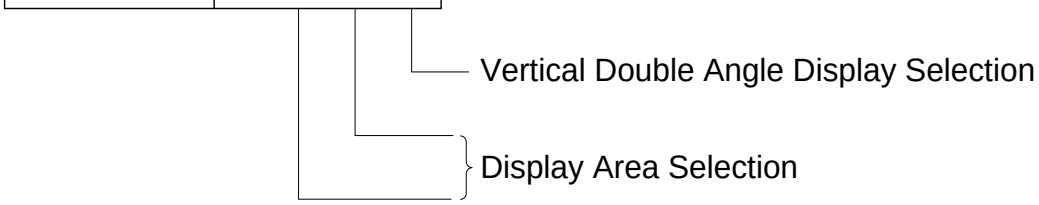


Table 4.12 Display Area Select Register (R11)

Address	Data
0 1 0 1 1	– M2 M1 M0



Data	Function	
	Data = 0	**Data = 1**
M0	Vertical double angle display present*	Vertical double angle display absent (YSCL = LP)

M1	M2	
	0	**1**
0	640 x 400	640 x 480
1	640 x 200	640 x 350

*The vertical double angle display is valid only when

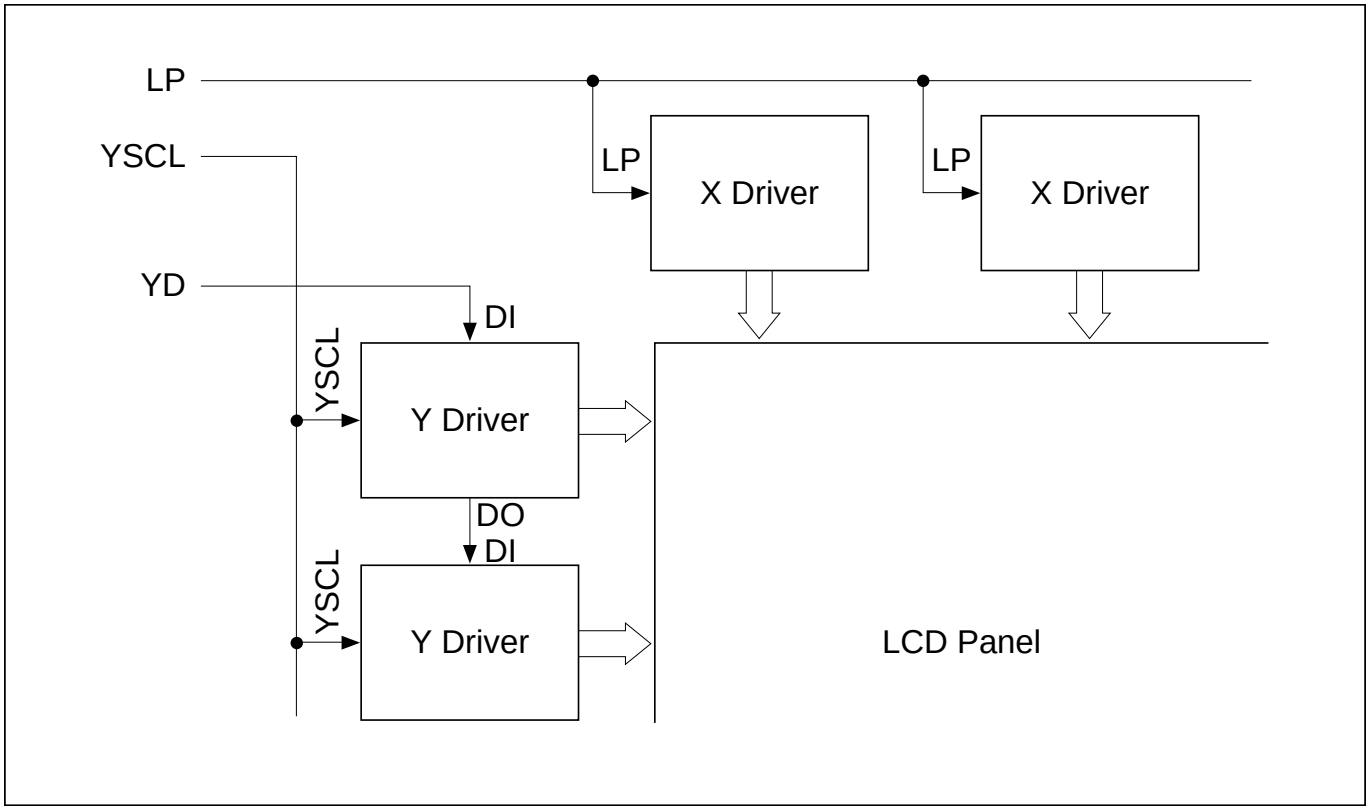
$$\begin{bmatrix}(S1,S2) = (0,0)\\(M1,M2) = (1,0)\end{bmatrix} \text{ or } \begin{bmatrix}(S1,S2) = (0,1)\\(M1,M2) = (1,0)\end{bmatrix}$$

M0: If M0 = 0 with

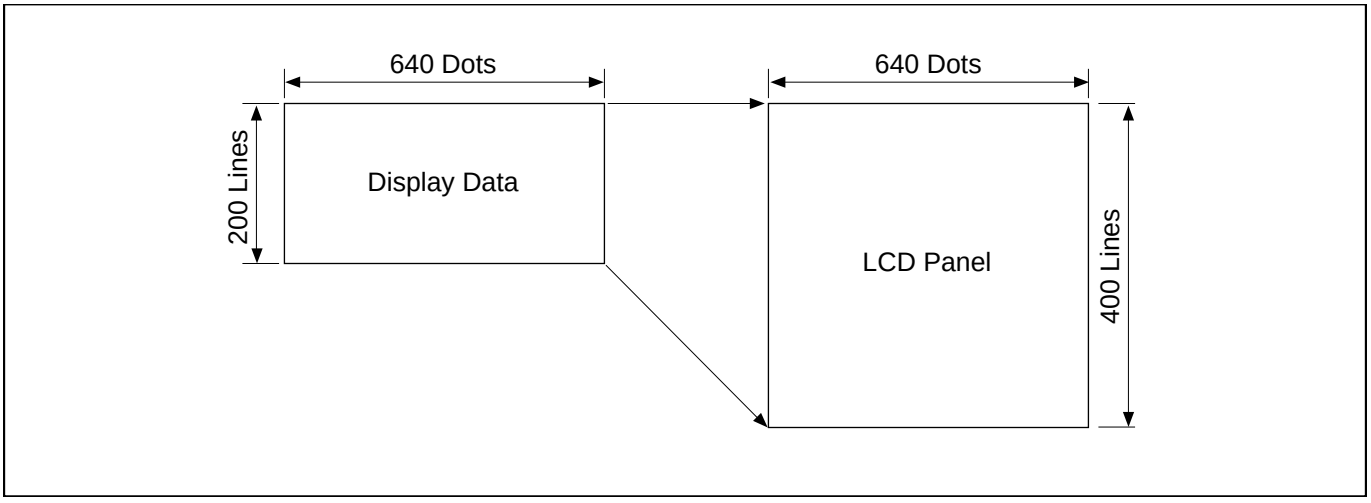
$$\begin{bmatrix}(S1,S2) = (0,0)\\(M1,M2) = (1,0)\end{bmatrix} \text{ or } \begin{bmatrix}(S1,S2) = (0,1)\\(M1,M2) = (1,0)\end{bmatrix}$$

the YSCL pin produces a 1/2 x latch pulse (LP) signal (see Fig. 4.3.3.4). (In all other cases, the YSCL pin produces the same signal as LP.) Vertical double angle display (display of the same data on a two-line basis (see Fig. 4.3.3.3) can be implemented by using YSCL as the Y-drive shift clock (see Fig. 4.3.3.2)).

4.3.3.2 Connection with Driver

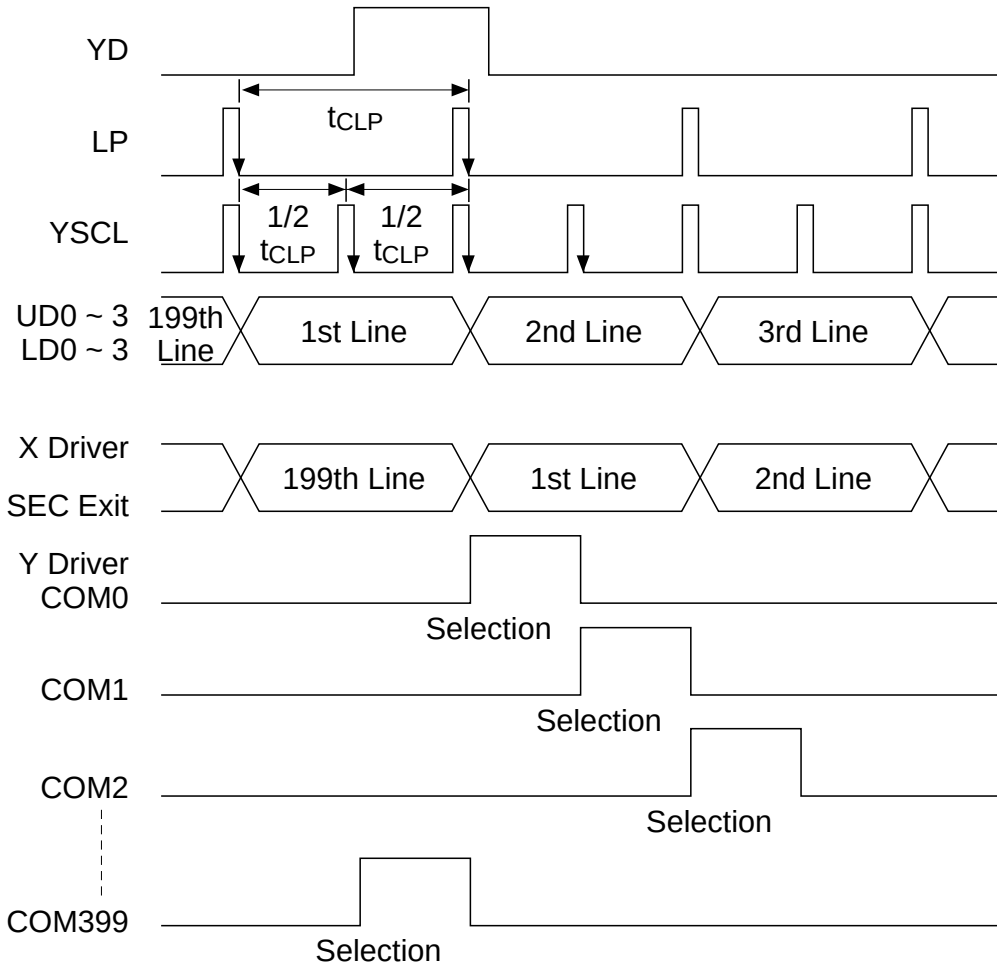


4.3.3.3 Vertical Double Angle Display



$$\begin{bmatrix} (S1,S2) = (0,0) \\ (M1,M2) = (1,0) \\ M0 = 0 \end{bmatrix}$$

4.3.3.4 Timing Chart

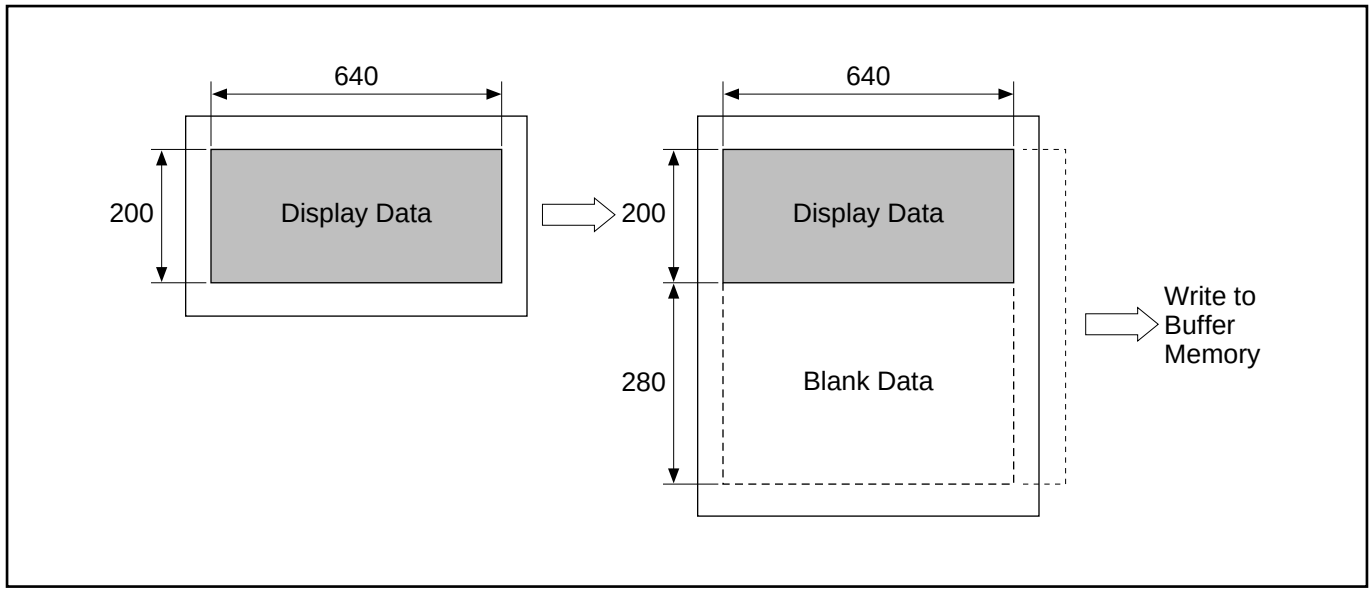


M1, M2: A display area different from the LCD panel can be used by setting M1 and M2 separately from S1 and S2. Consider the example shown in Fig. 4.3.3.1. First, using the LCD operation mode select register (R8), set (S1, S2) = (0, 1) as the LCD panel has a size of 640 x 480 dots. Next, using the display area select register (R11), set (M1, M2) = 0, 0). This provides a display area of 640 x 400 dots on the 640 x 480 dot LCD panel as shown. If the registers are set for (S1, S2) = (0, 1), (M1, M2) = (1, 0) and M0 = 0, the 640 x 200 dot area can be used as a vertical double angle display (640 x 400 dots).

Note: The blank data shown in Fig. 4.3.3.1 is read from the memory for any display. Therefore, the driving duty for the 640 x 400 dots display, for example, is the same as for the 640 x 480 dot display (e.g., 1/240 duty). This means that the dot clock frequency fCK is fixed to one value, independently of the display area, if the display size and frame frequency are definite. For example, if fCK = 24 MHz for a 640 x 480 dot display on the 640 x 480 dot LCD panel, this value of fCK should be the same (= 24 MHz) for a 640 x 350 or 640 x 200 dot display.

If a 640 x 200 dot display is to be implemented in the 640 x 480 panel, write the 640 x 480 dot video data (including blank data) into the buffer memory, as shown in Fig. 4.3.3.5. This signifies that normal display cannot be implemented without the 280 lines of blank data provided below the display area. The presence of the blank data area causes the frame frequency to be delayed accordingly if a dot clock (for example, 14 MHz) for a 640 x 200 dot display is used. Therefore, a dot clock (for example, 24 MHz) for the 640 x 480 dot display must be used as stated previously.

4.3.3.5 Writing the 640 x 480 Dot Video Data into the Buffer Memory

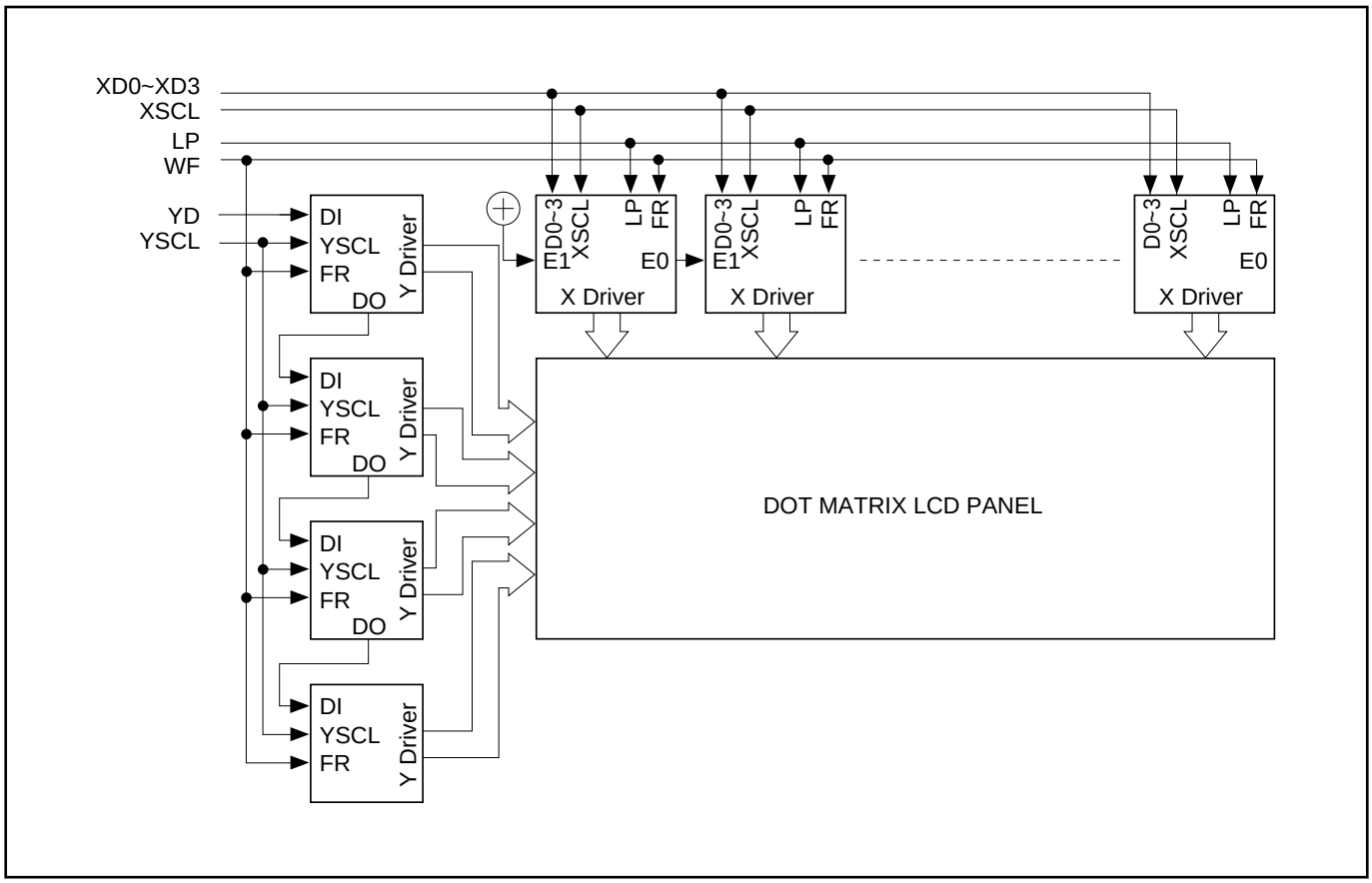


4.3.4 X-driver and Y-driver, and LCD Panel Connection

4.3.4.1 Examples of Connection

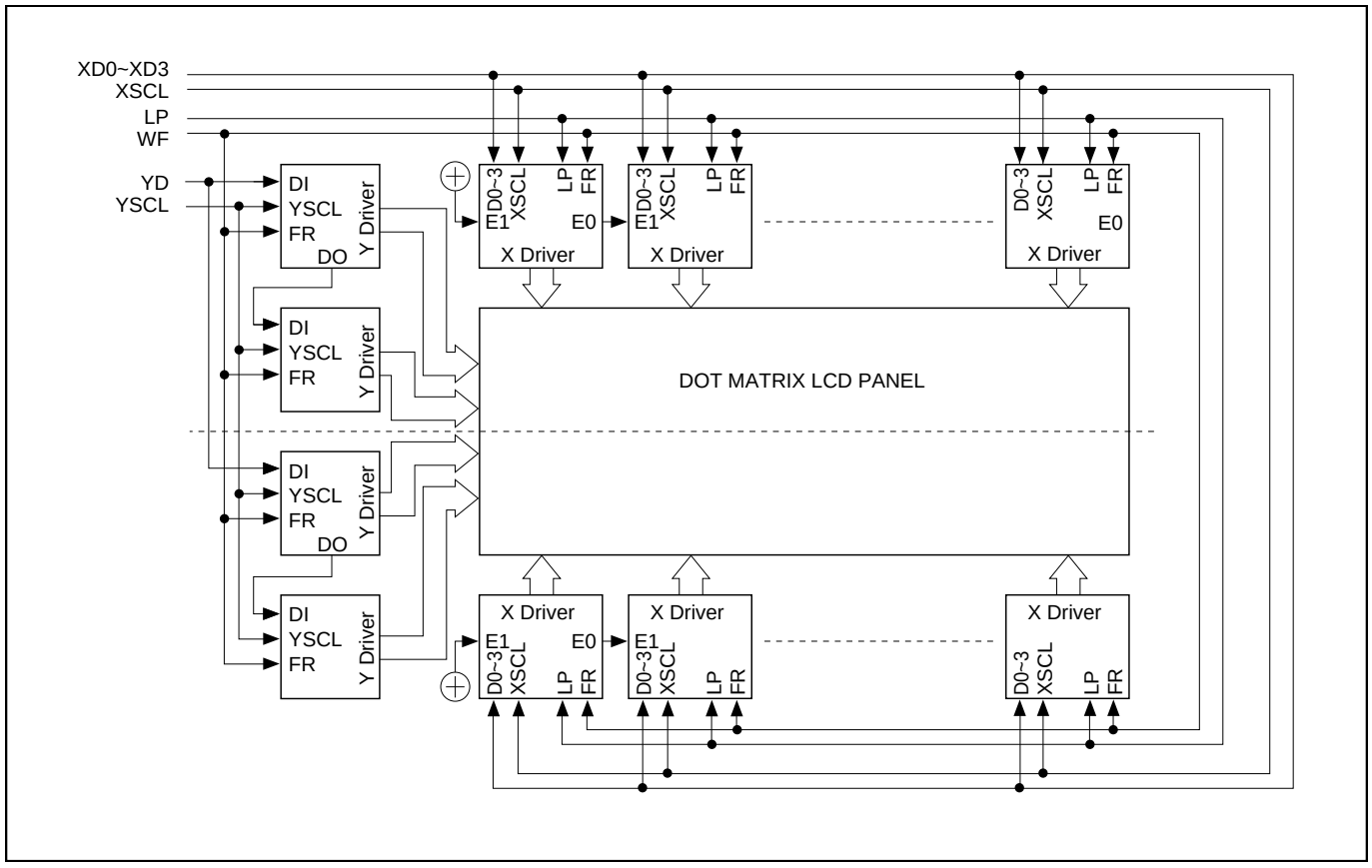
4.3.4.1.1 Connection to SED1600F/1630F <Single panel drive mode>

This is also applicable to the connection to the SED1180F/1190F or SED1600F/1610F.



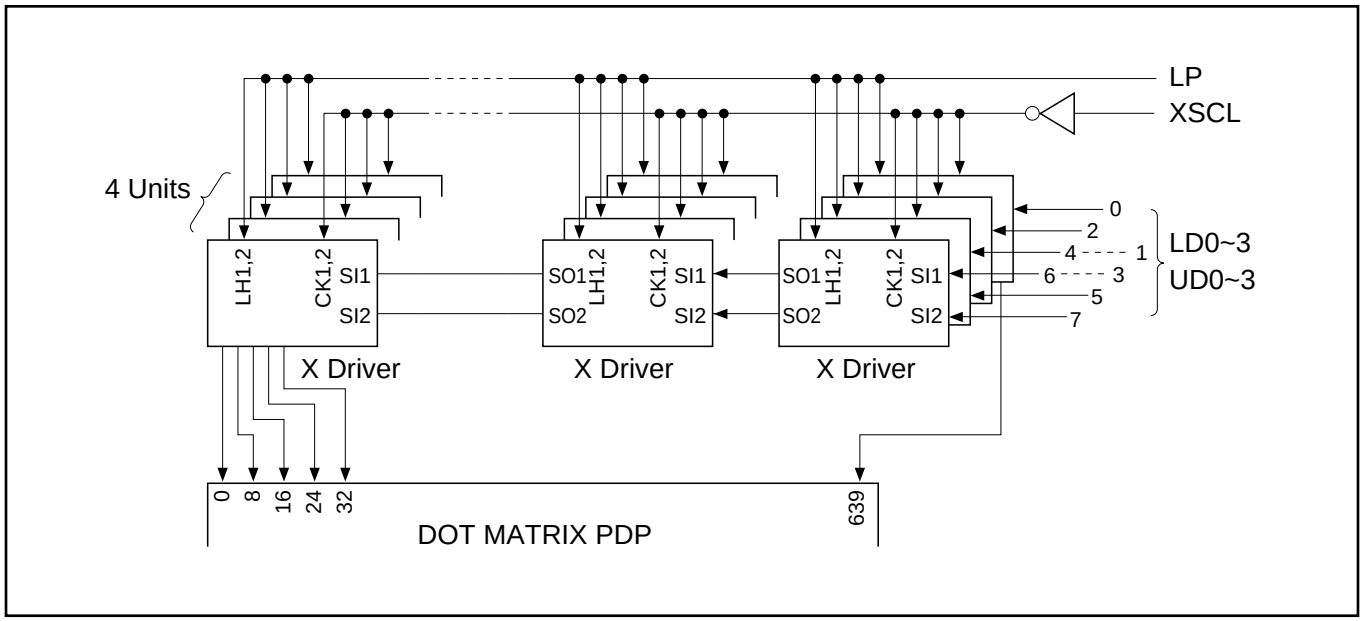
4.3.4.1.2 Connection to SED1600F/1630F <Double panel drive mode>

This is also applicable to the connection to the SED1180F/1190F or SED1600F/1610F.



The LCD also has a blanking period as shown in Fig. 4.2.2.1. For the double panel drive mode, the Y-drive cannot be connected to the upper and lower panels. (The Y-drive must be disconnected separately from the upper and lower panels so that the scanning start data is supplied independently from YD to the SED1345.) (See Fig. 4.3.4.1.2).

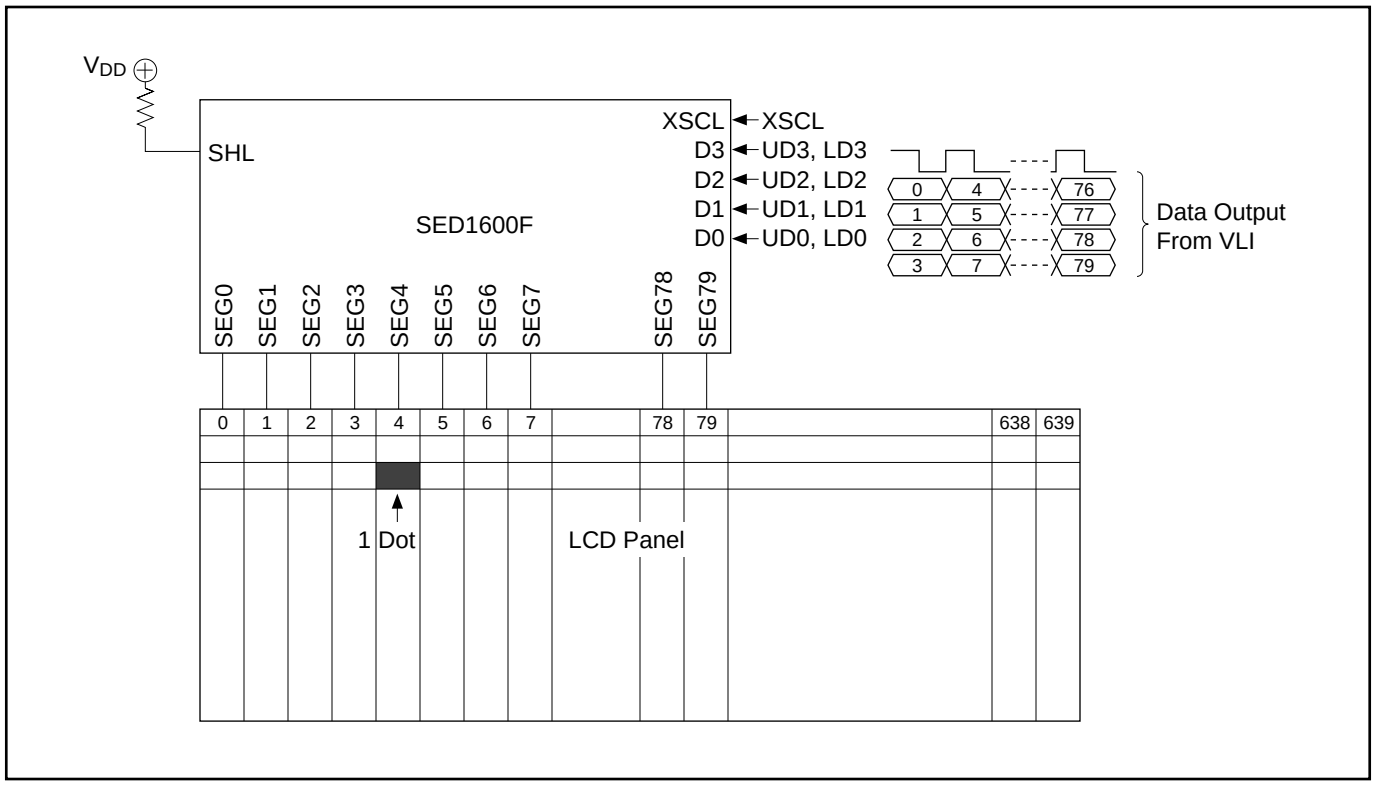
4.3.4.1.3 Connection to SED2032F, SED2000F



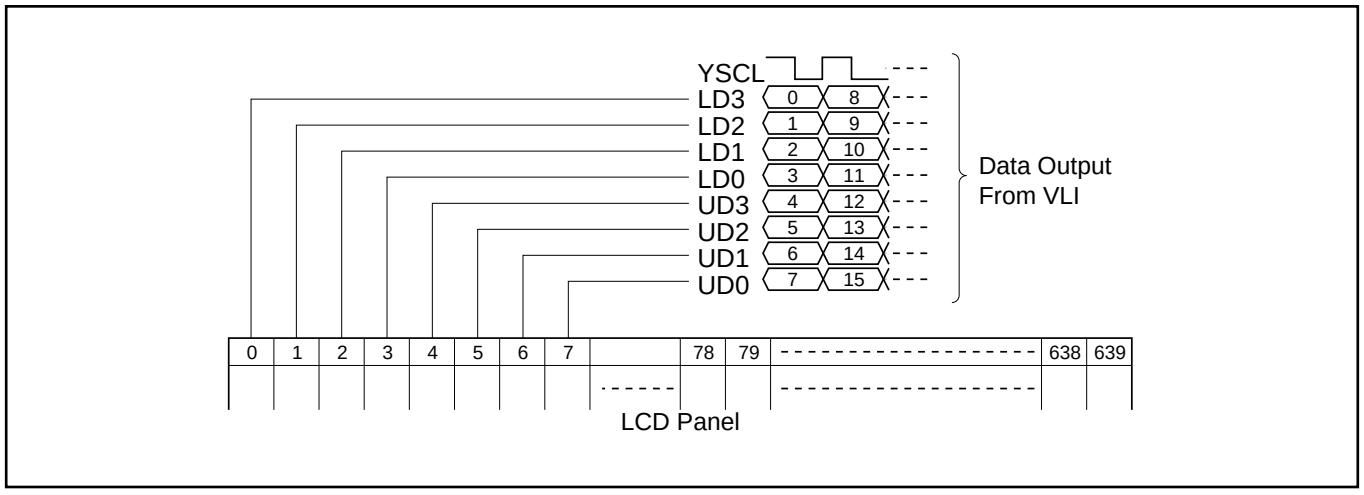
4.3.4.2 Positional Relation between UD3 to UD0/LD3 to LD0 and Display Dots

Figs. 4.3.4.2.1 and 4.3.4.2.2 show the positional relation between display data output from pins UD3 to UD0 and LD3 to LD0 and dots displayed on the LCD panel.

4.3.4.2.1 4-bit Bus Transfer (S6 = “1”)/4–bit x 2 Bus Transfer (S6 = “0”, S0 = “0”)



4.3.4.2.2 8–bit Bus Transfer (S6 = “0”, S0 = “1”)



4.4 MEMORY INTERFACE

4.4.1 Memory

The SED1345F directly manages a 16K to 40K byte memory area. The following two memories can be used:

64K SRAM (8192 words x 8 bits)
256K SRAM (32768 words x 8 bits)

Table 4.13 shows the relation between the LCD panel size and the number of memories used.

TABLE 4.13 LCD Panel Size and Memory

Memory	LCD size			
	640 x 200	**640 x 350**	**640 x 400**	**640 x 480**
64K SRAM	2	—	—	1 + 1
256K SRAM	—	1	1	

The SED1345F accesses a memory at a cycle time (tc) of 4t_{CCK} (t_{CCK}: dot clock cycle). Use fast access time memories (see “AC Characteristics, Memory Interface”.)

fCK = 24 MHz..... tc = 167 ns (typ.)
fCK = 16 MHz..... tc = 250 ns (typ.)

Recommended memory:

64K SRAM ..... SRM2264 (SMOS Systems)
256K SRAM ..... SRM20256 (SMOS Systems)

4.4.2 Memory Control Signals

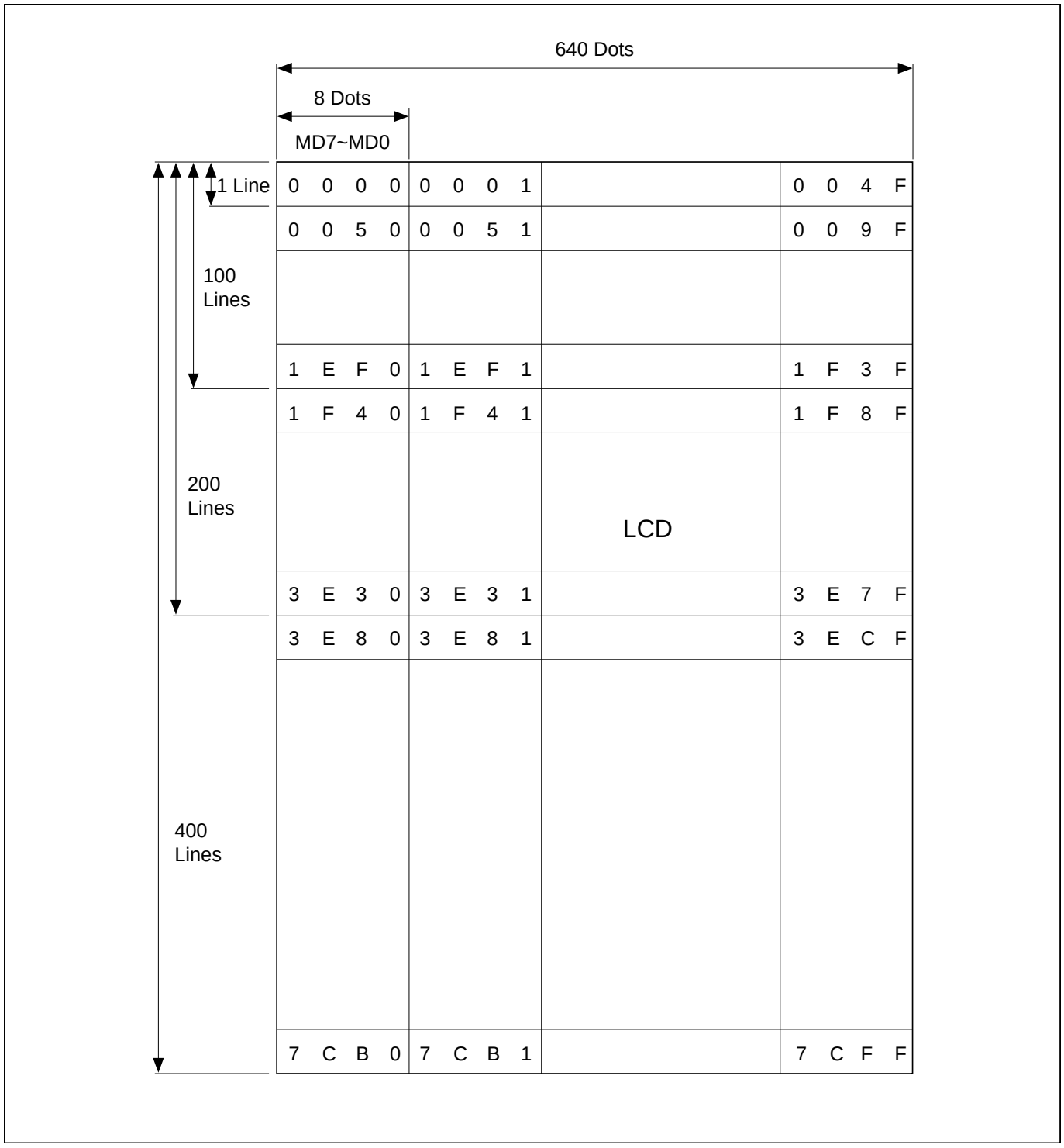
The memory control signal which the SED1345F outputs can directly be connected to memory without using any external circuit.

For the connection of the SED1345F to memory, see Section 6 “System Configuration”.

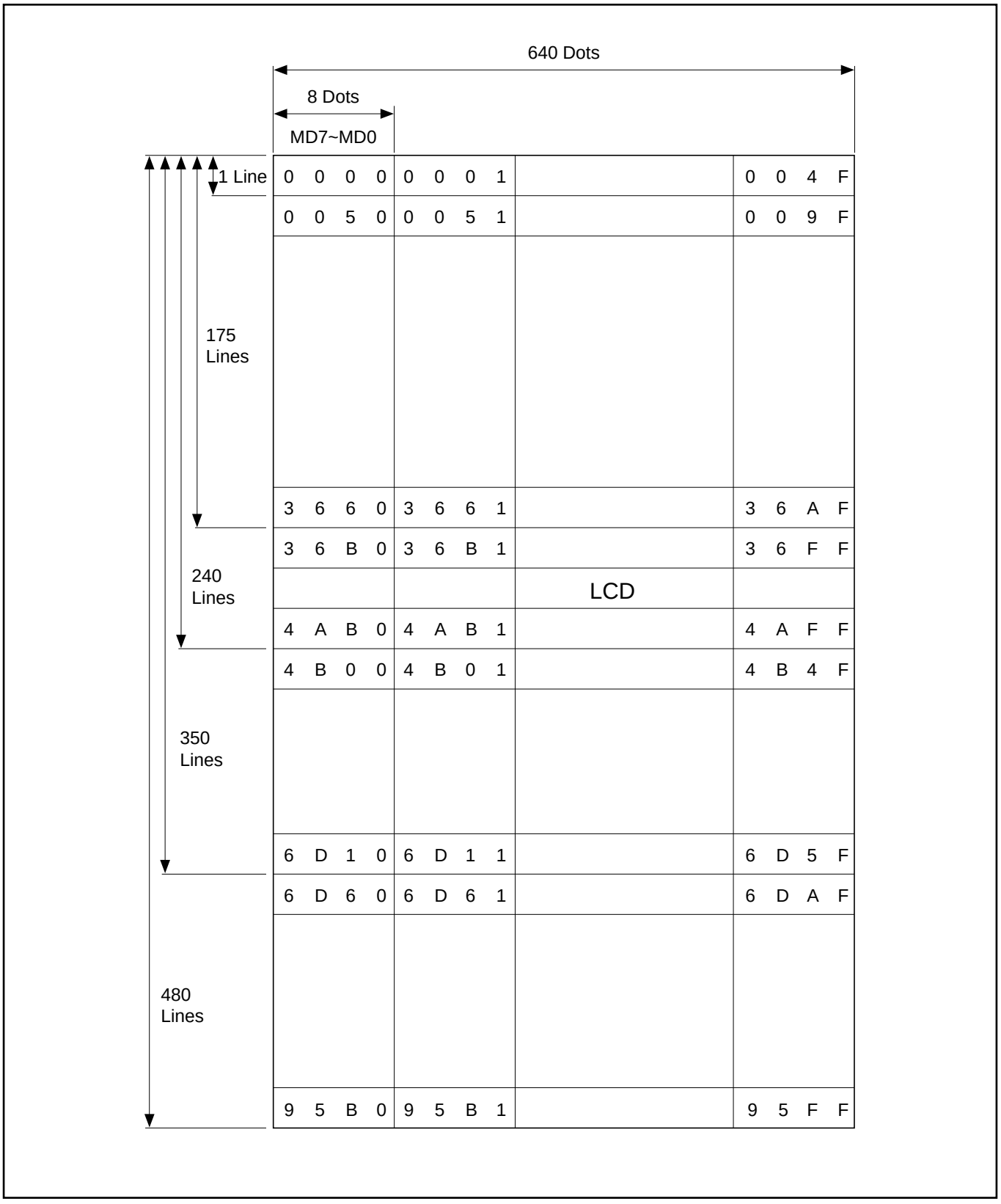
4.4.3 Memory Address

Figs. 4.4.3.1 and 4.4.3.2 show the positional relation between memory addresses output from the VLI and display positions on the LCD panel (straight binary).

4.4.3.1 640 x 200/640 x 400 Dot Panel Memory Addresses and Display Positions



4.4.3.2 640 x 350/640 x 480 Dot Panel Memory Addresses and Display Positions



4.5 POWER-ON CLEAR

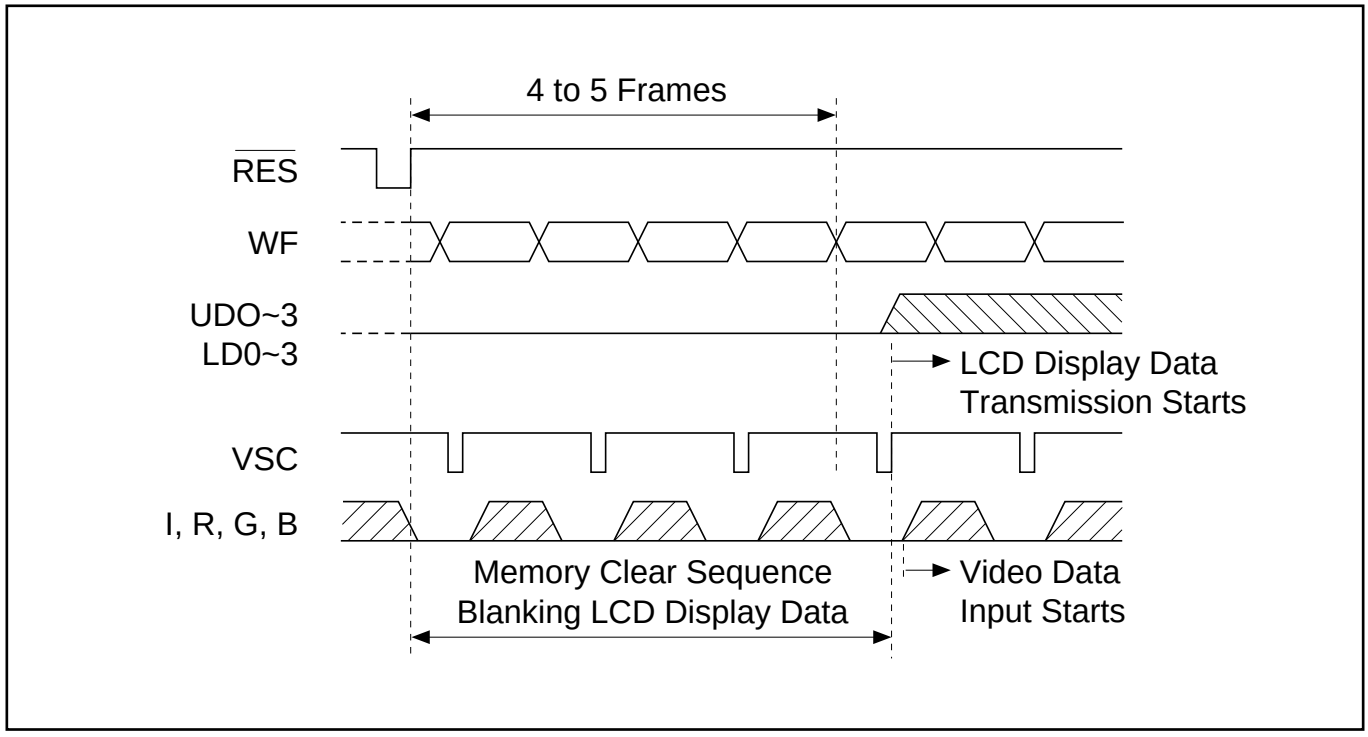
The SED1345F contains a power-on clear function which prevents an unusual display just following power-on or a display of random data from the buffer memory outside the selected display area.

A reset input enables the power-on clear function, causing the SED1345F to perform the following operations:

- Clears the frame buffer memory.
- Blanks the LCD display data.
- Presets the gray mode data of the color pallet.
- Resets internal registers (R0 to R3, R8 to R11) (Sets S5 of R9).

When VSC (vertical sync signal) is input 4 to 5 frames after clearance of the reset input, the power-on clear function is cancelled and normal display operation starts.

4.5.1 Power-on Clear Sequence



No video data is input during a memory clear sequence.

Even during a reset input, LCD-associated signals such as XSCL (shift clock) and LP (latch pulse) are output.

THIS PAGE INTENTIONALLY BLANK

5.0 ELECTRICAL CHARACTERISTICS

5.1 ABSOLUTE MAXIMUM RATINGS

V_{SS} = 0V

Parameter	Symbol	Condition	Ratings	Unit
Supply Voltage	V_{DD}	Based on V_{SS}	–0.3 to 7.0	V
Input Voltage	V_I		–0.3 to V_{DD} + 0.3	V
Output Voltage	V_D		–0.3 to V_{DD} + 0.3	V
I/O Voltage	$V_{I/O}$		–0.3 to V_{DD} + 0.3	V
Output Current/Pin	I_O		–10 to 10	mA
Power Dissipation	P_D		250	mW
Operating Temperature	T_{opr}		0 to 70	°C
Storage Temperature	T_{stg}		–65 to 150	°C
Soldering Temperature and Time	T_{sol}		260°C, 10s (at lead)	—

5.2 RECOMMENDED OPERATING CONDITIONS

V_{SS} = 0V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		4.75	5.00	5.25	V

5.3 DC CHARACTERISTICS

V_{DD} = 5V± 5%, V_{SS} = 0V, Ta = 0 to 70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Average Operating Current Consumption	I_{opr}	fck = 24MHz	—	—	40	mA
High Voltage Input Voltage 1	V_{IH1}	*1	2.0	—	V_{DD} + 0.3	V
Low Level Input Voltage 1	V_{IL1}		–0.3	—	0.8	V
High Level Input Voltage 2	V_{IH2}	*2	4.0	—	V_{DD} + 0.3	V
Low Level Input Voltage 2	V_{IL2}		–0.3	—	0.8	V
High Level Input Voltage 3	V_{IH3}	*3	3.0	—	V_{DD} + 0.3	V
Low Level Input Voltage 3	V_{IL3}		–3.0	—	0.6	V
High Level Output Voltage	V_{OH}	I_{OH} = –2mA	4.35	—	—	V
Low Level Output Voltage	V_{OL}	I_{OL} = 6mA	—	—	0.4	V
Input Current Leakage	I_{LI}	V_I = 0V to V_{DD}	–1	—	1	µA
I/O Current Leakage	$I_{LI/O}$	$V_{I/O}$ = 0V to V_{DD}	–1	—	1	µA

*1 Pad: I, R, G, B, CK, HSC,VSC, MD0 to MD7, A0 to A4, $\overline{CS}$, $\overline{WR}$

*2 Pad: D0 to D3, SEL

*3 Pad: $\overline{RES}$

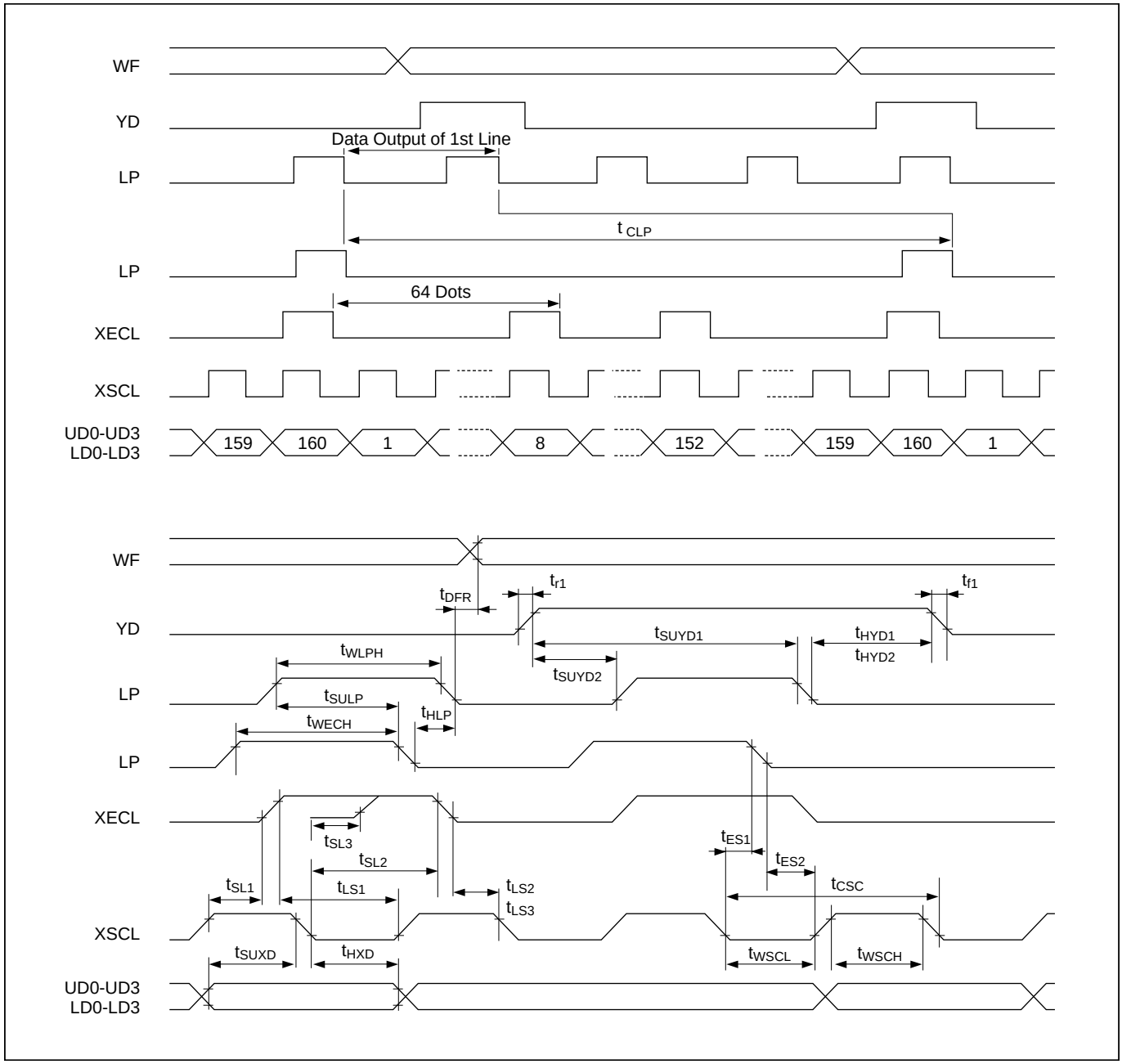
5.4 AC CHARACTERISTICS

5.4.1 LCD Interface

V_{DD} = 5V± 5%, V_{SS} = 0V, Ta = 0 to 70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output Rise Time	t_{ri}	CL = 150pF	—	—	50	ns
Output Fall Time	t_{fl}	CL = 150pF	—	—	50	ns

5.4.1.1 LCD Interface Timing Chart



Output Signal Reference Level: "H" = $V_{DD} \times 0.8V$
"L" = $V_{DD} \times 0.2V$

5.4.1.2 X Driver

V_{DD} = 5V± 5%, V_{SS} = 0V, Ta = 0 to 70°C

Parameter	Symbol	Condition		Min	Typ	Max	Unit
XSCL Cycle Time	t_{CSC}	S6 = “H”		2t1	—	—	ns
		S6 = “L”		4t1			
XSCL Pulse Width	t_{WSCH}	S6 = “H”		t1–20	—	—	ns
		S6 = “L”		2t1–20			
XSCL “L” Pulse Width	t_{WSCL}	S6 = “H”		t1–20	—	—	ns
		S6 = “L”		2t1–20			
UD0–3, LD0–3 Setup Time before XSCL	t_{SUXD}	S6 = “H”		t1–30	—	—	ns
		S6 = “L”		2t1–30			
UD0–3, LD0–3 Hold Time after XSCL	t_{HXD}	S6 = “H”		21–30	—	—	ns
		S6 = “L”		2t1–30			
XSCL to LP Time	t_{SL1}	S5 = “H”	S6 = “H”	0.5t1–30	—	—	ns
			S6 = “L”	t1–30			
XSCL to LP Time	t_{SL2}		S6 = “H”	t1–20	—	—	ns
			S6 = “L”	2t1–20			
LP to XSCL Time	t_{LS1}		S6 = “H”	1.5t1–50	—	—	ns
			S6 = “L”	3t1–50			
LP to XSCL Time	t_{LS2}		S6 = “H”	t1–20	—	—	ns
			S6 = “L”	2t1–20			
XSCL to LP Time	t_{SL3}	S5 = “L”	S5 = “H”	0.5t1–40	—	—	ns
			S6 = “L”	t1–40			
LP to XSCL Time	t_{LS3}		S6 = “H”	0.5t1–40	—	—	ns
			S6 = “L”	t1–40			
LP Cycle Time	t_{CLP}	S0 = “H”		320t1	—	—	ns
		S0 = “L”		640t1			
LP, YSCL “H” Pulse Width	t_{WLPH}	S5 = “H”	S6 = “H”	1.5t1–50	—	—	ns
			S6 = “L”	3t1–50			
		S5 = “L”	S6 = “H”	t1–40	—	—	ns
			S6 = “L”	2t1–40			
LP Setup Time before XECL	t_{SULP}	S5 = “H”, S6 = “H”		t1–50	—	—	ns

V_{DD} = 5V± 5%, V_{SS} = 0V, Ta = 0 to 70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
LP Hold Time after XECL	t_{HLP}	S5 = "H", S6 = "H"	0.5t1–40	—	—	ns
XSCL to XECL Time	t_{ES1}	S5 = "H", S6 = "H"	0.5t1–30	—	—	ns
XECL to XSCL Time	t_{ES2}	S5 = "H", S6 = "H"	0.5t1–40	—	—	ns
XECL "H" Pulse Width	t_{WECH}	S5 = "H", S6 = "H"	1.5t1–50	—	—	ns
WF Output Delay Time After LP, YSCL	t_{DFR}	S5 = "H", S6 = "H"	—	—	100	ns

t1 = 2t_{CCK} (t_{CCK} = dot clock cycle)

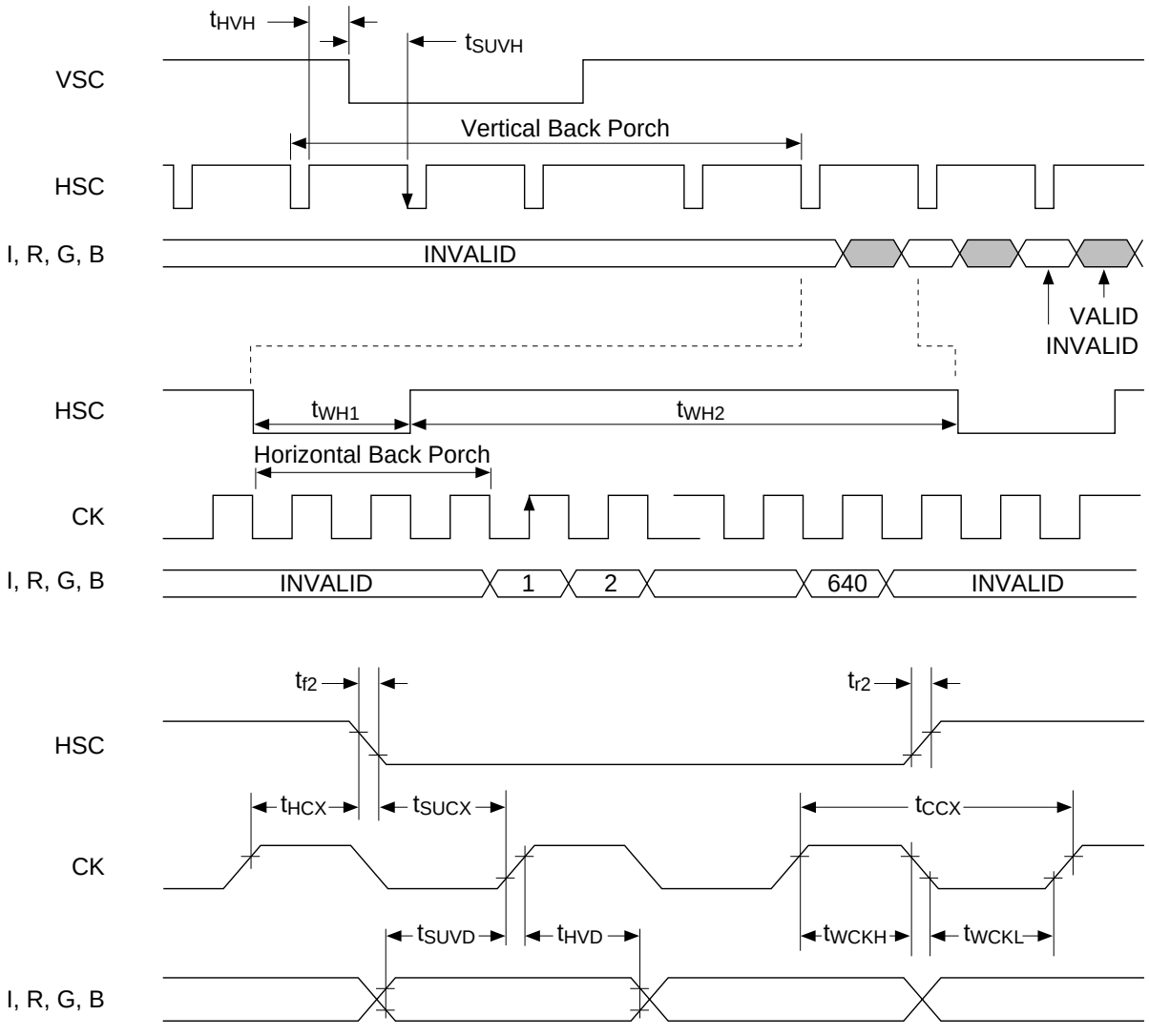
5.4.1.3 Y Driver

V_{DD} = 5V± 5%, V_{SS} = 0V, Ta = 0 to 70°C

Parameter	Symbol	Condition			Min	Typ	Max	Unit
YD Setup Time before LP, YSCL	t_{SUYD1}	S5 = "H"	S0 = "H"		142t1–100	—	—	ns
			S0 = "L"		302t1–100			
YD Hold Time after LP, YSCL	t_{hYD1}		S0 = "H"		18t1–100	—	—	ns
			S0 = "L"		18t1–100			
YD Setup Time before LP, YSCL	t_{SUYD2}	S5 = "L"	S0 = "H"	S6 = "H"	141.5t1–100	—	—	ns
				S6 = "L"	141t1–100			
			S0 = "L"	S6 = "H"	301.5t1–100			
				S6 = "L"	301t1–100			
YD Hold Time after LP, YSCL	t_{HYD2}		S0 = "H"	S6 = "H"	17.5t1–100	—	—	ns
				S6 = "L"	17t1–100			
			S0 = "L"	S6 = "H"	17.5t1–100			
				S6 = "L"	17t1–100			

t1 = 2t_{CCK} (t_{CCK} = dot clock cycle)

5.4.2 Video Signal Interface



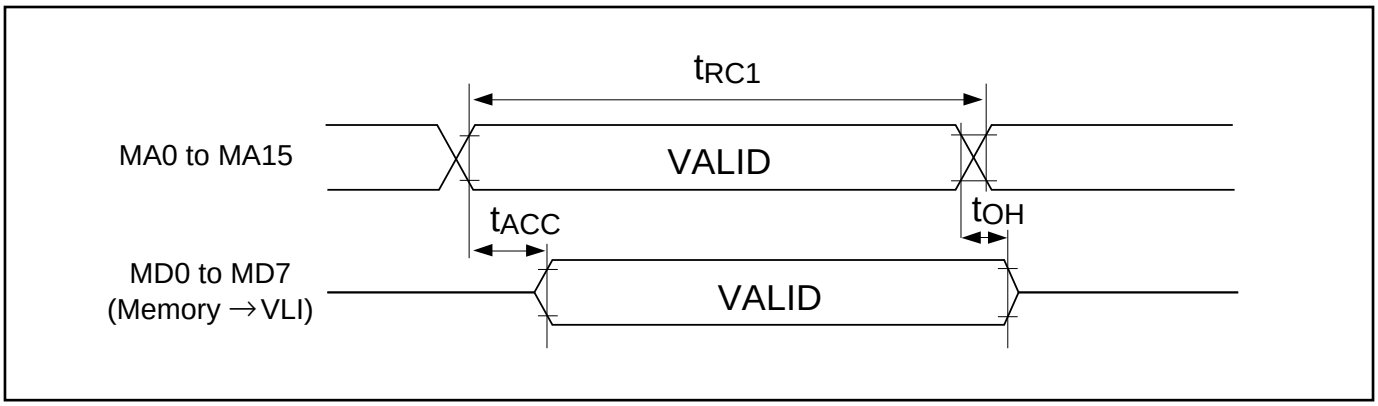
* Input Signal Level Identification Voltages:
"H" level – – – – 2.0V
"L" level – – – – 0.8V

V_{DD} = 5V± 5%, V_{SS} = 0V, Ta = 0 to 70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
CK Cycle Time	t_{CCK}		33	—	—	ns
CK “H” Pulse Width	t_{WCKW}		12	—	—	ns
CK “L” Pulse Width	t_{WCKL}		12	—	—	ns
Input Rise Time	t_{r2}		—	—	5	ns
Input Fall Time	t_{f2}		—	—	5	ns
VD Setup Time Before CK	t_{SUVD}		16	—	—	ns
VD Hold Time After CK	t_{HVD}		2	—	—	ns
CK Setup Time Before HSC	t_{SUCK}		20	—	—	ns
CK Hold Time After HSC	t_{HCK}		0	—	—	ns
HSC Setup Time Before VSC	t_{SUVH}		80	—	—	ns
HSC Hold Time After VSC	t_{HVM}		0	—	—	ns
Active Pulse Width HSC	t_{WH1}		$8t_{CCK}$	—	—	ns
Non-Active Pulse Width HSC	t_{WH2}		$64t_{CCK}$	—	—	ns

5.4.3 Memory Interface

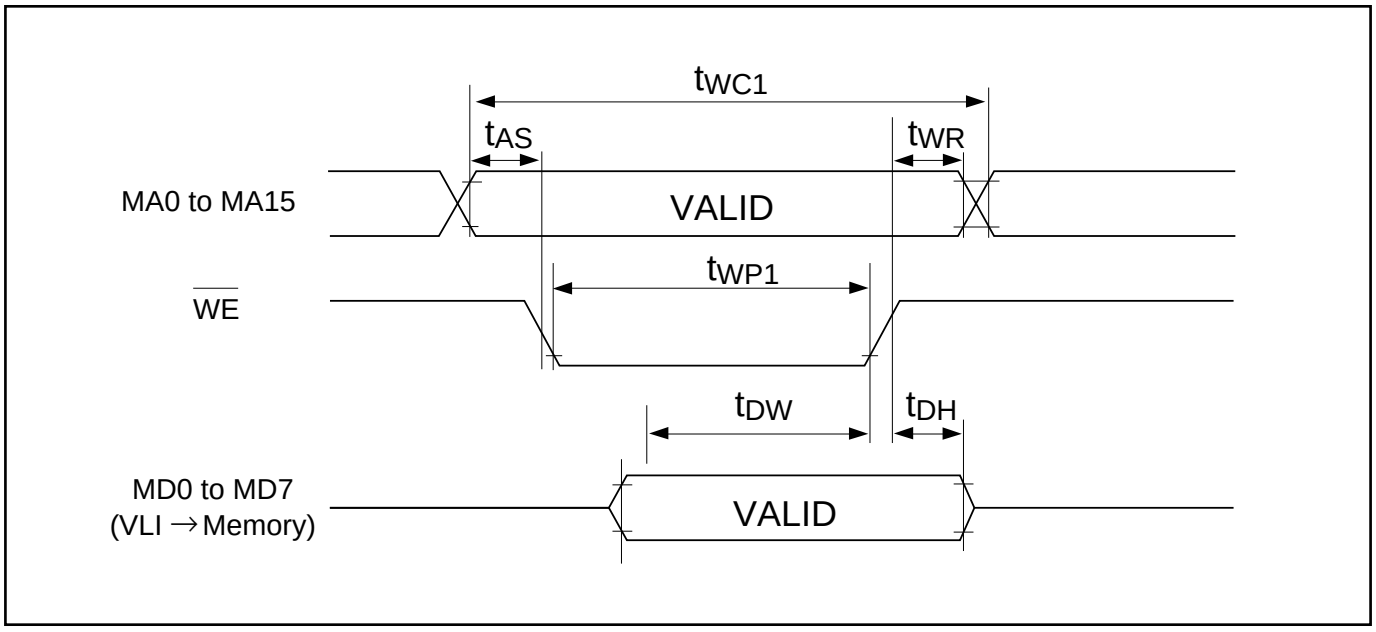
5.4.3.1 SRAM Read Cycle



V_{DD} = 5V± 5%, V_{SS} = 0V, Ta = 0 to 70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Read Cycle Time	t_{RC1}		$4t_{CCK}$	—	—	ns
Address Access Time	t_{ACC}		—	—	$4t_{CCK}$–17	ns
Output Hold Time	t_{OH}		10	—	—	ns

5.4.3.2 SRAM Write Cycle



V_{DD} = 5V± 5%, V_{SS} = 0V, Ta = 0 to 70°C

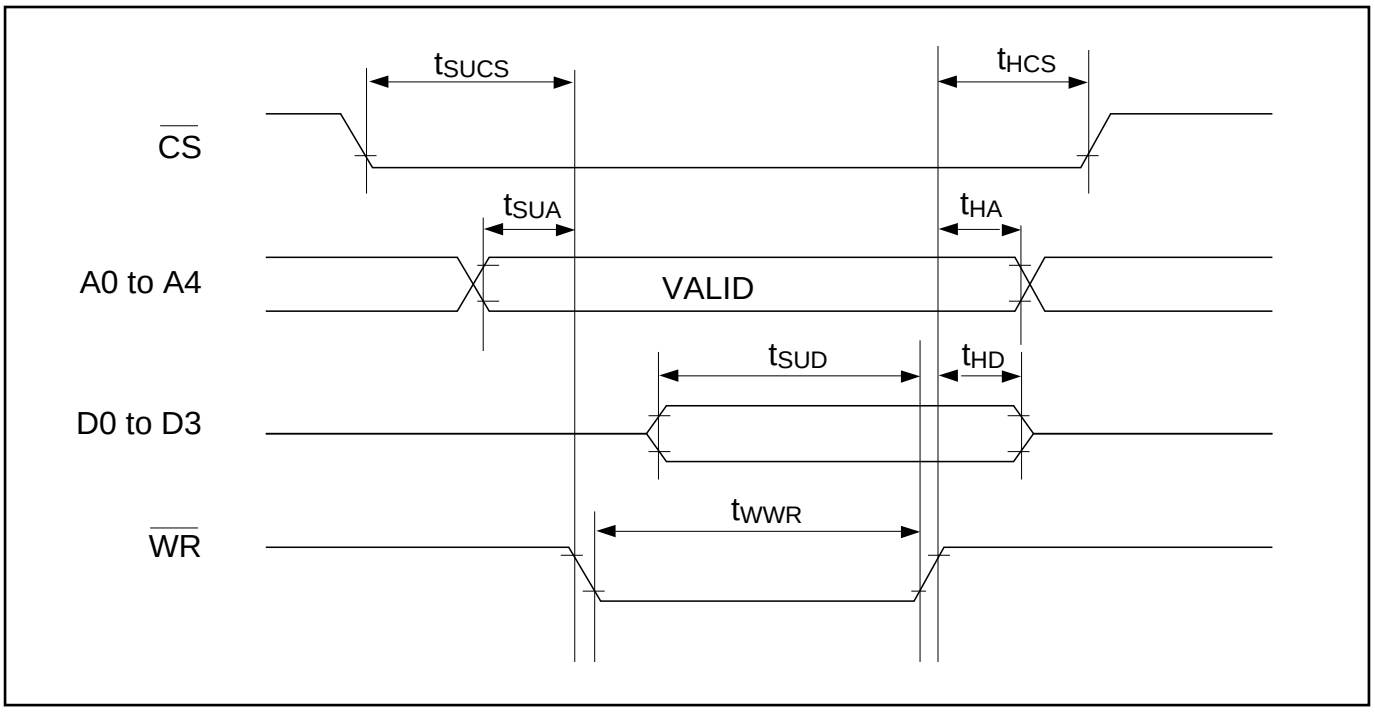
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Write Cycle Time	tWC1		4tCCK	—	—	ns
Write Pulse Width	tWP1		3tCCK–13	—	—	ns
Address Setup Time	tAS		0.5tCCK–14	—	—	ns
Address Hold Time	tWR		0.5tCCK–14	—	—	ns
Data Setup Time	tDW		3tCCK–38	—	—	ns
Data Hold Time	tDH		5	—	—	ns

Input/Output Signal Reference Level: “H” = 2.0V “L” = 0.8V

*tCCK is the cycle time of dot clock (tCCK = 1/fCK).

5.4.4 Register Program

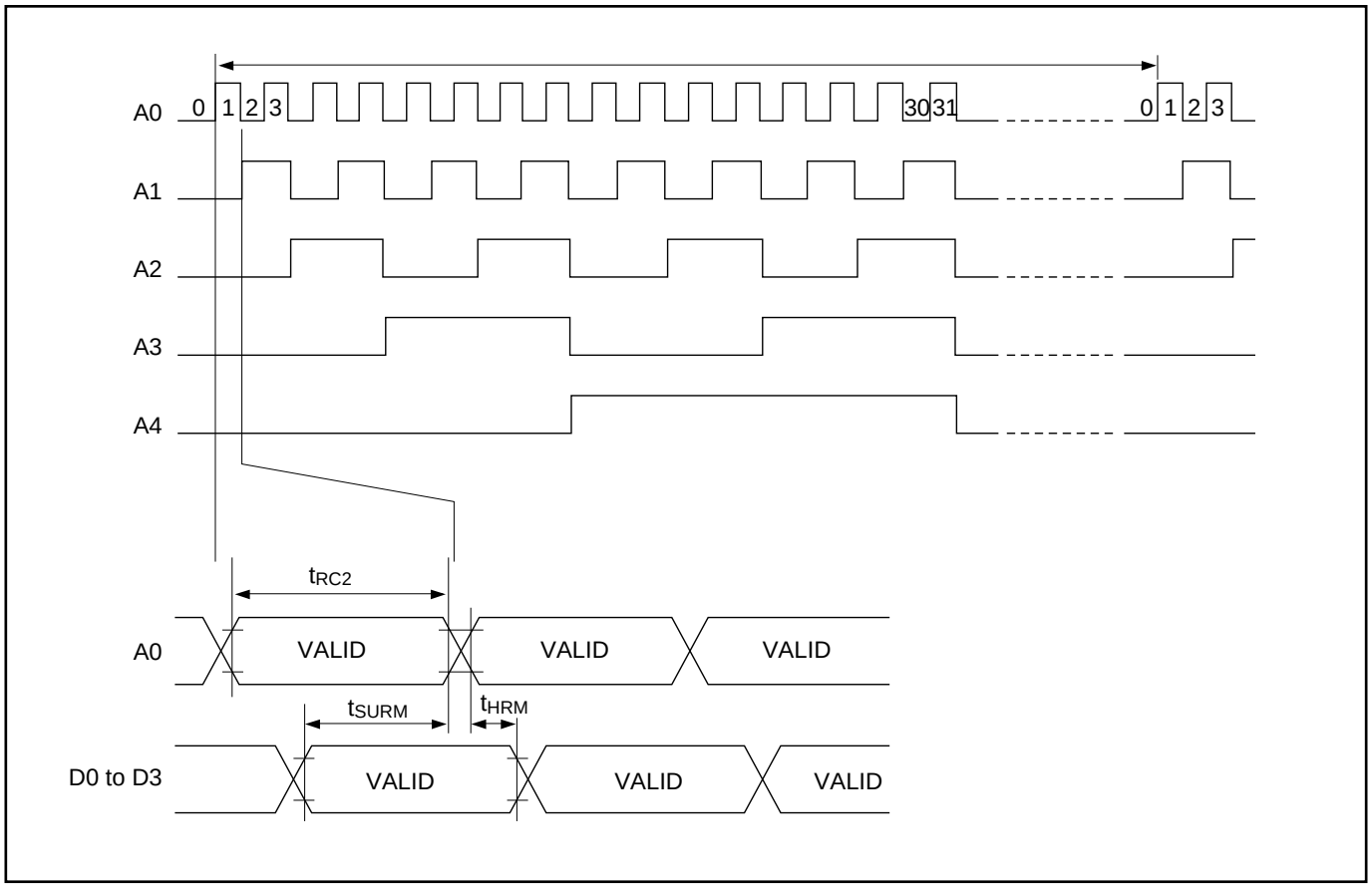
5.4.4.1 Write Data Using MPU



V_{DD} = 5V± 5%, V_{SS} = 0V, Ta = 0 to 70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
$\overline{CS}$ Setup Time	t_{SUCS}		50	—	—	ns
$\overline{CS}$ Hold Time	t_{HCSH}		50	—	—	ns
A0–A4 Setup Time	t_{SUA}		50	—	—	ns
A0–A4 Hold Time	t_{HA}		50	—	—	ns
D0–D3 Setup Time	t_{SUD}		100	—	—	ns
D0–D3 Hold Time	t_{HD}		50	—	—	ns
$\overline{WR}$ Pulse Width	t_{WWR}		50	—	—	ns

5.4.4.2 Write Data Using ROM

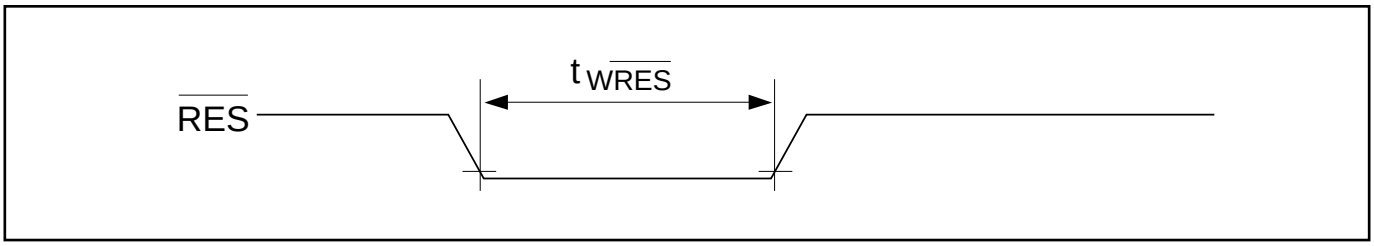


V_{DD} = 5V± 5%, V_{SS} = 0V, Ta = 0 to 70°C

Parameter	Symbol	Condition	Min*	Typ	Max	Unit
ROM Read Cycle Time	t_{RC2}		8t1–100	—	—	ns
D0 to D3 Setup Time	t_{SURM}		100	—	—	ns
D0 to D3 Hold Time	t_{HRM}		10	—	—	ns

* t1 = 2t_{CCK} (t_{CCK} is a cycle time of dot clock)

5.4.5 Reset Input



V_{DD} = 5V± 5%, V_{SS} = 0V, Ta = 0 to 70°C

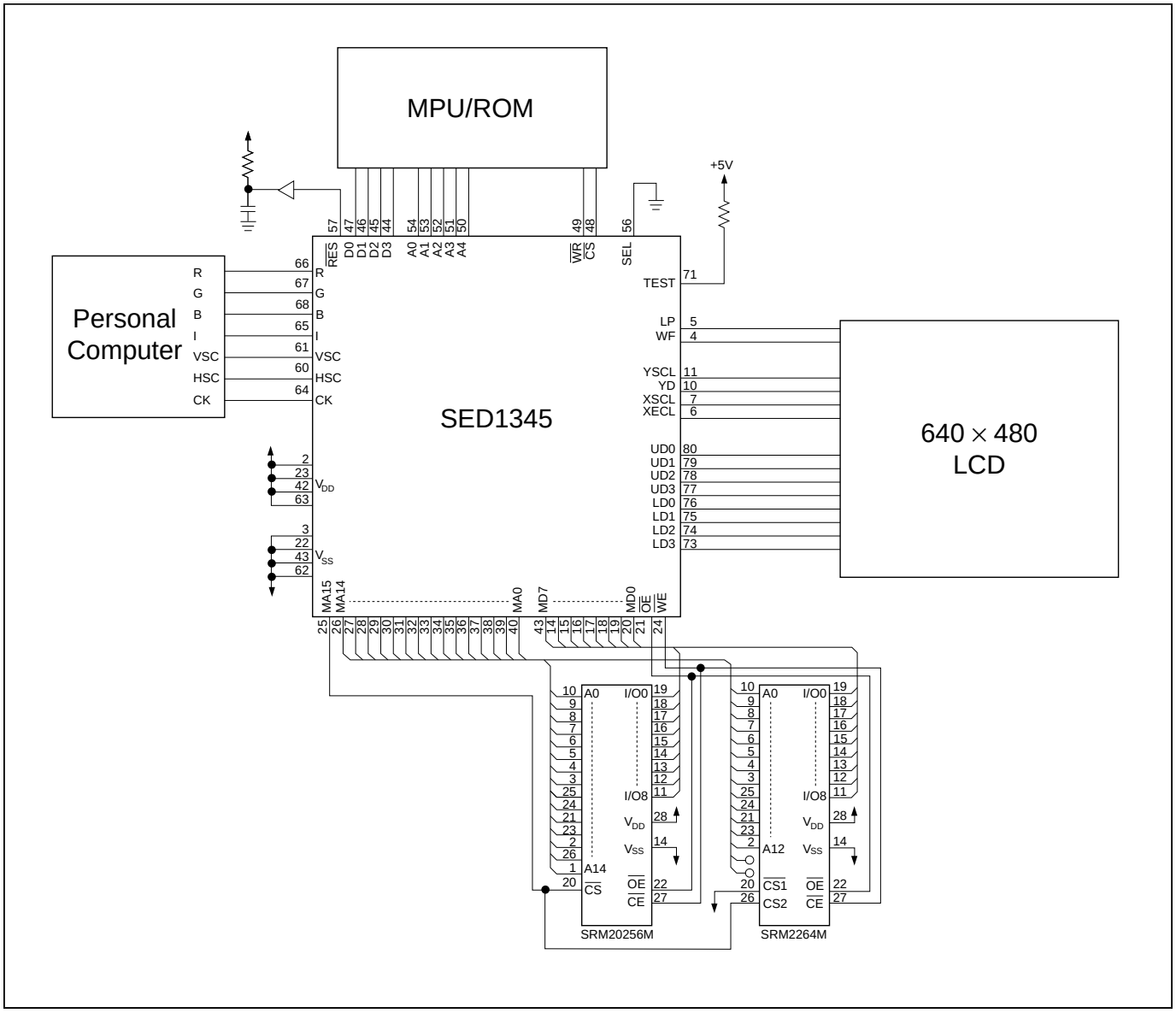
Parameter	Symbol	Condition	Min	Typ	Max	Unit
$\overline{RES}$ Pulse Width	$t_{W\overline{RES}}$		1.0	—	—	ns

Input Signal Reference Level: “H” = 2.0V “L” = 0.8V

t_{CCK} is the cycle time of dot clock (t_{CCK} = 1/f_{CK})

6.0 SYSTEM CONFIGURATION

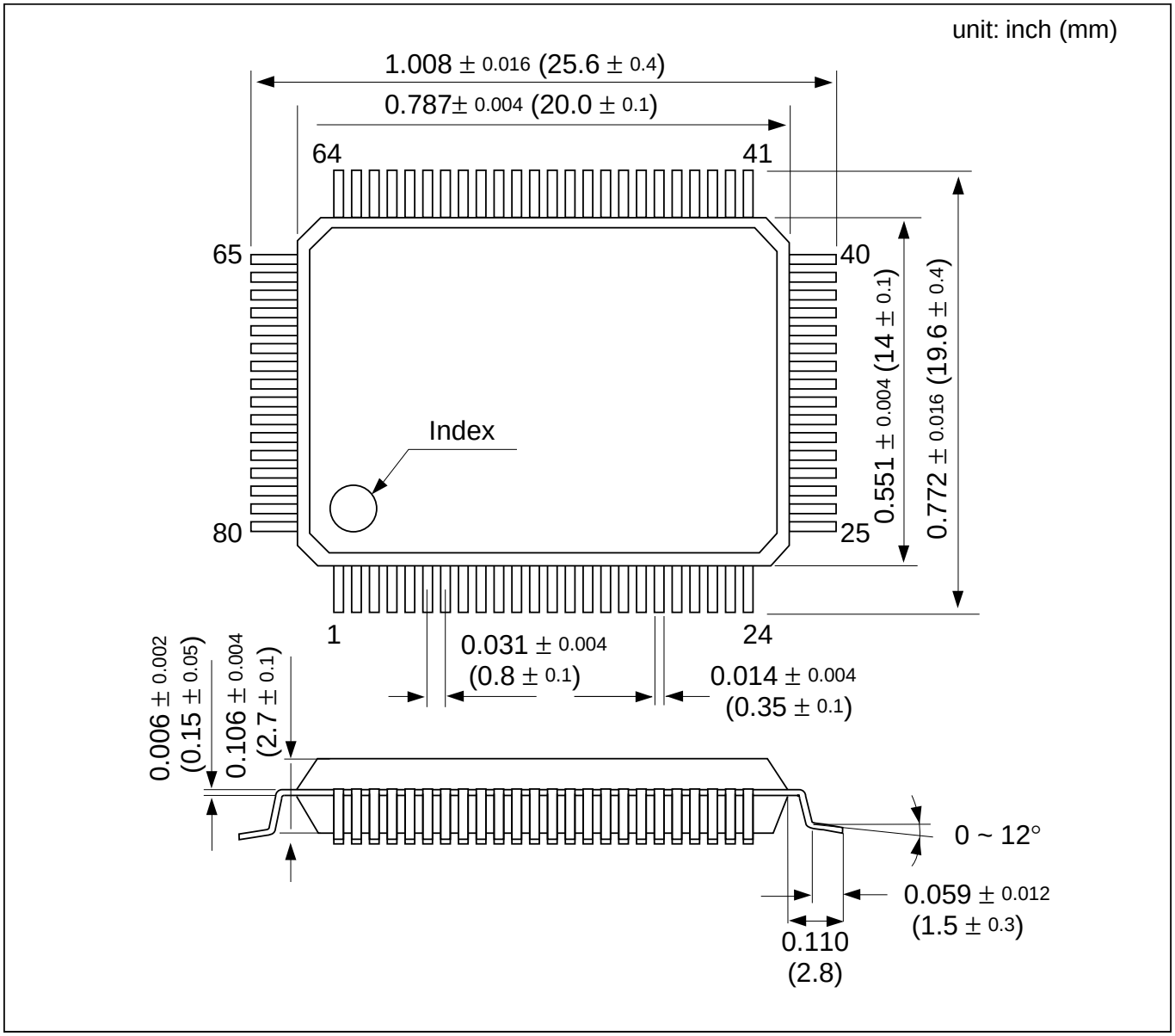
6.1 SYSTEM CONFIGURATION



THIS PAGE INTENTIONALLY BLANK

7.0 PACKAGE DIMENSIONS

7.1 PLASTIC QFP5-80 PIN



* This sketch is for reference only. The delivery specification will define formal dimensions and tolerances.

October 1996 Printed in U.S.A. 369-1.0