

SRM2017C_{10/12}

CMOS 16K-BIT STATIC RAM

- Low Supply Current
- Access Time 100ns/120ns
- 2,048 Words × 8 Bits Asynchronous

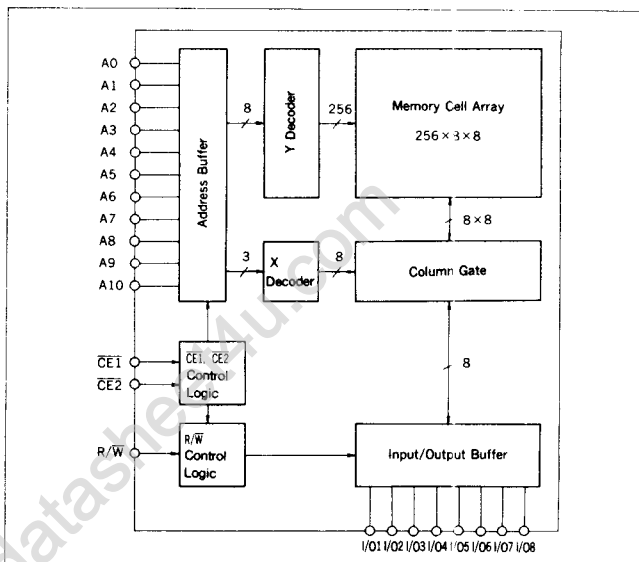
DESCRIPTION

The SRM2017C_{10/12} is a 2,048 words × 8 bits asynchronous, static, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible and the 3-state output allows easy expansion of memory capacity.

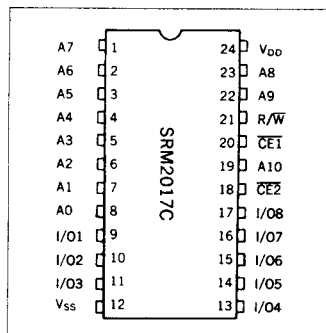
FEATURES

- Access time SRM2017C₁₀ 100ns (Max)
SRM2017C₁₂ 120ns (Max)
- Low supply current standby : 1 μ A (Typ)
operation : SRM2017C₁₀ 30mA (Typ)
SRM2017C₁₂ 25mA (Typ)
- Complete static operation
- Single power supply 5V \pm 10%
- TTL compatible inputs and outputs
- 3-state output with wired-OR capability
- Non-volatile storage with back-up batteries
- Package SRM2017C_{10/12} 24-pin DIP (plastic)
SRM2017M_{10/12} 24-pin SOP (plastic)
SRM2017N_{10/12} 24-pin Skinny DIP (plastic)

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

A0 to A10	Address Input
R/W	Read/Write
CE1	Chip Enable 1
CE2	Chip Enable 2
I/O1 to 8	Data Input/Output
V _{DD}	Power Supply (+5V)
V _{SS}	Power Supply (0V)

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V _{DD}	-0.5 to 7.0	V
Input voltage*	V _I	-0.5 to 7.0	V
Input/output voltage*	V _{I/O}	-0.5 to V _{DD} +0.3	V
Power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to 70	°C
Storage temperature	T _{stg}	-65 to 150	°C
Soldering temp. & time	T _{sol}	260°C, 10s (at lead)	—

*V_I, V_{I/O} = -1.0V when pulse width is 50 ns

■ RECOMMENDED OPERATING CONDITIONS

(T_a=0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V _{DD}		4.5	5.0	5.5	V
	V _{SS}		0	0	0	V
Input voltage	V _{IH}		2.2	3.5	V _{DD} +0.3	V
	V _{IL}		-0.3*	—	0.8	V

*V_{IL}(Min) = -1.0V when pulse width is 50ns

■ ELECTRICAL CHARACTERISTICS

● DC Electrical Characteristics

(V_{DD}=5V±10%, V_{SS}=0V, T_a=0 to 70°C)

Parameter	Symbol	Conditions	SRM2017C ₁₀			SRM2017C ₁₂			Unit
			Min	Typ*	Max	Min	Typ*	Max	
Input leakage current	I _{LI}	V _{DD} =5.5V, V _I =0 to V _{DD}	-1	—	1	-1	—	1	μA
Output leakage current	I _{LO}	CE1 or CE2=V _{IH} , V _{I/O} =0 to V _{DD}	-1	—	1	-1	—	1	μA
Operating supply current	I _{DDO}	CE2 = V _{IL} , I _{I/O} =0mA	—	30	60	—	25	50	mA
	I _{DDO1}	V _{IH} =3.5V, V _{IL} =0.6V, I _{I/O} =0mA	—	16	—	—	16	—	mA
Average operating current	I _{DDA}	Min. cycle, duty = 100%, I _{I/O} =0mA	—	30	60	—	25	50	mA
Standby supply current	I _{DDS}	CE2 = V _{IH}	—	1.5	3.0	—	1.5	3.0	mA
	I _{DDS1}	CE2 = V _{DD} - 0.2V	—	1	50	—	1	50	μA
Output voltage	V _{OL}	I _{OL} = 4.0mA	—	—	0.4	—	—	0.4	V
	V _{OH}	I _{OH} = -1.0mA	2.4	—	—	2.4	—	—	V

*Typical values are for reference, with V_{DD}=5V and T_a=25°C assumed.

● Terminal Capacitance

(f = 1MHz, T_a = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C _I	V _I =0V	—	4	6	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	6	8	pF

● AC Electrical Characteristics

○ Read Cycle

(V_{DD}=5V±10%, V_{SS}=0V, T_a=0 to 70°C)

Parameter	Symbol	Conditions	SRM2017C ₁₀		SRM2017C ₁₂		Unit
			Min	Max	Min	Max	
Read cycle time	t _{RC}	*1	100	—	120	—	ns
Address access time	t _{ACC}		—	100	—	120	ns
CE1 access time	t _{ACE1}		—	55	—	55	ns
CE2 access time	t _{ACE2}		—	100	—	120	ns
CE1 output setup time	t _{CLZ1}	*2	10	—	10	—	ns
CE1 output floating	t _{CHZ1}		0	40	0	40	ns
CE2 output setup time	t _{CLZ2}		10	—	10	—	ns
CE2 output floating	t _{CHZ2}		0	40	0	40	ns
Output hold time	t _{OH}	*1	10	—	10	—	ns

○ Write Cycle

($V_{DD}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=0$ to $70^\circ C$)

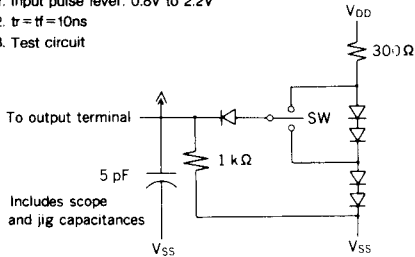
Parameter	Symbol	Conditions	SRM2017C ₁₀		SRM2017C ₁₂		Unit
			Min	Max	Min	Max	
Write cycle time	t_{WC}	*1	100	—	120	—	ns
Chip select time (CE1)	t_{CW1}		80	—	85	—	ns
Chip select time (CE2)	t_{CW2}		80	—	85	—	ns
Address enable time	t_{AW}		80	—	85	—	ns
Address setup time	t_{AS}		0	—	0	—	ns
Write pulse width	t_{WP}		65	—	70	—	ns
Input data setup time	t_{DW}		45	—	50	—	ns
Address hold time	t_{WR}		5	—	5	—	ns
Input data hold time	t_{DH}		0	—	0	—	ns
R/W output setup time	t_{OW}	*3	5	—	10	—	ns
R/W output floating	t_{WHZ}		0	45	0	50	ns

*1 Test conditions.

1. Input pulse level: 0.8V to 2.2V
2. $t_r = t_f = 10ns$
3. Input/output timing reference level: 1.5V
4. Output load: $I_{TTL} + C_L = 100pF$

*3 Test conditions.

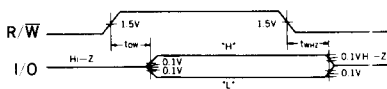
1. Input pulse level: 0.8V to 2.2V
2. $t_r = t_f = 10ns$
3. Test circuit



○ SW is set to the V_{DD} side when measuring Hi-z-high and high-Hi-z: of t_{OW} or t_{WHZ} .

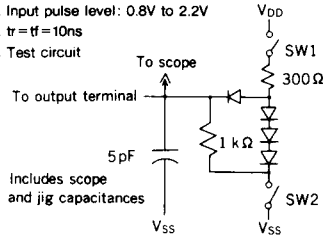
○ SW is set to the V_{SS} side when measuring Hi-z-low and low-Hi-z of t_{OW} or t_{WHZ} .

Output turn-on turn-off times



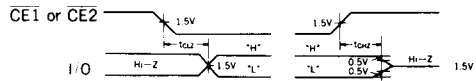
*2 Test conditions.

1. Input pulse level: 0.8V to 2.2V
2. $t_r = t_f = 10ns$
3. Test circuit



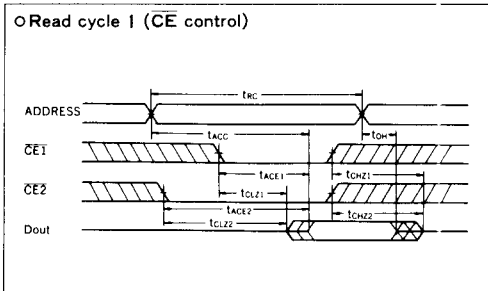
- Both SW1 and SW2 are closed when measuring t_{CHZ} or t_{OLZ} .
- SW1 is open and SW2 is closed when measuring Hi-z-high of t_{OZ} or t_{OLZ} .
- SW1 is closed and SW2 is open when measuring Hi-z-low of t_{OZ} or t_{OLZ} .

Output turn-on turn-off times

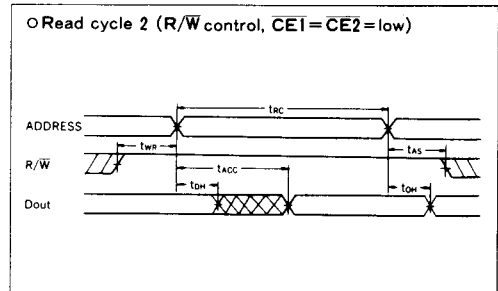


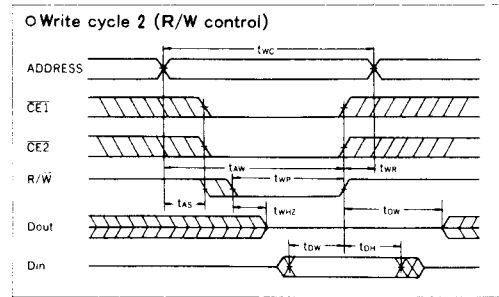
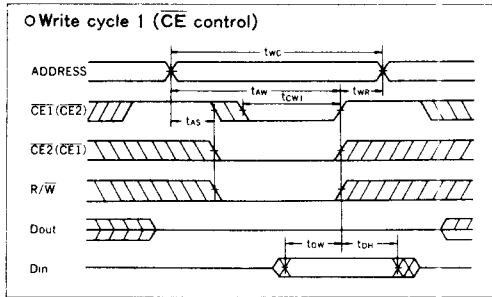
● Timing Chart

○ Read cycle 1 (CE control)



○ Read cycle 2 (R/W control, CE1=CE2=low)





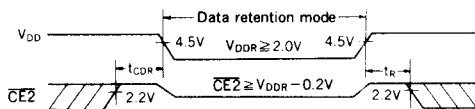
DATA RETENTION CHARACTERISTICS WITH LOW SUPPLY VOLTAGE

($T_a = 0$ to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDR}	$\overline{\text{CE2}} \geq V_{\text{DDR}} - 0.2\text{V}$	2.0	—	5.5	V
Data retention current	I_{DDR}	$V_{\text{DD}} = 3.0\text{V}, \overline{\text{CE2}} \geq 2.8\text{V}$	—	—	25	μA
Chip select data hold time	t_{CDR}	Refer to the figure below.	0	—	—	ns
Operation recovery time	t_{R}		t_{RC}^*	—	—	ns

* t_{RC} : read cycle time

Data retention timing



Note: When retaining data in the stand-by mode, supply voltage can be lowered within a certain range. Read or write cycle cannot be performed while the supply voltage is low.

FUNCTIONS

Truth Table

$\overline{\text{CE1}}$	$\overline{\text{CE2}}$	R/W	A0 to A10	DATA I/O	Mode	I_{DD}
—	H	—	—	Hi-Z	Unselected	$I_{\text{DDs}}, I_{\text{DDs1}}$
H	L	X	X	Hi-Z	Unselected	I_{DD0}
L	L	H	Stable	Output data	Read	I_{DD0}
L	L	L	Stable	Input data	Write	I_{DD0}

X: "H" or "L" —: "H", "L" or "Hi-Z"

Reading Data

Data can be read out if an address is set while $\overline{\text{CE1}}$ is held low, and R/W is held high.

● Writing Data

There are the following three ways of writing data into the memory.

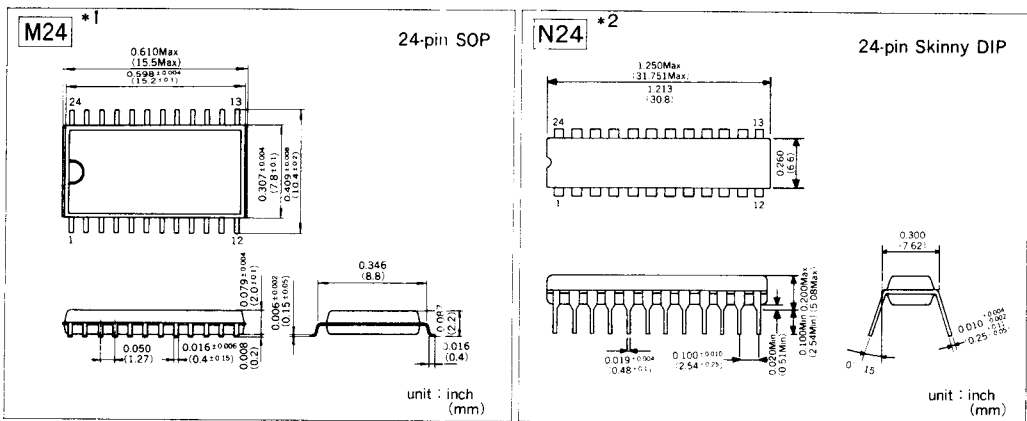
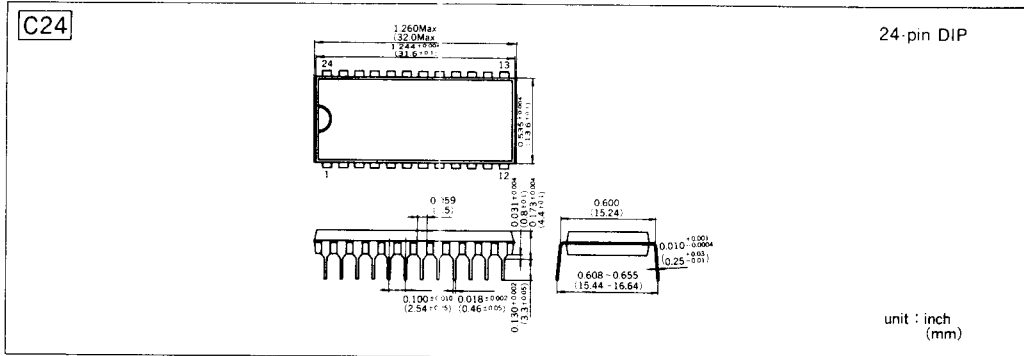
- (1) Hold $\overline{CE1}$ and $\overline{CE2}$ low, set the address, and apply a low pulse to R/\overline{W} .
- (2) Hold R/\overline{W} low and hold $\overline{CE1}$ or $\overline{CE2}$ low, set the address, and apply a low pulse to $\overline{CE2}$ or $\overline{CE1}$.
- (3) Set the address, then apply low pulses to $\overline{CE1}$, $\overline{CE2}$, and R/\overline{W} .

In each case, data from the DATA I/O terminal is fetched into the SRM2017C_{10/12} at the last transition of a section in which $\overline{CE1}$, $\overline{CE2}$, and R/\overline{W} are low. Because the DATA I/O terminal is in high-impedance state when both $\overline{CE1}$ and $\overline{CE2}$ are high or R/\overline{W} is low, competition of data driver and memory output is avoided.

● Standby Mode

When $\overline{CE2}$ is high, SRM2017C_{10/12} is in the stand-by mode and only retains the data. At this time the DATA I/O terminal is in high-impedance state and input of an address, R/\overline{W} signal, or data is prohibited. When $\overline{CE2}$ is above $V_{DD}-0.2V$, current flowing within the SRM2017C_{10/12} chip is only that in the high-resistance portion of the memory cells and leakage current.

■ PACKAGE DIMENSIONS



*1 Represents model SRM2017M_{10/12} that has the same electrical characteristics as model SRM2017C_{10/12}.

*2 Represents model SRM2017N_{10/12} that has the same electrical characteristics as model SRM2017C_{10/12}.

CHARACTERISTICS CURVES

