

# SRM20256L<sub>10/12</sub>

## CMOS 256K-BIT STATIC RAM

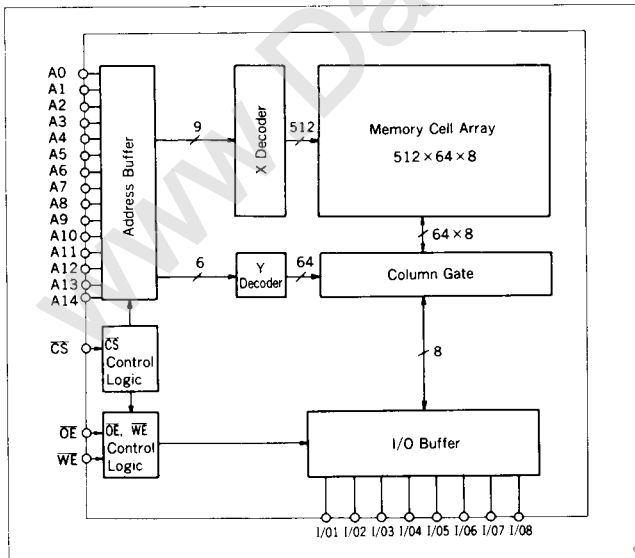
### DESCRIPTION

The SRM20256L<sub>10/12</sub> is a 32,768 words x 8 bits asynchronous, static, random access memory fabricated using an advanced CMOS technology. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refresh circuit. Input and output ports are TTL compatible and the three-state output allows easy expansion of memory capacity.

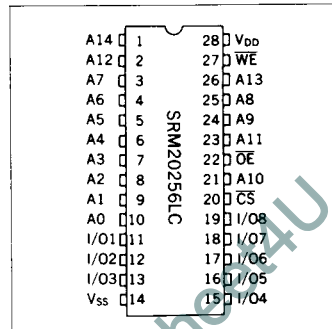
### FEATURES

- Fast access time ..... SRM20256L<sub>10</sub> 100ns (Max)  
SRM20256L<sub>12</sub> 120ns (Max)
- Low supply current ..... Standby : 2 $\mu$ A (Typ)  
Operation: 13mA/1MHz (Typ)
- Completely static ..... No clock required
- Single power supply ..... 5V  $\pm$  10%
- TTL compatible inputs and outputs
- 3-state output
- Battery back-up operation
- Package ..... SRM20256LC<sub>10/12</sub> 28-pin DIP (plastic)  
SRM20256LM<sub>10/12</sub> 28-pin SOP (plastic)  
SRM20256LS<sub>10/12</sub> 28-pin Shrink DIP (plastic)  
SRM20256L<sub>10/12</sub> 28-pin TSOP (plastic)

### BLOCK DIAGRAM



### PIN CONFIGURATION



### PIN DESCRIPTION

A0 to A14	Address Input
WE	Write Enable
OE	Output Enable
CS	Chip Select
I/O1 to 8	Data Input/Output
V <sub>DD</sub>	Power Supply (+5V)
V <sub>SS</sub>	Power Supply (0V)

### ■ ABSOLUTE MAXIMUM RATINGS

(V<sub>SS</sub> = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V <sub>DD</sub>	-0.5 to 7.0	V
Input voltage	V <sub>I</sub>	-0.5* to 7.0	V
Input/Output voltage	V <sub>I/O</sub>	-0.5* to V <sub>DD</sub> +0.3	V
Power dissipation	P <sub>D</sub>	1.0	W
Operating temperature	T <sub>opr</sub>	0 to 70	°C
Storage temperature	T <sub>stg</sub>	-65 to 150	°C
Soldering temperature and time	T <sub>sol</sub>	260°C, 10s (Lead only)	—

\*V<sub>I</sub>, V<sub>I/O</sub>(Min) = -1.0V when pulse width is less or equal to 50ns

### ■ DC RECOMMENDED OPERATING CONDITIONS

(V<sub>SS</sub> = 0V, T<sub>a</sub> = 0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V <sub>DD</sub>		4.5	5.0	5.5	V
	V <sub>SS</sub>		0	0	0	V
Input voltage	V <sub>IH</sub>		2.2	3.5	V <sub>DD</sub> +0.3	V
	V <sub>IL</sub>		-0.3*	0	0.8	V

\*V<sub>IL</sub>(Min) = -1.0V when pulse width is less or equal to 50ns

### ■ ELECTRICAL CHARACTERISTICS

#### ● DC Electrical Characteristics

(V<sub>DD</sub> = 5V ± 10%, V<sub>SS</sub> = 0V, T<sub>a</sub> = 0 to 70°C)

Parameter	Symbol	Conditions	SRM20256LC10			SRM20256LC12			Unit
			Min	Typ*	Max	Min	Typ*	Max	
Input leakage	I <sub>LI</sub>	V <sub>I</sub> = 0 to V <sub>DD</sub>	-1	—	1	-1	—	1	μA
Standby supply current	I <sub>DDs</sub>	CS = V <sub>IH</sub>	—	1.5	3.0	—	1.5	3.0	mA
	I <sub>DDs1</sub>	CS ≥ V <sub>DD</sub> - 0.2V	—	2	100	—	2	100	μA
Average operating current	I <sub>DDA</sub>	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> I <sub>I/O</sub> = 0mA t <sub>cyc</sub> = Min	—	40	70	—	37	70	mA
	I <sub>DDA1</sub>	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> I <sub>I/O</sub> = 0mA t <sub>cyc</sub> = 1μs	—	13	—	—	13	—	mA
Operating supply current	I <sub>DDO</sub>	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> I <sub>I/O</sub> = 0mA	—	35	65	—	35	65	mA
Output leakage	I <sub>LO</sub>	CS = V <sub>IH</sub> or WE = V <sub>IL</sub> or OE = V <sub>IH</sub> V <sub>I/O</sub> = 0 to V <sub>DD</sub>	-1	—	1	-1	—	1	μA
High level output voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0mA	2.4	V <sub>DD</sub> -0.1	—	2.4	V <sub>DD</sub> -0.1	—	V
Low level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1mA	—	0.2	0.4	—	0.2	0.4	V

\*Typical values are measured at T<sub>a</sub> = 25°C and V<sub>DD</sub> = 5.0V

#### ● Terminal Capacitance

(f = 1MHz, T<sub>a</sub> = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address Capacitance	C <sub>ADD</sub>	V <sub>ADD</sub> = 0V	—	—	10	pF
Input Capacitance	C <sub>I</sub>	V <sub>I</sub> = 0V	—	—	10	pF
I/O Capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0V	—	—	10	pF

#### ● AC Electrical Characteristics

##### ○ Read Cycle

(V<sub>DD</sub> = 5V ± 10%, V<sub>SS</sub> = 0V, T<sub>a</sub> = 0 to 70°C)

Parameter	Symbol	Conditions	SRM20256LC10		SRM20256LC12		Unit
			Min	Max	Min	Max	
Read cycle time	t <sub>RC</sub>		100	—	120	—	ns
Address access time	t <sub>ACC</sub>	*1	—	100	—	120	ns
CS access time	t <sub>ACS</sub>		—	100	—	120	ns
OE access time	t <sub>OE</sub>		—	50	—	60	ns
CS output set time	t <sub>CLZ</sub>	*2	10	—	10	—	ns
CS output floating	t <sub>CHZ</sub>		—	35	—	40	ns
OE output set time	t <sub>OLZ</sub>		5	—	5	—	ns
OE output floating	t <sub>OHZ</sub>		—	35	—	40	ns
Output hold time	t <sub>OH</sub>	*1	10	—	10	—	ns

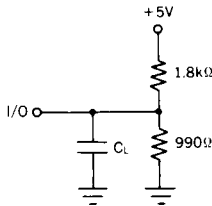
○ Write Cycle

( $V_{DD}=5V \pm 10\%$ ,  $V_{SS}=0V$ ,  $T_a=0$  to  $70^\circ C$ )

Parameter	Symbol	Conditions	SRM20256LC10		SRM20256LC12		Unit
			Min	Max	Min	Max	
Write cycle time	$t_{WC}$	*1	100	—	120	—	ns
Chip select time	$t_{CW}$		80	—	85	—	ns
Address valid to end of write	$t_{AW}$		80	—	85	—	ns
Address setup time	$t_{AS}$		0	—	0	—	ns
Write pulse width	$t_{WP}$		75	—	80	—	ns
Address hold time	$t_{WR}$		0	—	0	—	ns
Input data set time	$t_{DW}$		45	—	50	—	ns
Input data hold time	$t_{DH}$		0	—	0	—	ns
Write to Output floating	$t_{WHZ}$	*2	—	35	—	40	ns
Output Active from end of write	$t_{OW}$		10	—	10	—	ns

\*1 Test Conditions

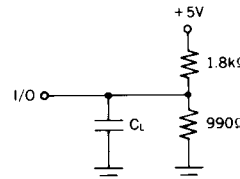
1. Input pulse level : 0.6V to 2.4V
2.  $t_r = t_f = 5ns$
3. Input and output timing reference levels : 1.5V
4. Output load  $C_L = 100pF$



$C_L = 100pF$  (Includes Jig Capacitance)

\*2 Test Conditions

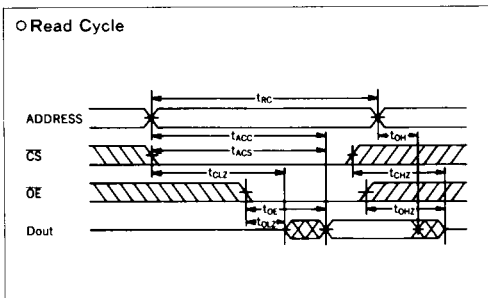
1. Input pulse level : 0.6V to 2.4V
2.  $t_r = t_f = 5ns$
3. Input timing reference levels : 1.5V
4. Output timing reference levels :  $\pm 200mV$  (the level displaced from stable output voltage level)
5. Output load  $C_L = 5pF$



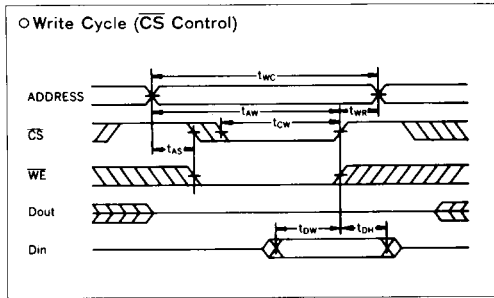
$C_L = 5pF$  (Includes Jig Capacitance)

● Timing Chart

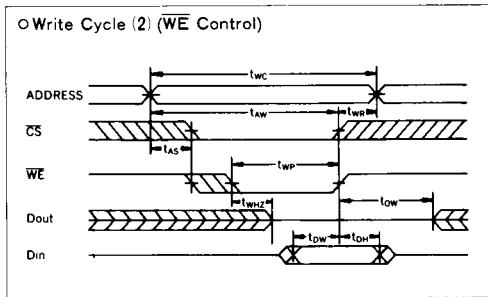
○ Read Cycle



○ Write Cycle ( $\overline{CS}$  Control)



○ Write Cycle (2) ( $\overline{WE}$  Control)



Note :

1. During read cycle time,  $\overline{WE}$  is to be "H" level.
2. During write cycle time that is controlled by  $\overline{CS}$ , Output Buffer is in high impedance state, whether  $\overline{OE}$  level is "H" or "L".
3. During write cycle time that is controlled by  $\overline{WE}$ , Output Buffer is in high impedance state if  $\overline{OE}$  is "H" level.

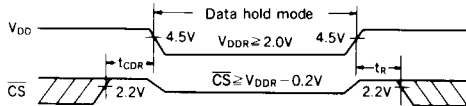
### DATA RETENTION CHARACTERISTIC WITH LOW VOLTAGE POWER SUPPLY

(V<sub>SS</sub> = 0V, T<sub>a</sub> = 0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V <sub>DDR</sub>		2.0	—	5.5	V
Data retention current	I <sub>DDR</sub>	V <sub>DD</sub> = 3V, $\overline{CS} \geq V_{DDR} - 0.2V$	—	1	50	μA
Chip select data hold time	t <sub>CDR</sub>		0	—	—	ns
Operation recovery time	t <sub>r</sub>		t <sub>rc</sub> *	—	—	ns

\*t<sub>rc</sub> = Read cycle time

#### Data retention timing



### FUNCTIONS

#### ● Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	A0 to A14	DATA I/O	Mode	I <sub>DD</sub>
H	—	—	—	Hi-Z	Standby	I <sub>DDs</sub> , I <sub>DDs1</sub>
L	X	L	Stable	D <sub>IN</sub>	Write	I <sub>DDA</sub> , I <sub>DDA1</sub>
L	L	H	Stable	D <sub>OUT</sub>	Read	I <sub>DDA</sub> , I <sub>DDA1</sub>
L	H	H	Stable	Hi-Z	Output disable	I <sub>DDA</sub> , I <sub>DDA1</sub>

#### ● Read Mode

The Data appear when the address is set while holding  $\overline{CS} = "L"$ ,  $\overline{OE} = "L"$  and  $\overline{WE} = "H"$ . When  $\overline{OE} = "H"$ , Data I/O terminals are in high impedance state, that makes circuit design and bus control easy.

#### ● Write Mode

There are the following 3 ways of writing data into memory.

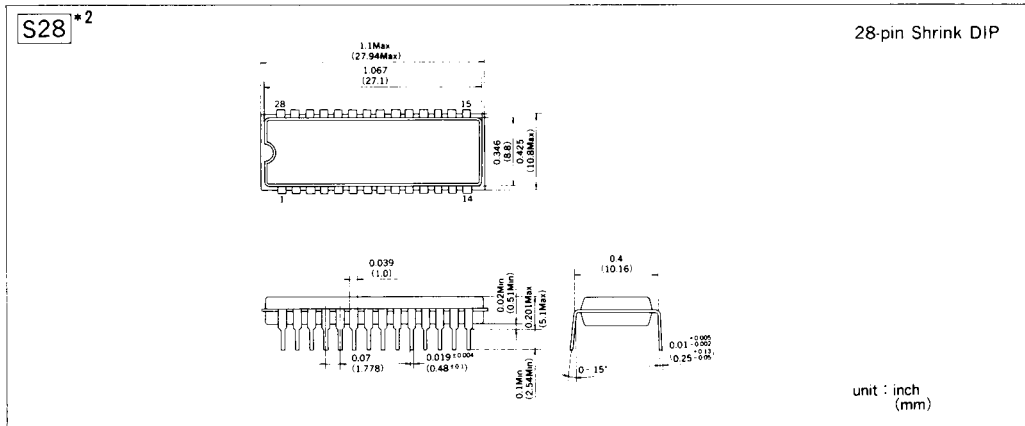
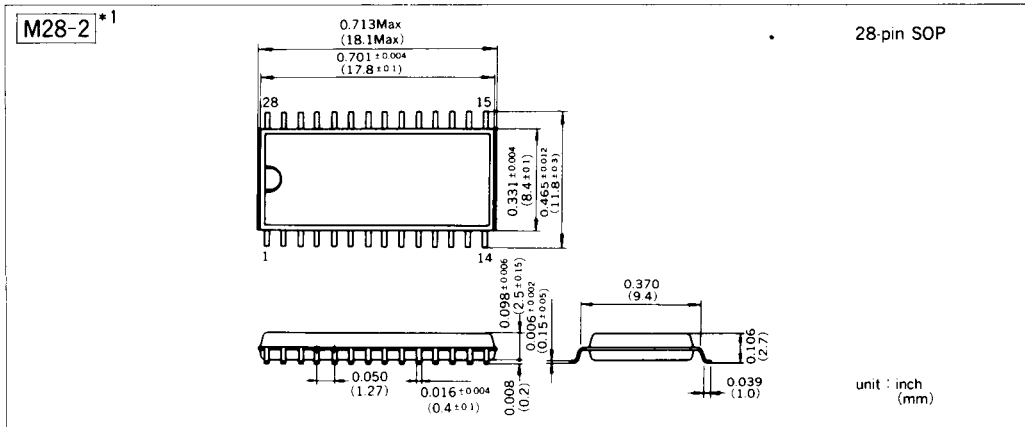
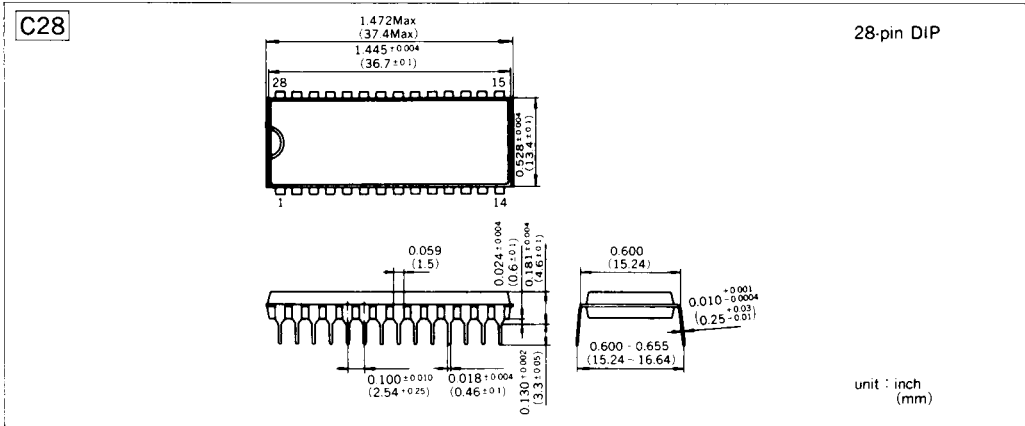
- (1) Hold  $\overline{CS} = "L"$  and  $\overline{WE} = "L"$ , set address.
- (2) Hold  $\overline{CS} = "L"$  then set address and give "L" pulse to  $\overline{WE}$ .
- (3) After setting addresses, give "L" pulse to both  $\overline{CS}$  and  $\overline{WE}$ .

In above any case data on the DATA I/O terminals are latched up into the SRM20256L10/12 when  $\overline{CS}$  or  $\overline{WE}$  is in positive-going. Since DATA I/O terminals are high impedance when  $\overline{CS}$  or  $\overline{OE} = "H"$ , bus contention between data driver and memory outputs can be avoided.

#### ● Standby Mode

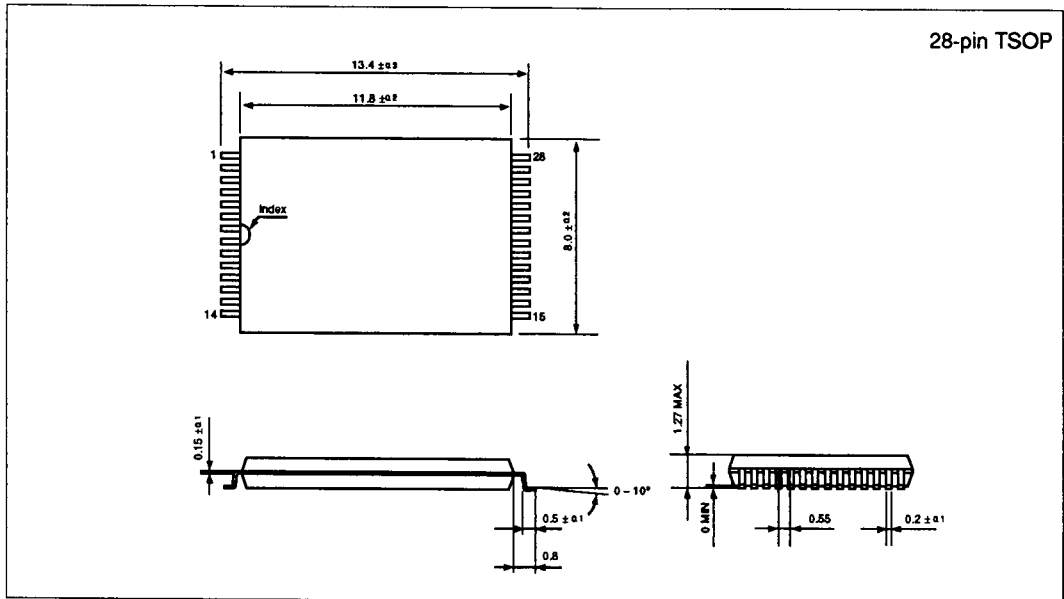
When  $\overline{CS}$  is "H" the SRM20256L10/12 become in the stand-by mode. In this mode, data I/O terminals are Hi-Z, and all inputs of addresses, WE and data can be any "H" or "L". When  $\overline{CS}$  is over than V<sub>DD</sub> - 0.2V, the SRM20256L10/12 is in the data retention battery back-up mode, in this case, there is a small current in the SRM20256L10/12 which flow through the high resistances of the memory cells.

PACKAGE DIMENSIONS



\*1 Represents SRM20256LM10/12 that has the same electrical characteristics as SRM20256LC10/12.  
 \*2 Represents SRM20256LS10/12 that has the same electrical characteristics as SRM20256LC10/12.

## PACKAGE DIMENSIONS



CHARACTERISTICS CURVES

