EPSON

SRM20V100LLMX7

1M-Bit Static RAM

Low Voltage Operation Products

- Low Supply Voltage
- Wide Temperature Range
- Low Supply Current
- Access Time 70ns (2.7V)
- 131,072 Words×8-Bit Asynchronous

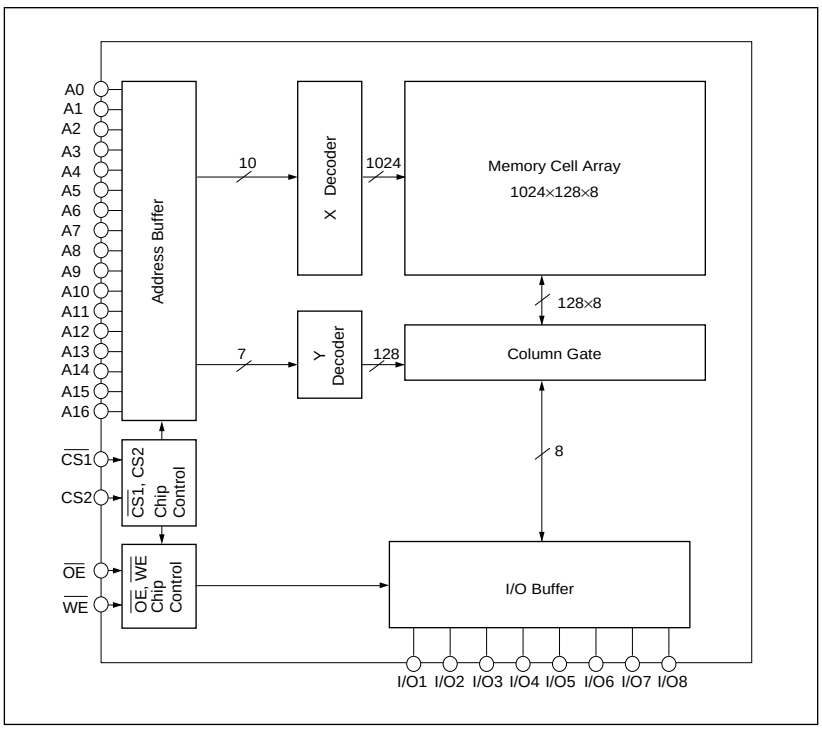
■ DESCRIPTION

The SRM20V100LLMX7 is an 131,072 words×8-bit asynchronous, static, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. And —25 to 85°C operating temperature range makes it ideal for portable equipment. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible and 3-state output allows easy expansion of memory capacity.

■ FEATURES

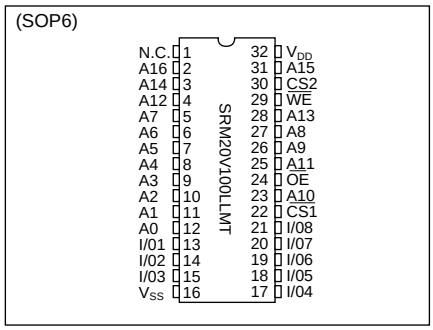
- Wide temperature range ..... –25 to 85°C
- Fast Access time ..... SRM20V100LLMX7 70ns (Max.)
- Low supply current ..... standby: 0.6µA (Typ.): LL Version
  0.3µA (Typ.): SL Version
  operation: 8mA/1MHz (Typ.)
- Completely static ..... No clock required
- Supply voltage..... 2.7V to 3.6V
- TTL compatible inputs and outputs
- 3-state output with wired-OR capability
- Non-volatile storage with back-up batteries
- Package ..... SRM20V100LLMX7 SOP6-32pin (plastic)
  SRM20V100LLTX7 TSOP (I)-32pin (plastic)
  SRM20V100LLRX7 TSOP (I)-32pin-R1 (plastic)
  SRM20V100LLKX7 Slim-TSOP (I)-32pin (plastic)
  SRM20V100LLYX7 Slim-TSOP (I)-32pin-R1 (plastic)

■ BLOCK DIAGRAM

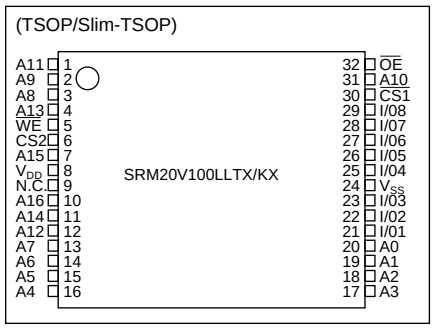


■ PIN CONFIGURATION

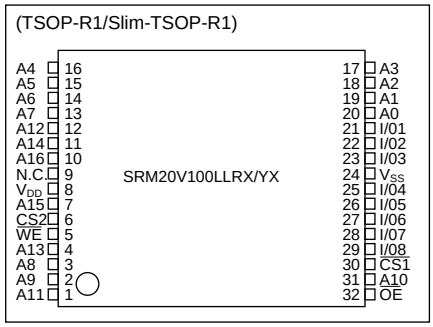
(SOP6)



(TSOP/Slim-TSOP)



(TSOP-R1/Slim-TSOP-R1)



¡ PIN DESCRIPTION

A0 to A16	Address Input
WE	Write Enable
OE	Output Enable
CS1, CS2	Chip Select
I/O1 to I/O8	Data I/O
VDD	Power Supply (2.7V to 3.6V)
VSS	Power Supply (0V)
N. C.	No connection

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	–0.5 to 4.6	V
Input voltage	V_I	–0.5 to V_{DD}+0.3	V
Input/Output voltage	$V_{I/O}$	–0.5 to V_{DD}+0.3	V
Power dissipation	P_D	0.5	W
Operating temperature	T_{opr}	–25 to 85	°C
Storage temperature	T_{stg}	–65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

*VI, VI/O (Min.) = –3.0V (Pulse width is 50ns)

■ DC RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V, Ta = –25 to 85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	—	2.7	3.0	3.6	V
	V_{SS}	—	0	0	0	V
Input voltage	V_{IH}	—	2.2	—	V_{DD}+0.3	V
	V_{IL}	—	–0.3*	—	0.4	V

*If pulse width is less than 50ns, it is –3.0V

■ ELECTRICAL CHARACTERISTICS

● DC Electrical Characteristics

(V_{DD} = 2.7 to 3.6V, V_{SS} = 0V, Ta = –25 to 85°C)

Parameter	Symbol	Conditions		Min.	Typ.*	Max.	Unit
Input leakage	I_{LI}	V_I=0 to V_{DD}		–1	—	1	µA
Output leakage	I_{LO}	$\overline{CS1}$ = V_{IH} or $\overline{CS2}$ = V_{IL} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, V_{IO} = 0 to V_{DD}		–1	—	1	µA
Standby supply current	I_{DDS}	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL}		—	—	1.0	mA
	I_{DDS1}	$\overline{CS1}$ = CS2≥V_{DD}—0.2V or CS2≤0.2V	LL	—	0.6	60	µA
			SL	—	0.3	30	
Average operating current	I_{DDA}	V_I = V_{IL}, V_{IH} $I_{I/O}$ = 0mA, t_{cyc} = Min.		—	20	35	mA
	I_{DDA1}	V_I = V_{IL}, V_{IH} $I_{I/O}$ = 0mA, t_{cyc} = 1µs		—	8	15	mA
Operating supply current	I_{DDO}	V_I = V_{IL}, V_{IH} $I_{I/O}$ = 0mA		—	8	15	mA
High level output voltage	V_{OH}	V_{DD}≥3V, I_{OH} = –2.0mA		2.4	—	—	V
		I_{OH} = –100µA		V_{DD}—0.2	—	—	
Low level output voltage	V_{OL}	V_{DD}≥3V, I_{OL} = –2.0mA		—	—	0.4	V
		I_{OL} = 100µA		—	—	0.2	

*Typical values are measured at Ta=25°C and V_{DD}=3.0V

● Terminal Capacitance

(f = 1MHz, Ta = 25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Address Capacitance	C_{ADD}	V_{ADD}=0V	—	—	8	pF
Input Capacitance	C_I	V_i=0V	—	—	8	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	—	10	pF

● AC Electrical Characteristics

❍Read Cycle

(V_{DD} = 2.7V to 3.6V, V_{SS} = 0V, Ta = –25 to 85°C)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Read cycle time	t_{RC}	∗1	70	—	ns
Address access time	t_{ACC}		—	70	ns
Chip select1 access time	t_{ACS1}		—	70	ns
Chip select2 access time	t_{ACS2}		—	70	ns
Output enable access time	t_{OE}		—	40	ns
Chip select1 output set time	t_{CLZ1}	∗2	5	—	ns
Chip select1 output floating	t_{CHZ1}		—	30	ns
Chip select2 output set time	t_{CLZ2}		5	—	ns
Chip select2 output floating	t_{CHZ2}		—	30	ns
Output enable output set time	t_{OLZ}		0	—	ns
Output enable output floating	t_{OHZ}		—	30	ns
Output hold time	t_{OH}	∗1	10	—	ns

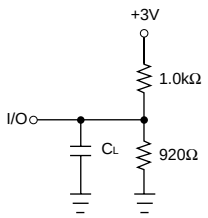
❍Write Cycle

(V_{DD} = 2.7V to 3.6V, V_{SS} = 0V, Ta = –25 to 85°C)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Write cycle time	t_{WC}	∗1	70	—	ns
Chip select time1	t_{CW1}		60	—	ns
Chip select time2	t_{CW2}		60	—	ns
Address enable time	t_{AW}		60	—	ns
Address setup time	t_{AS}		0	—	ns
Write pulse width	t_{WP}		55	—	ns
Address hold time	t_{WR}		0	—	ns
Input data setup time	t_{DW}		30	—	ns
Input data hold time	t_{DH}		0	—	ns
$\overline{WE}$ Output floating	t_{WHZ}	∗2	—	30	ns
$\overline{WE}$ Output setup time	t_{OW}		5	—	ns

*1 Test Conditions

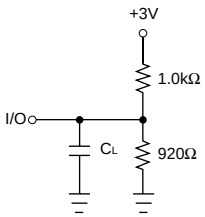
1. Input pulse level: 0.4V to 2.4V
2. $t_r = t_f$ = 5ns
3. Input and output timing reference levels : 1.5V
4. Output load C_L = 100pF



C_L=100pF (Includes Jig Capacitance)

*2 Test Conditions

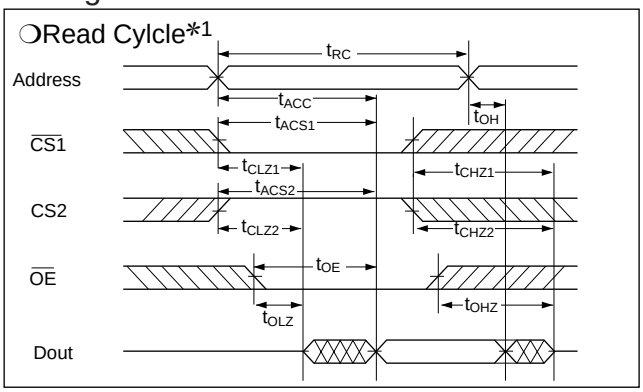
1. Input pulse level : 0.4V to 2.4V
2. $t_r = t_f$ = 5ns
3. Input timing reference levels: 1.5V
4. Output timing reference levels: ±200mV (the level displaced from stable output voltage level)
5. Output load C_L = 5pF



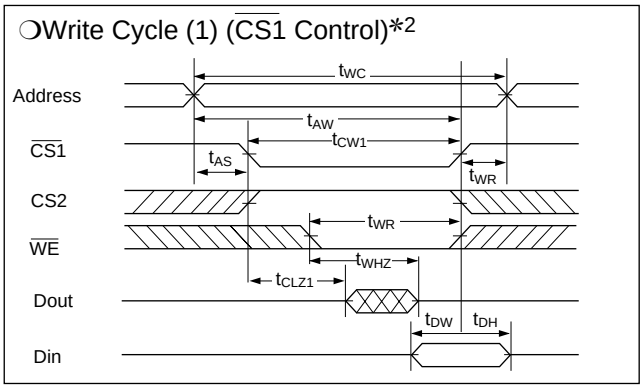
C_L=5pF (Includes Jig Capacitance)

● Timing chart

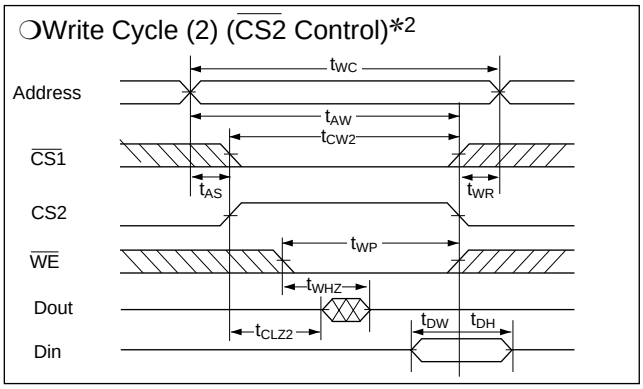
❍Read Cylcle*1



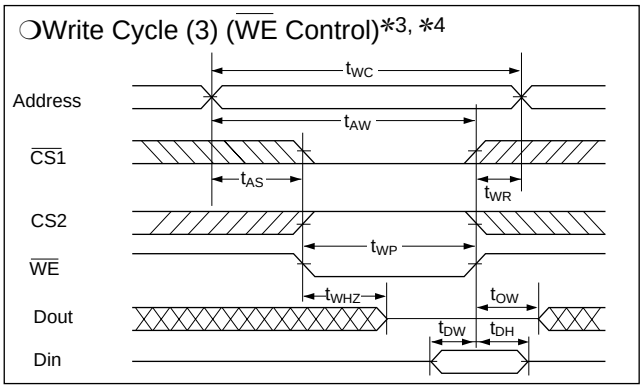
❍Write Cycle (1) (CS1 Control)*2



❍Write Cycle (2) (CS2 Control)*2



❍Write Cycle (3) (WE Control)*3, *4



Note : 1. During read cycle time, $\overline{WE}$ is to be "H" level.
2. During write cycle time that is controlled by $\overline{CS1}$ or CS2, Output Buffer is in high impedance state, whether $\overline{OE}$ level is "H" or "L".
3. During write cycle time that is controlled by $\overline{WE}$, Output Buffer is high impedance state if $\overline{OE}$ is "H" level.
4. When I/O terminals are output mode, be careful that do not give the opposite signals to the I/O terminals.

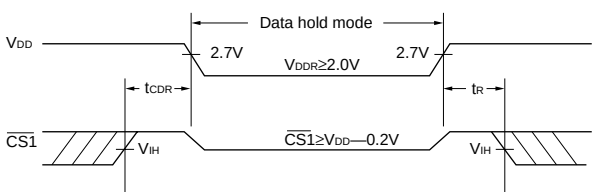
● DATA RETENTION CHARACTERISTIC WITH LOW VOLTAGE POWER SUPPLY

(V_{SS} = 0V, Ta = –25 to 85°C)

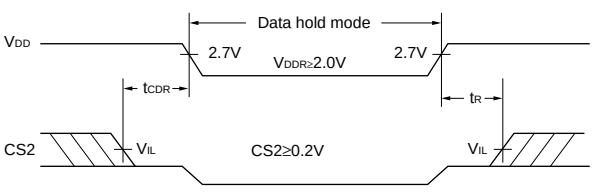
Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Data retention Supply voltage	V_{DDR}			2.0	—	3.6	V
Data retention current	I_{DDR}	V_{DD} = 2.7V $\overline{CS1}$ = CS2≥V_{DD}—0.2V or CS2≤0.2V	LL	—	0.5*	50	µA
			SL	—	0.25*	25	
Chip select data hold time	t_{CDR}			0	—	—	ns
Operation recovery time	t_R			5	—	—	ms

*Ta = 25°C

Data retention timing (CS1 Control)



Data retention timing (CS2 Control)



* when retaining data in standby mode, supply voltage can be lowered with in a certain range. But read or write cycle cannot be performed while the supply voltage is low.

■ FUNCTIONS

● Truth Table

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	DATA I/O	Mode	I_{DD}
H	X	X	X	Hi-Z	Unselected	I_{DDS}, I_{DDS1}
X	L	X	X	Hi-Z	Unselected	I_{DDS}, I_{DDS1}
L	H	X	L	Input data	Write	I_{DDO}
L	H	L	H	Output data	Read	I_{DDO}
L	H	H	H	Hi-Z	Output disable	I_{DDO}

X : "H" or "L"

● Reading data

Data is able to be read when the address is set while holding $\overline{CS1}$ = "L", CS2 = "H", $\overline{OE}$ = "L" and $\overline{WE}$ = "H". Since DATA I/O terminals are in high impedance state when $\overline{OE}$ = "H", the data bus line can be used for any other objective, then access time apparently is able to be cut down.

● Writing data

There are the following four ways of writing data into the memory.

(1) Hold CS2 = "H", $\overline{WE}$ = "L", set addresses and give "L" pulse to $\overline{CS1}$.

(2) Hold $\overline{CS1}$ = "L", $\overline{WE}$ = "L" ,set addresses and give "H"pulse to CS2.

(3) Hold $\overline{CS1}$ = "L", CS2 = "H", set addresses and give "L" pulse to $\overline{WE}$.

(4) After setting addresses, give "L" pulse to $\overline{CS1}$, $\overline{WE}$ and give "H" pulse to CS2.

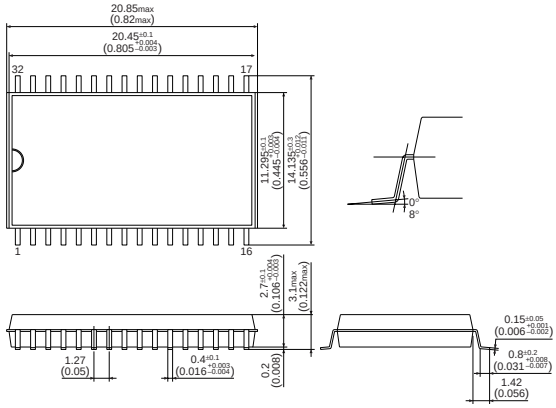
Anyway, data on the Data I/O terminals are latched up into the SRM20V100LLMX7 at the end of the period that $\overline{CS1}$, $\overline{WE}$ are "L" level, and CS2 is "H" level. As Data I/O terminals are in high impedance state when any of $\overline{CS1}$, $\overline{OE}$ = "H", or CS2 = "L", the contention on the data bus can be avoided.

● Standby mode

When $\overline{CS1}$ is "H" or CS2 is "L" level, the SRM20V100LLMX7 is in the standby mode which has retaining data operation. In this case Data I/O terminals are Hi-Z, and all inputs of addresses, $\overline{WE}$ and data can be any "H" or "L". When CS1 and $\overline{CS2}$ level are in the range over V_{DD}-0.2V, CS2 level is in the range under 0.2V, in the SRM20V100LLMX7 there is almost no current flow except through the high resistance parts of the memory.

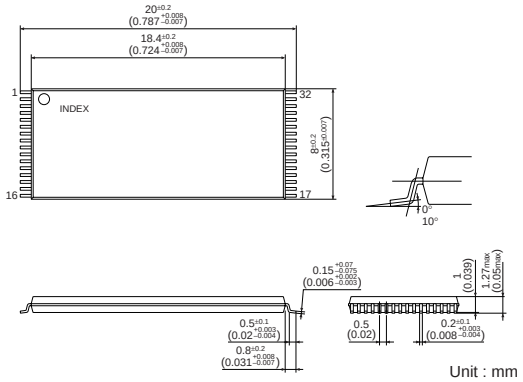
■ PACKAGE DIMENSIONS

Plastic SOP6-32pin



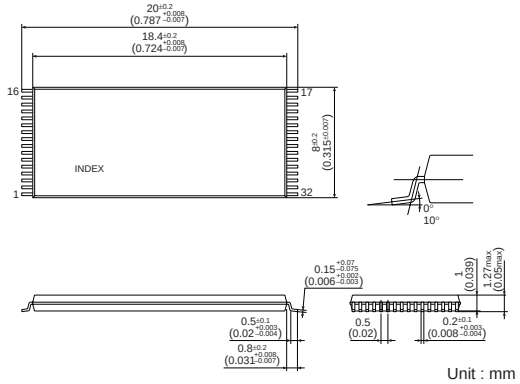
Unit : mm
(inch)

Plastic TSOP (I) -32pin



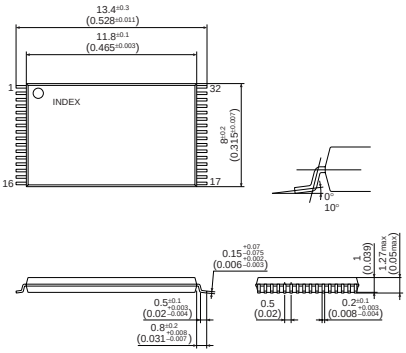
Unit : mm
(inch)

Plastic TSOP (I) -32pin-R1



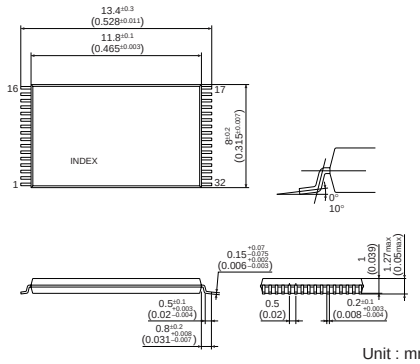
Unit : mm
(inch)

Plastic Slim-TSOP (I) -32pin



Unit : mm
(inch)

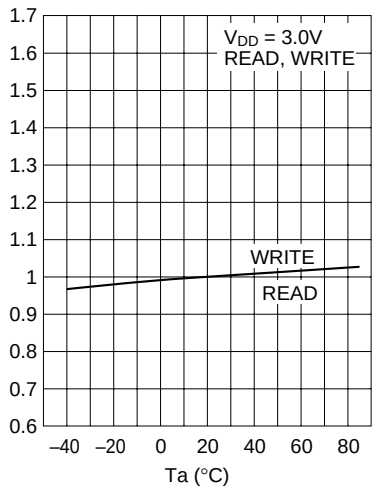
Plastic Slim-TSOP (I) -32pin-R1



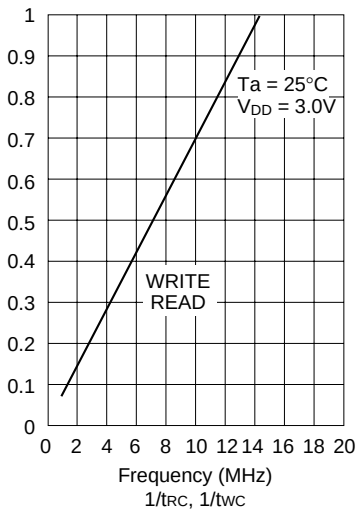
Unit : mm
(inch)

■ CHARACTERISTICS CURVES

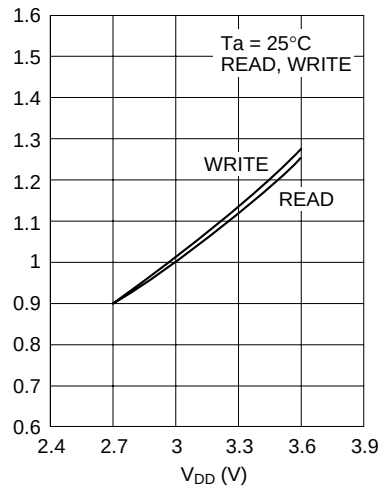
Normalized I_{DDA}–Ta



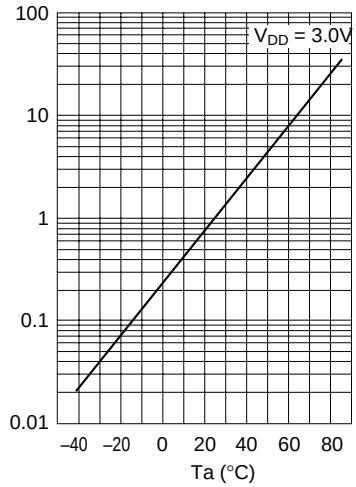
Normalized I_{DDA}–Frequency



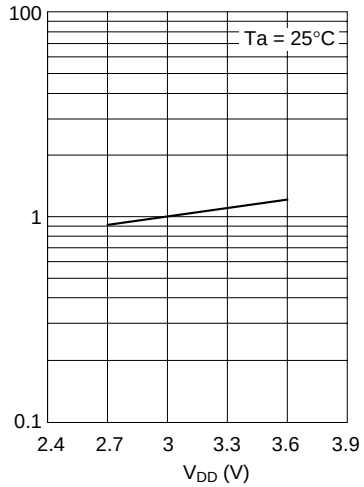
Normalized I_{DDA}–V_{DD}



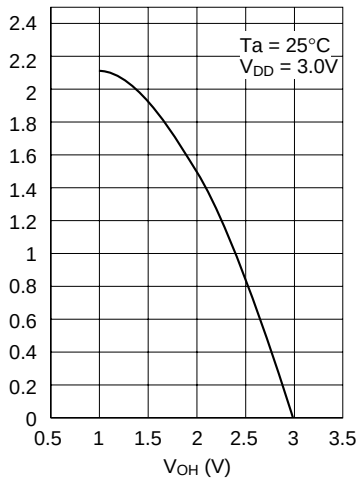
Normalized I_{DDS1}—Ta

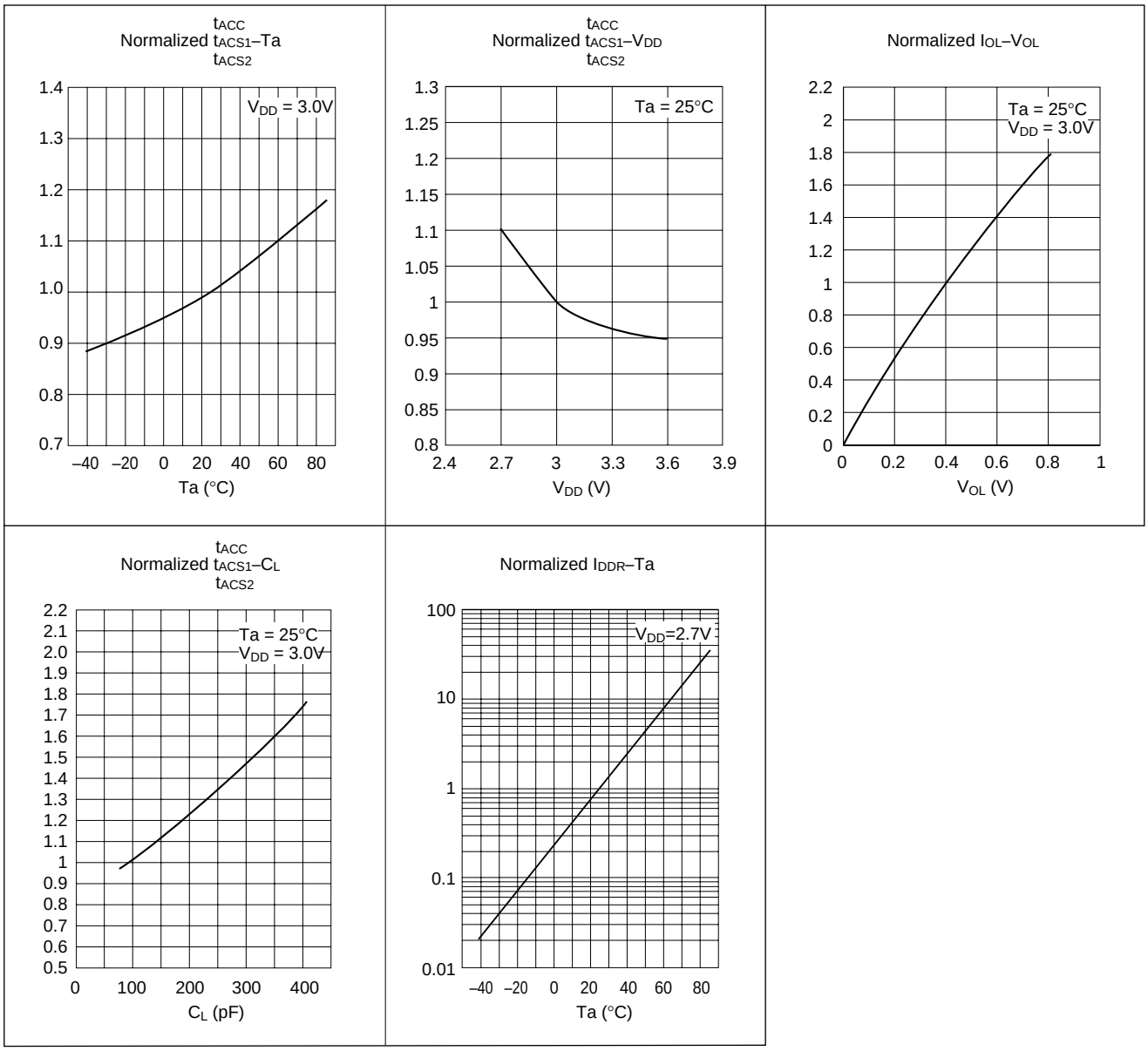


Normalized I_{DDS1}–V_{DD}



Normalized I_{OH}–V_{OH}





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