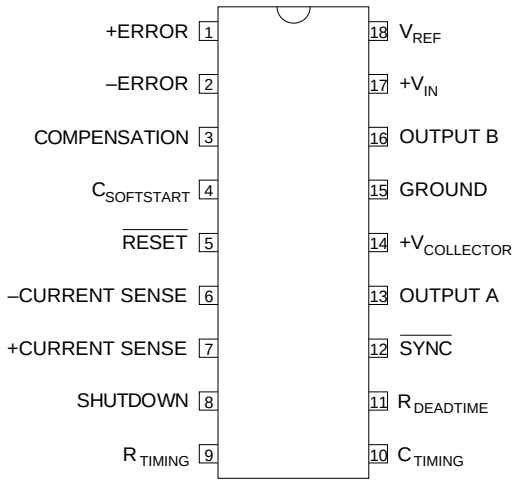
IP1526A SERIES

TOP VIEW



J Package – 18 Pin Ceramic DIP
N Package – 18 Pin Plastic DIP
D Package – 18 Pin Plastic (300) SOIC

Order Information

Part Number	J–Pack 18 Pin	N–Pack 18 Pin	D–18 18 Pin	Temp. Range
IP1526A	✔			-55 to +125°C
IP3526A	✔	✔	✔	0 to +70°C

Note:
To order, add the package identifier to the part number.
eg. IP1526AJ
IP3526AD–18

ADVANCED REGULATING PULSE WIDTH MODULATOR

FEATURES

- **Low drain current**
- **8 to 35V operation**
- **High performance 5V ±1% reference**
- **Low t.c. 1Hz to 400kHz oscillator range**
- **Dual 100mA source/sink outputs**
- **Digital current limiting**
- **Double pulse suppression**
- **Programmable deadtime**
- **Accurate current limit sense voltage**
- **Undervoltage lockout**
- **Single Pulse metering**
- **Programmable soft start**
- **Wide current limit common mode range**
- **TTL/CMOS compatible logic ports**
- **Symmetry correction capability**
- **Guaranteed 6 unit synchronisation**

ABSOLUTE MAXIMUM RATINGS (T_{case} = 25°C unless otherwise stated)

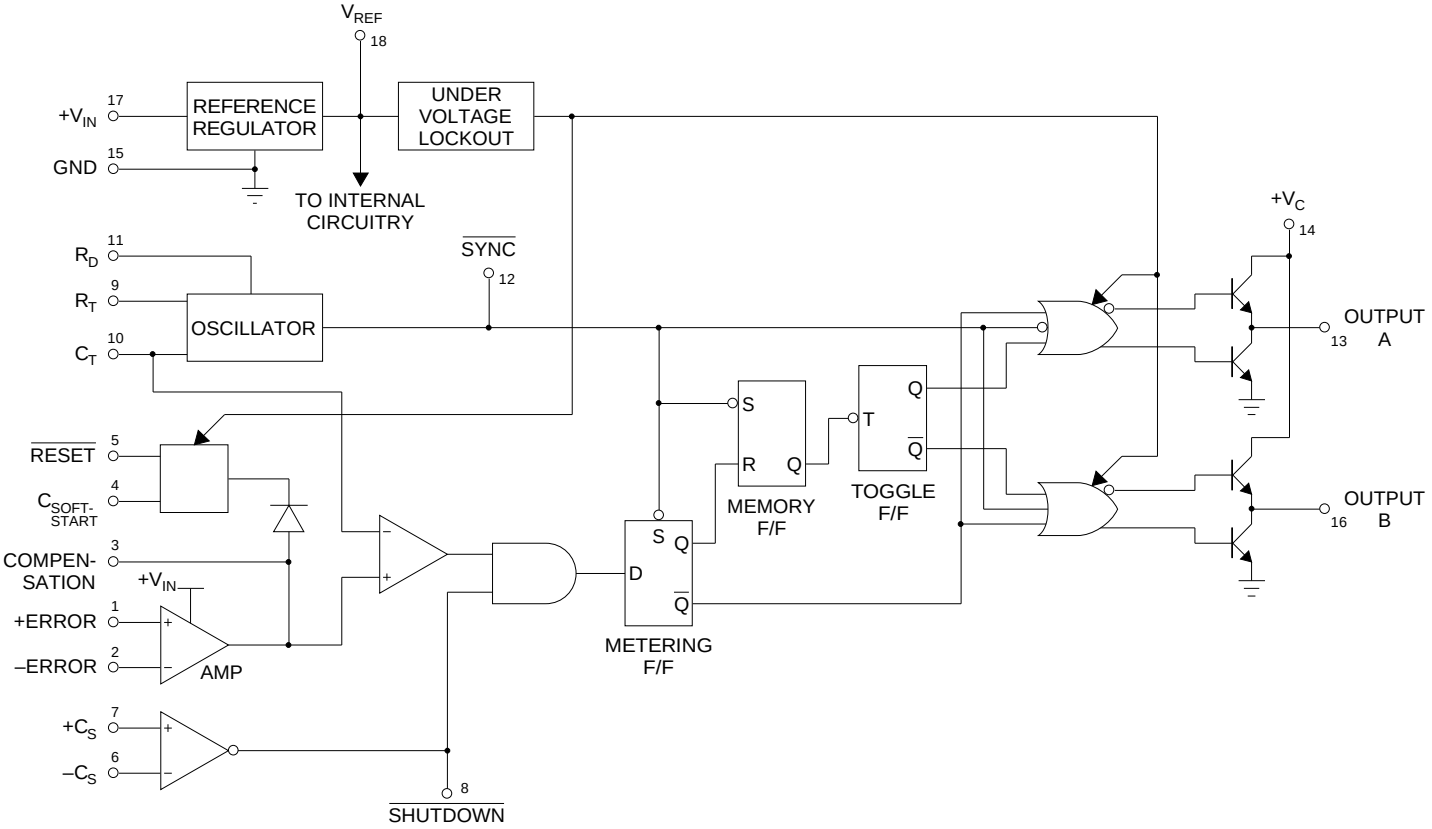
$+V_{IN}$	Input Voltage		+40V
	Collector Supply Voltage		+40V
	Logic Inputs		–0.3 to +5.5V
	Analogue Inputs		–0.3 to $+V_{IN}$
	Source / Sink Load Current	(Each output, continuous)	200mA
	Reference Load Current		Internally Limited
	Logic Sink Current		15mA
P_D	Power Dissipation	T_A = 25°C	1W
		Derate @ T_A > 50°C	10mW/°C
P_D	Power Dissipation	T_C = 25°C	3W
		Derate @ T_C > 25°C	24mW/°C
T_J	Operating Junction Temperature		See Ordering Information
T_{STG}	Storage Temperature Range		–65 to +150°C
T_L	Lead Temperature	(soldering, 10 seconds)	+300°C

IP1526A SERIES

DESCRIPTION

The IP1526A series of high performance pulse width modulator circuits is a direct replacement for the IP1526 series in all applications and features improved performance in several key areas. Functions included are a temperature compensated voltage reference, sawtooth oscillator, error amplifier, PWM comparator, pulse metering and steering logic, and two low impedance power drivers. Also included are protective features such as soft-start, undervoltage lockout, digital current limiting, double pulse inhibit, a data latch for single pulse metering, adjustable dead-time and provision for symmetry correction inputs. For ease of interface, all digital control ports are TTL and 9-series CMOS compatible. Active LOW logic design allows wired-OR connections for maximum flexibility. This versatile device can be used to implement single-ended or push-pull switching regulators of either polarity, both transformerless and transformer coupled .

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{IN}	Input Voltage		+8 to +35V
	Collector Voltage		+4.5 to +35V
	Sink/Source Load Current (Each Output)		0 to 100mA
	Reference Load Current		–5 to 20mA
	Oscillator Frequency Range		1Hz to 400kHz
R_T	Oscillator Timing Resistor		2kΩ to 150kΩ
C_T	Oscillator Timing Capacitor		470pF to 20µF
	Available Deadtime Range @ 40kHz		3% to 50%
	Operating Ambient Temperature Range	IP1526A	–55 to +125°C
		IP3526A	0 to +70°C

ELECTRICAL CHARACTERISTICS (T_J = Over Operating Temperature Range unless otherwise stated)

Parameter	Test Conditions	IP1526A			IP3526A			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
	REFERENCE SECTION							
Output Voltage	T_J = 25°C	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation	V_{IN} = 8 to 35V		2	10		2	15	mV
Load Regulation	I_L = –5 to 20mA		5	10		5	20	
Temperature Stability			15	50		15	50	mV
Total Output Voltage Range		4.9	5.0	5.1	4.85	5.0	5.15	V
Short Circuit Current	V_{REF} = 0	30	80	140	30	80	140	mA
	UNDERVOLTAGE LOCKOUT							
$\overline{\text{RESET}}$ Output Voltage	V_{REF} = 3.8V		0.2	0.4		0.2	0.4	V
	V_{REF} = 4.8V	2.4	4.8		2.4	4.8		
	OSCILLATOR SECTION [2]							
Initial Accuracy	T_J = 25°C		±3	±8		±3	±8	%
Voltage Stability	V_{IN} = 8 to 35V		0.5	1		0.5	1	
Temperature Stability			1	3		1	6	
Minimum Frequency	R_T = 150kΩ C_T = 0.2µF			100			100	Hz
Maximum Frequency	R_T = 2kΩ C_T = 470pF	400	700		400	700		kHz
Sawtooth Peak Voltage	V_{IN} = 35V		3	3.5		3	3.5	V
Sawtooth Valley Voltage	V_{IN} = 8V	0.3	1		0.3	1		
	ERROR AMPLIFIER SECTION [3]							
Input Offset Voltage	$R_S \leq 2k\Omega$		2	5		2	10	mV
Input Bias Current			–350	–1000		–350	–2000	nA
Input Offset Current			35	100		35	200	
DC Open Loop Gain	$R_L \geq 10M\Omega$	64	72		60	72		dB
High Output Voltage	$V_{PIN1} - V_{PIN2} \geq 150mV$ I_{SOURCE} = 100µA	3.6	4.2		3.6	4.2		V
Low Output Voltage	$V_{PIN1} - V_{PIN2} \geq 150mV$ I_{SINK} = 100µA		0.2	0.4		0.2	0.4	V
Common Mode Rejection	$R_S \leq 2k\Omega$	70	94		70	94		dB
Supply Voltage Rejection	V_{IN} = 12V to 18V	66	80		66	80		

NOTES

1. Test Conditions unless otherwise stated:
   V_{IN} = 15V
   T_J = –55 to +125°C for IP1526A
   T_J = 0 to +70°C for IP3526A
2. Oscillator / PWM Section Test Conditions:
   f_{OSC} = 40kHz
   (R_T = 4.12kΩ ±1% , C_T = 0.01µF ±1%, R_D = 0)
3. Error Amplifier Section Test Condition:
   V_{CM} = 0 to 5.2V

ELECTRICAL CHARACTERISTICS (T_J = Over Operating Temperature Range unless otherwise stated)

Parameter	Test Conditions	IP1526A			IP3526A			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
	PWM COMPARATOR [2]							
Minimum Duty Cycle	$V_{PIN2} - V_{PIN1} \geq 150mV$			0			0	%
Maximum Duty Cycle	$V_{PIN1} - V_{PIN2} \geq 150mV$	45	49		45	49		%
	DIGITAL PORTS (SYNC, SHUTDOWN & RESET)							
HIGH Output Voltage	I_{SOURCE} = 40µA	2.4	4.0		2.4	4.0		V
LOW Output Voltage	I_{SINK} = 3.6mA		0.2	0.4		0.2	0.4	V
HIGH Input Current	V_{IH} = 2.4V		-125	-200		-125	-200	µA
LOW Input Current	V_{IL} = 0.4V		-225	-360		-225	-360	µA
	CURRENT LIMIT COMPARATOR [4]							
Sense Voltage	$R_S \leq 50\Omega$	90	100	110	80	100	120	mV
Input Bias Current			-3	-10		-3	-10	µA
	SOFT–START SECTION							
Error Clamp Voltage	$\overline{RESET}$ = 0.4V		0.1	0.4		0.1	0.4	V
C_S Charging Current	$\overline{RESET}$ = 2.4V	50	100	150	50	100	150	µA
	OUTPUT DRIVERS (each output) [5]							
HIGH Output Voltage	I_{SOURCE} = 20mA	12.5	13.5		12.5	13.5		V
	I_{SOURCE} = 100mA	12	13		12	13		V
LOW Output Voltage	I_{SINK} = 20mA		0.2	0.3		0.2	0.3	V
	I_{SINK} = 100mA		1.2	2.0		1.2	2.0	V
Collector Leakage	V_C = 40V		50	150		50	150	µA
Rise Time	C_L = 1000pF		0.3	0.6		0.3	0.6	µs
Fall Time	C_L = 1000pF		0.1	0.2		0.1	0.2	µs
	POWER CONSUMPTION							
Standby Current	V_{IN} = 35V R_T = 4.12kΩ $\overline{SHUTDOWN}$ = 0.4V		14	20		14	20	mA

NOTES

1. Test Conditions unless otherwise stated:
   V_{IN} = 15V
   T_J = –55 to +125°C for IP1526
   T_J = 0 to +70°C for IP3526

2. Oscillator / PWM Section Test Conditions:
   f_{OSC} = 40kHz
   (R_T = 4.12kΩ , C_T = 0.01µF ±1%, R_D = 0)

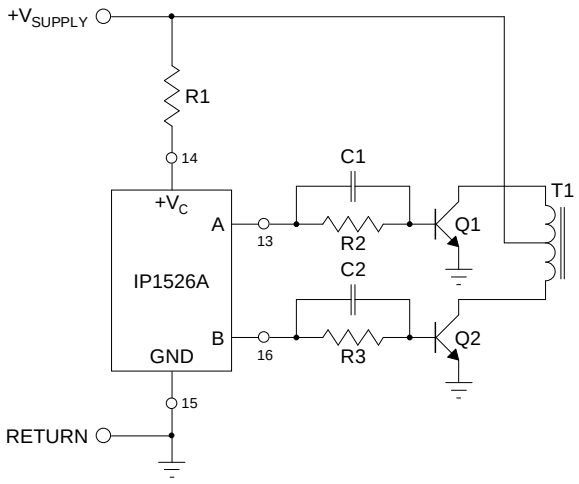
3. Error Amplifier Section Test Conditions:
   V_{CM} = 0 to 5.2V

4. Current Limit Comparator Section Test Conditions:
   V_{CM} = 0 to 12V

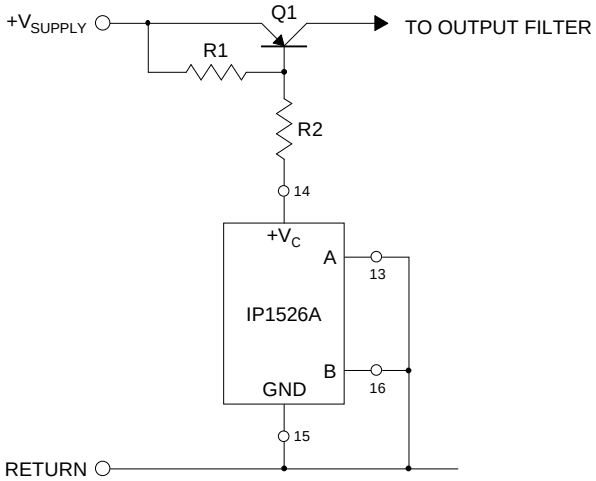
5. Output Driver Section Test Conditions:
   V_C = 15V unless otherwise stated.

APPLICATIONS INFORMATION

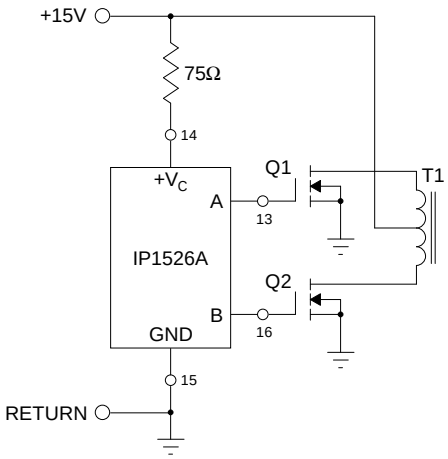
Push–Pull Configuration



Single–Ended Configuration

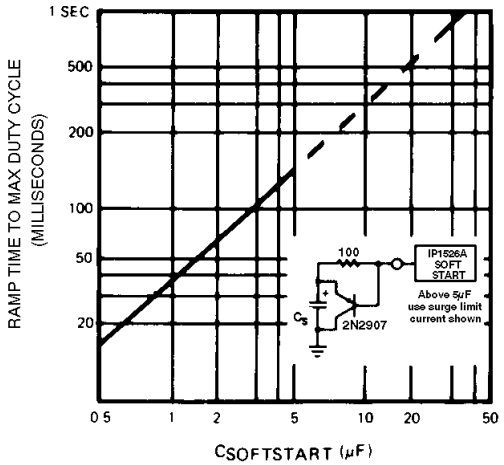


Driving N–Channel Power MOSFETs

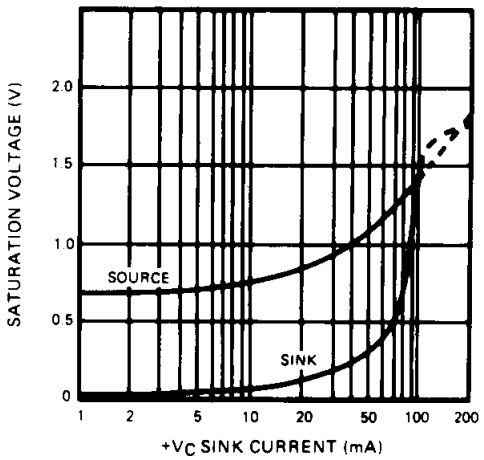


TYPICAL PERFORMANCE CHARACTERISTICS

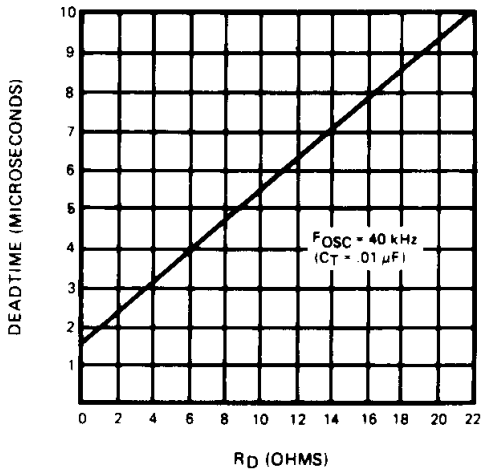
Soft Start Time vs C_S



Output Driver Saturation Voltage



Output Driver Deadtime vs R_D Value



Oscillator Period vs R_T and C_T