TC521000P/J

1MBit (256K x 4) Field Memory

PRELIMINARY

DESCRIPTION

The TC521000P/J is a CMOS 1Mbit Field Memory organized as 256K words by 4 bits, and features separate inputs/outputs, each equipped with an 8 bit serial shift register (32K words x 8 bit shift register x 4 bits), and also features high speed operation with a clock rate of 33MHz (serial cycle time: 30ns). The TC521000P/J is a high speed serial read/write memory with a random access capability per 8 words, and is suitable for use in field/frame memory in digital TV, VCR and other video spplications which require improvements in picture quality and enhancements in performance. The TC521000P/J is fabricated using TOSHIBA's CMOS silicon gate process technology as well as advanced circuitry to provide low power dissipation and wide operating margins.

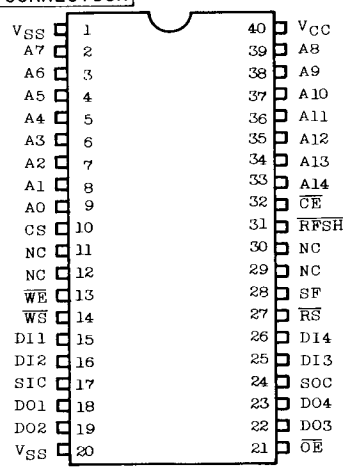
FEATURES

- High speed and low power

Serial Access Time		20ns
Serial Read Cycle Time		30ns
Serial Write Cycle Time		30ns
Read, Write Cycle Time		190ns
Read-Modify-Write Cycle Time		240ns
Read-Read-Write Cycle Time		480ns
Power Dissipation	Operating Power	550mW
	Standby Power	110mW

- Organization: 32K word × 8bit shift register × 4bit
- Single 5V power supply: 5V±10%
- On-chip 8bit shift registers
- Separate inputs and outputs
- Serial read/write, Read/Write, Read-Modify-Write, High Speed Read-Read-Write capability
- Random Access Capability per 8 word
- 8ms/512 refresh cycles
- On-chip refresh counter
- All inputs and outputs: TTL compatible
- Package: 40 pin 600mils wide standard plastic DIP

PIN CONNECTION

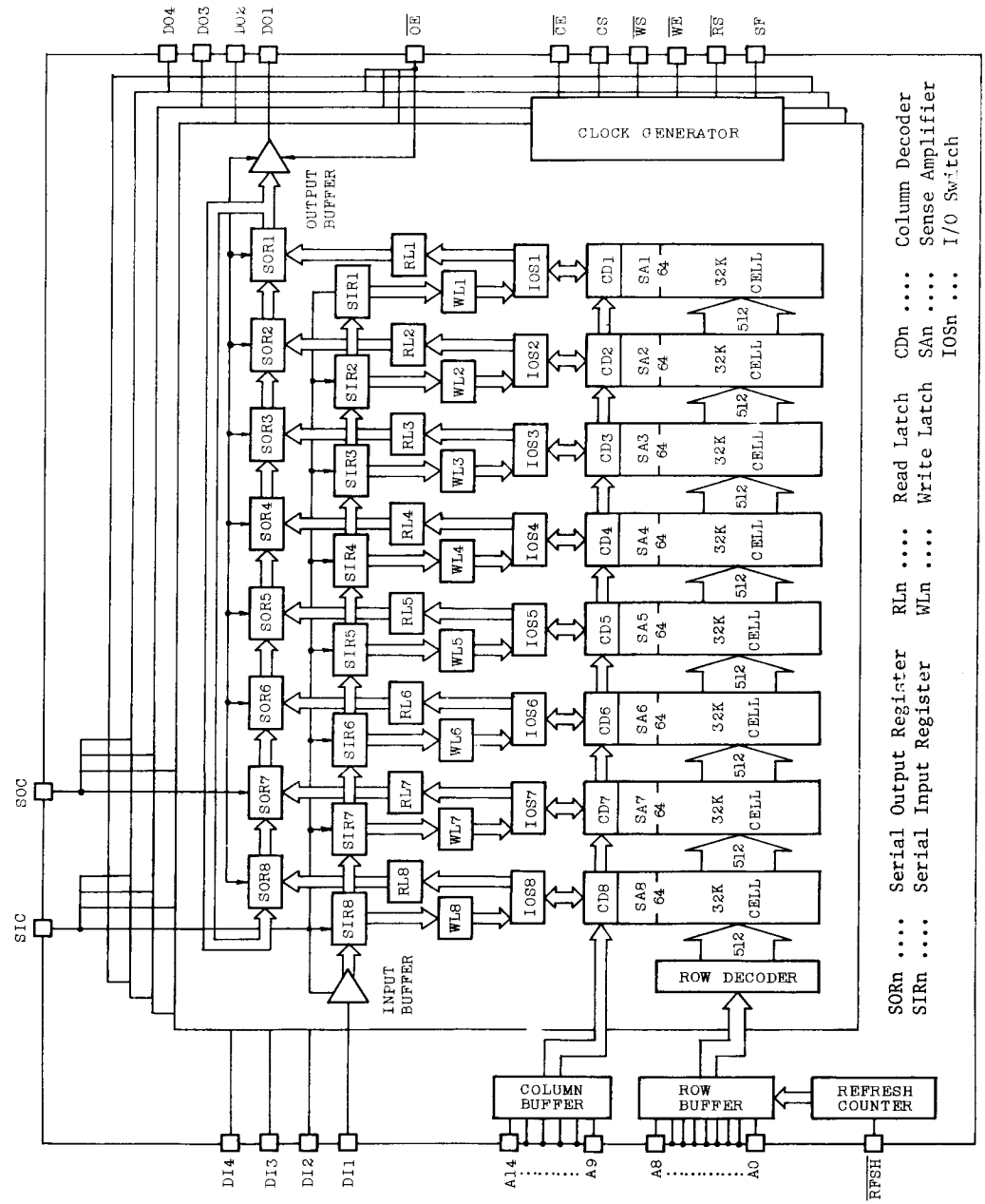


40-pin 600 mil DIP, 400 mil SOJ

PIN NAMES

SYMBOL	NAME
A0 ∿ A14	Address Input
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{WS}$	Write Strobe Input
$\overline{RS}$	Read Strobe Input
CS	Chip Select Input
SIC	Serial Input Clock Input
SOC	Serial Output Clock Input
DI1 ∿ DI4	Data Input
DO1 ∿ DO4	Data Output
$\overline{RFSH}$	Refresh Control Input
SF	Special Function Input
VCC	Ground (5V)
VSS	Ground (0V)
NC	Non Connection

BLCOK DIAGRAM



PIN NAMES AND FUNCTIONS

SYMBOL	NAME	FUNCTION
A0 ∿ A8	Row Address Inputs	Row Addresses
A9 ∿ A14	Column Address Inputs	Column Addresses The A14 is a column LSB address and is controlled internally by SF signal.
$\overline{CE}$	Chip Enable Input	The falling edge of $\overline{CE}$ latches the A0 ∿ A14 and CS. The read data is retained in Read Latch (RL), even if the $\overline{CE}$ goes high.
CS	Chip Select Input	The low CS forbid the memory cell access operation, but allows the refresh operation. ($\overline{CE}$ ONLY REFRESH)
$\overline{RS}$	Read Strobe Input	The $\overline{RS}$ controls the transfer operation to Output Shift Register from Read Latch (RL).
SF	Special Function	The SF controls the column LSB A14 internally.
$\overline{WS}$	Write Strobe Input	The $\overline{WS}$ controls the transfer operation to Write Latch (WL) from Input Shift Register.
$\overline{WE}$	Write Enable Input	The $\overline{WE}$ controls the write operation into the memory cell.
$\overline{OE}$	Output Enable Input	The $\overline{OE}$ enables the DO1 ∿ DO4 output buffers.
$\overline{RFSH}$	Refresh Control Input	The $\overline{RFSH}$ controls the auto refresh operation.
SOC	Serial Output Clock Input	The SOC is a shift clock input to Output Shift Register.
SIC	Serial Input Clock Input	The SIC is a shift clock input to Input Shift Register.
DO1 ∿ DO4	Data Outputs	Serial Output Terminals.
DI1 ∿ DI4	Data Inputs	Serial Input Terminals.

ABSOLUTE MAXIMUM RATINGS (Note: 1)

SYMBOL	ITEM	RATING	UNITS	NOTES
V_{IN}·V_{OUT}	Input • Output Voltage	-1 ∿ 7	V	2
V_{CC}	Power Supply Voltage	-1 ∿ 7	V	2
T_{opr}	Operating Temperature	0 ∿ 70	°C	
T_{stg}	Storage Temperature	-55 ∿ 150	°C	
T_{solder}	Soldering Temperature • Time	260 • 10	°C•sec	
P_D	Power Dissipation	1	W	
I_{OUT}	Short Circuit Output Current	50	mA	

RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	(10) TYP.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT ($\overline{CE}$, SIC, SOC Cycling: t_C, t_{SIC}, t_{SOC}=min.)	-	65	100	mA	3, 4
I_{CC2}	STANDBY CURRENT ($\overline{CE}$=$\overline{OE}$=V_{IH}, SIC=SOC=V_{IL})	-	3	20	mA	
I_{CC3}	REFRESH CURRENT ($\overline{RFSH}$ Cycling: t_{FC}=t_{FC} min.)	-	50	100	mA	3
$I_{I1(L)}$	INPUT LEAKAGE CURRENT (Except for SF Pin) (0V ≤ V_{IN} ≤ 6.5V, All other pins not under test=0V)	-10	-	10	µA	
$I_{I2(L)}$	INPUT LEAKAGE CURRENT (SF Pin ONLY) (0V ≤ V_{IN} ≤ 6.5V, All other pins not under test=0V)	-50	-	50	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (0V ≤ V_{OUT} ≤ V_{CC}, Output is disabled)	-10	-	10	µA	
V_{OH}	OUTPUT HIGH LEVEL VOLTAGE (I_{OUT}=-2mA)	2.4	-	-	V	
V_{OL}	OUTPUT LOW LEVEL VOLTAGE (I_{OUT}=2mA)	-	-	0.4	V	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTES
C_{I1}	Input Capacitance (A0 ∿ A14)	-	7	pF	
C_{I2}	Input Capacitance ($\overline{CE}$, $\overline{CS}$, $\overline{RS}$, $\overline{WS}$, $\overline{WE}$, $\overline{OE}$, SF, $\overline{RFSH}$, SIC, SOC)	-	7	pF	
C_{I3}	Input Capacitance (DI1 ∿ DI4)	-	7	pF	
C_O	Output Capacitance (DO1 ∿ DO4)	-	9	pF	

AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ∿ 70°C) (Note: 5, 6, 7)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTES
t_C	Read, Write Cycle Time	190		ns	
t_{RMW}	Read-Modify-Write Cycle Time (=8x t_{SOC}, t_{SIC})	240		ns	
t_{RRW}	Read-Read-Write Cycle Time (=16x t_{SOC})	480		ns	
t_{CE}	$\overline{CE}$ Pulse Width	100	2,000	ns	
t_P	$\overline{CE}$ Precharge Time	80		ns	
t_{ASC}	Address, CS Set-up Time	0		ns	
t_{AHC}	Address, CS Hold Time	50		ns	
t_{SOC}	Serial Output Cycle Time	30		ns	
t_{SO}	SOC Low Pulse Width	10		ns	
t_{SOP}	SOC High Pulse Width	10		ns	
t_{SOA}	SOC Access Time		20	ns	8
t_{SOH}	SOC Output Data Hold Time	5		ns	
t_{SIC}	Serial Input Cycle Time	30		ns	
t_{SI}	SIC Low Pulse Width	10		ns	
t_{SIP}	SIC High Pulse Width	10		ns	
t_{RCS}	Read Command Set-up Time	0		ns	
t_{RCH}	Read Command Hold Time	0		ns	
t_{CRD}	$\overline{CE}$-$\overline{RS}$ Delay Time	85		ns	
t_{RS}	$\overline{RS}$ Pulse Width	20		ns	
t_{RCP}	$\overline{RS}$-$\overline{CE}$ Precharge Time	0		ns	
t_{RSP}	$\overline{RS}$ Precharge Time	30		ns	
t_{SOS}	SOC-$\overline{RS}$ Set-up Time	0		ns	
t_{SOV}	SOC-$\overline{RS}$ Hold Time	15		ns	
t_{RSL}	SIC-$\overline{RS}$ Lead Time	0		ns	
t_{OE}	$\overline{OE}$ Pulse Width	30		ns	
t_{OEP}	$\overline{OE}$ Precharge Time	30		ns	
t_{OEA}	$\overline{OE}$ Access Time		25	ns	8
t_{OEZ}	$\overline{OE}$ Output Buffer Turn-off Delay Time	0	30	ns	9
t_{RWD}	$\overline{RS}$-$\overline{WE}$ Delay Time	0		ns	
t_{CWD}	$\overline{CE}$-$\overline{WE}$ Delay Time (Read-Modify-Write Cycle)	90		ns	
t_{WHC}	$\overline{WE}$ Hold Time	70		ns	
t_{WP}	$\overline{WE}$ Pulse Width	30		ns	
t_{CWL}	$\overline{WE}$-$\overline{CE}$ Lead Time	40		ns	

(Continued)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTES
t_{SWE}	$\overline{WS}$-$\overline{WE}$ Set-up Time	20		ns	
t_{WS}	$\overline{WS}$ Pulse Width	20		ns	
t_{WSP}	$\overline{WS}$ Precharge Time	30		ns	
t_{WIH}	$\overline{WS}$ Inhibit Time referenced to $\overline{WE}$	50		ns	
t_{WIHC}	$\overline{WS}$ Inhibit Time referenced to $\overline{CE}$	100		ns	
t_{SIV}	SIC-$\overline{WS}$ Set-up Time	5		ns	
t_{SIH}	SIC-$\overline{WS}$ Hold Time	10		ns	
t_{DS}	Data Input Set-up Time	5		ns	
t_{DH}	Data Input Hold Time	5		ns	
t_{SFS}	SF-$\overline{CE}$ Set-up Time	0		ns	
t_{SFH}	SF-$\overline{CE}$ Hold Time	0		ns	
t_{CSL}	SF-$\overline{CE}$ Lead Time (Read-Read-Write Cycle)	50		ns	
t_{SSH}	SOC-SF Hold Time (Read-Read-Write Cycle)	20		ns	
t_T	Transition Time (Rise and Fall)	3	50	ns	7
t_{REF}	Refresh Period		8	ms	
t_{FC}	Refresh Cycle Time	190		ns	
t_{CFD}	$\overline{CE}$ Precharge-$\overline{RFSH}$ Delay Time	80		ns	
t_{FAP}	$\overline{RFSH}$ Pulse Width	100	2,000	ns	
t_{FP}	$\overline{RFSH}$ Precharge Time	80		ns	
t_{FSC}	$\overline{RFSH}$ Precharge-$\overline{CE}$ Delay Time	80		ns	

Note

(1) Stress greater than those listed under "Absolute maximum ratings" may cause permanent damage to the device.

(2) All voltages are referenced to V_{SS}.

(3) I_{CC1} and I_{CC2} depend on cycle time. These values are specified at the condition of minimum cycle time.

(4) I_{CC1} depends on output loading. Specified value is obtained with the output open.

(5) An initial pause of 200μs is required after power up followed by 8 $\overline{CE}$ cycles before proper device operation is achieved. In case of using auto refresh, a minimum of 8 $\overline{RFSH}$ cycle are required.

(6) AC measurements assume t_T=5ns.

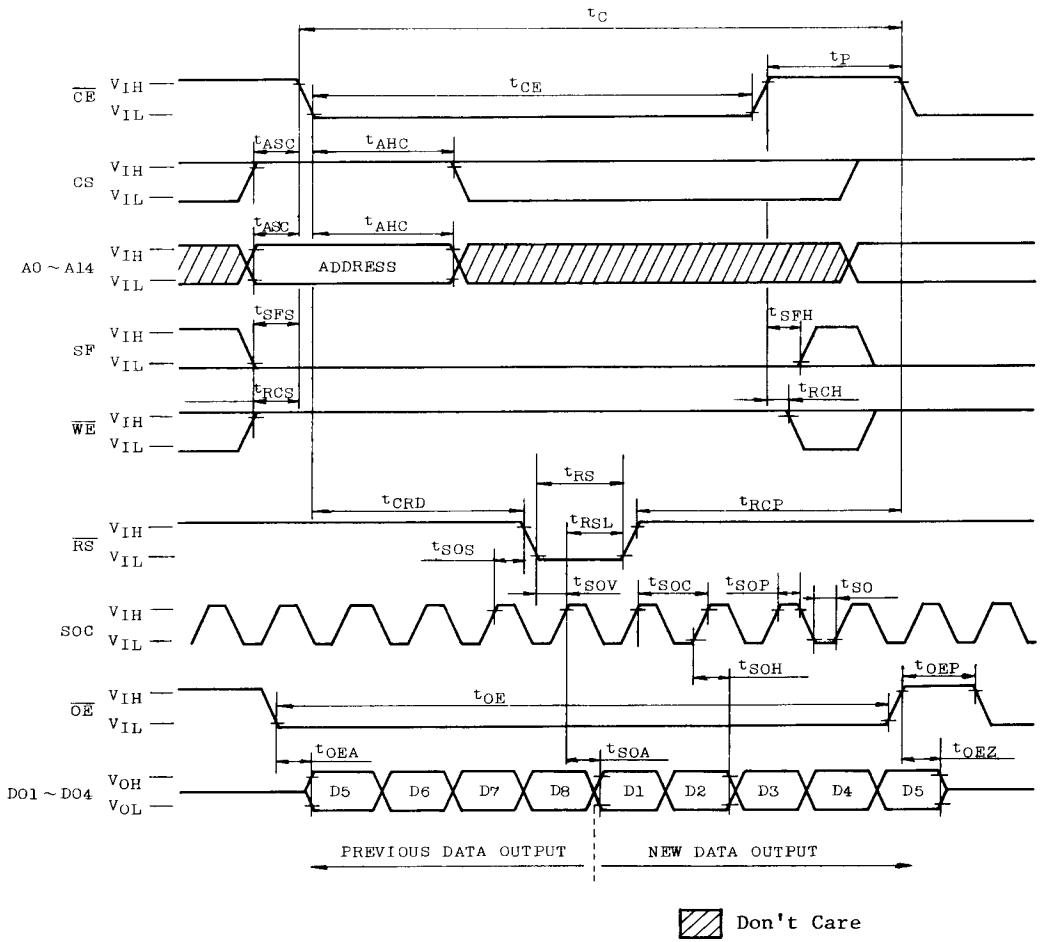
(7) V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} and V_{IL}.

(8) Output timings are measured with a load equivalent to 2 TTL load and 30pF. D_{OUT} comparate level: V_{OH}/V_{OL}=2.0V/0.8V

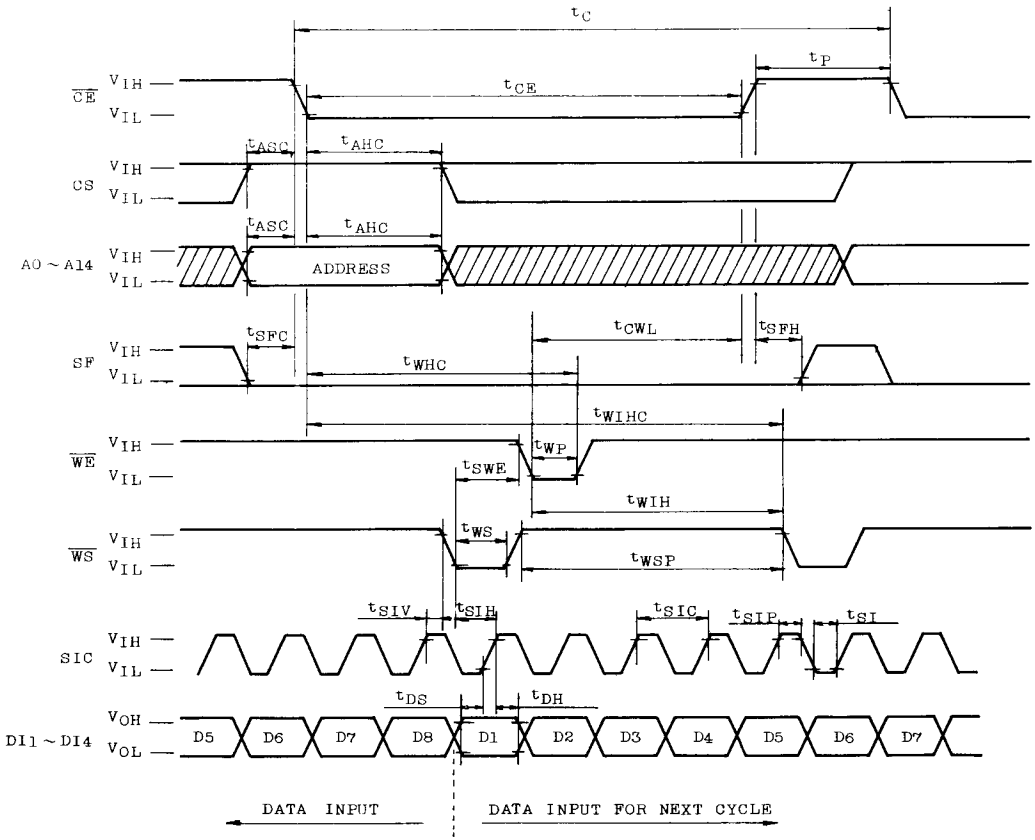
(9) t_{OEZ}(max.) defines the time at which the output achieve the open state.

(10) Typical values are at Ta=25°C and V_{CC}=5.0V.

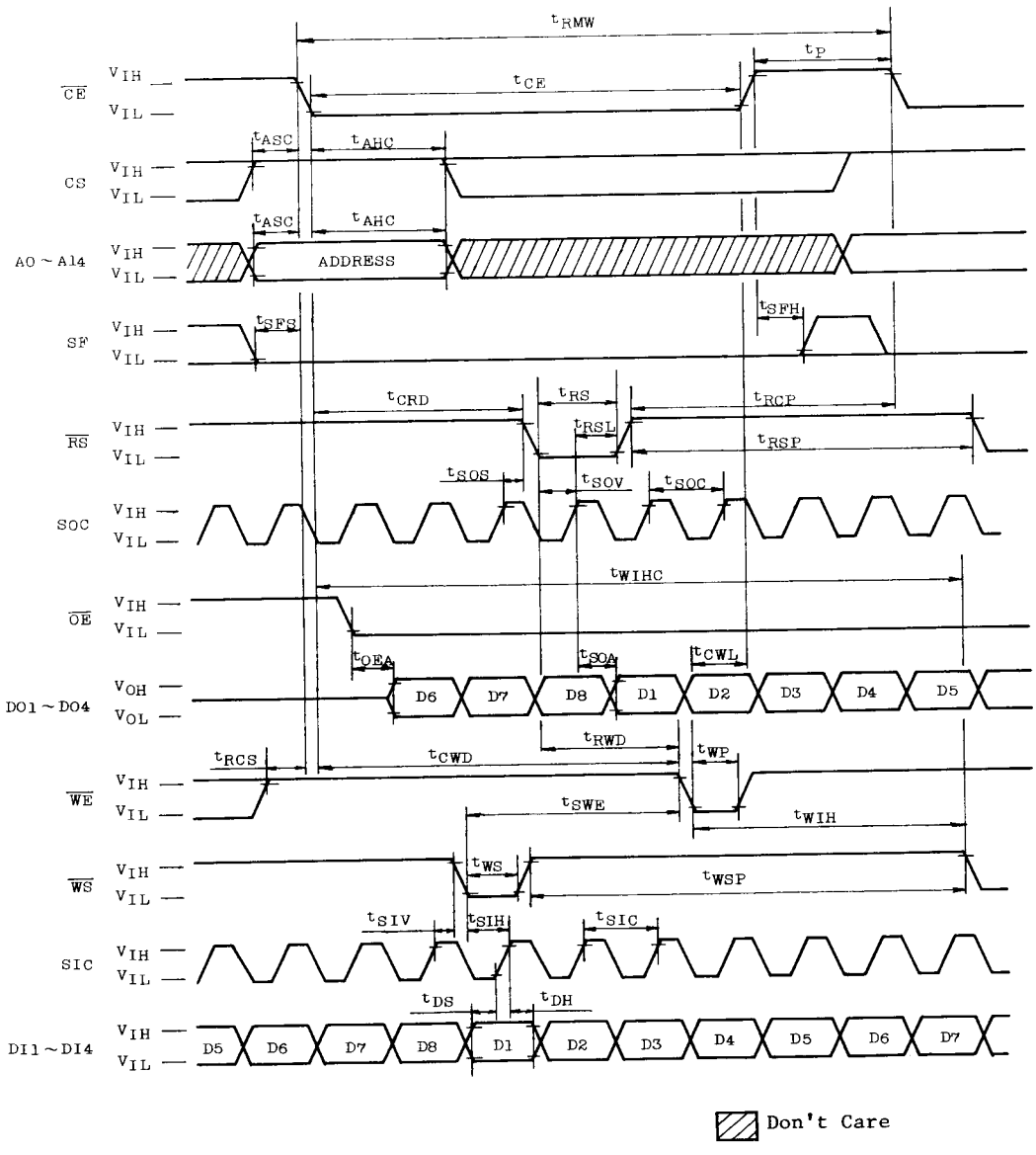
READ/SERIAL READ CYCLE



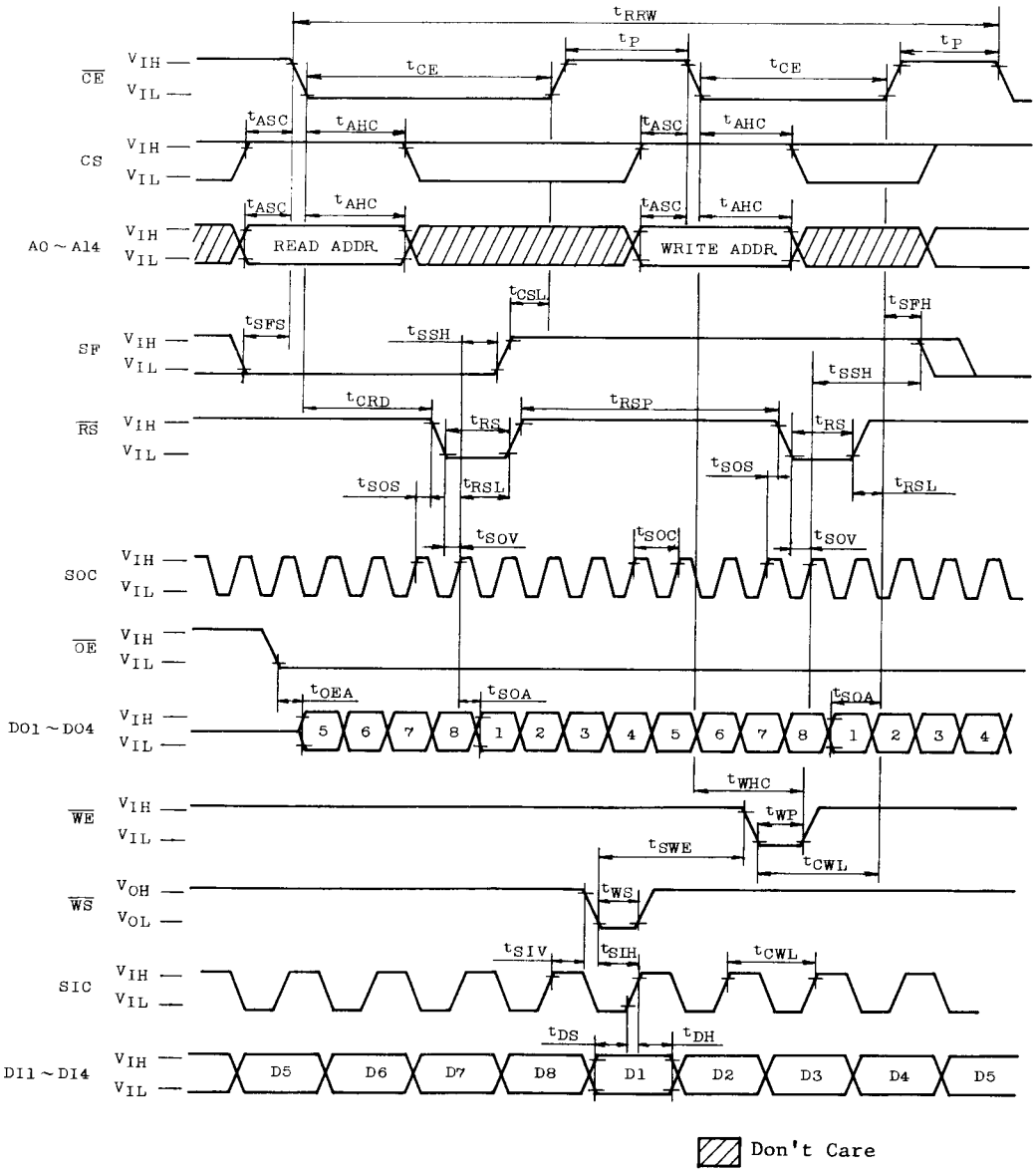
WRITE/SERIAL WRITE CYCLE



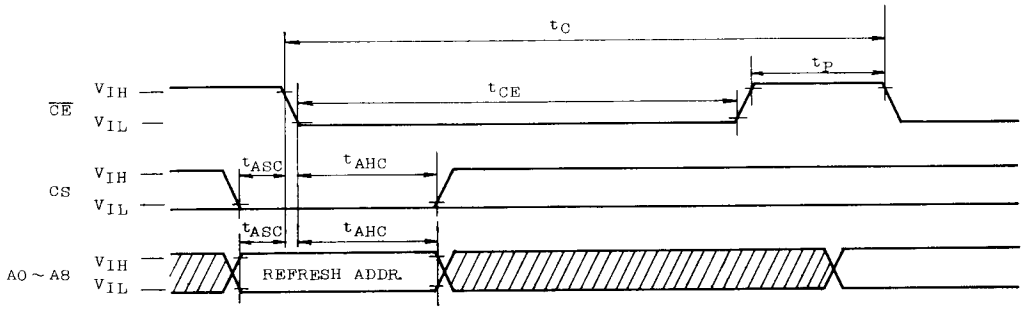
READ MODIFY WRITE CYCLE



READ-READ-WRITE CYCLE

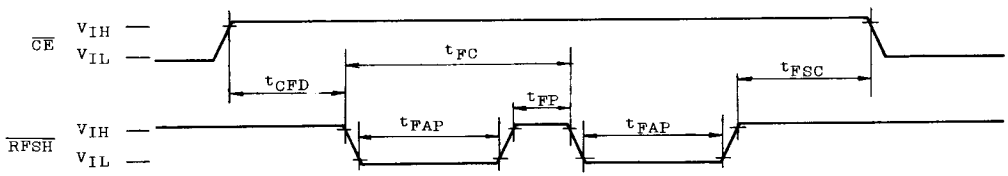


$\overline{CE}$ ONLY REFRESH



$\overline{WE}$, A9 ∿ 14 ..... Don't Care

$\overline{RFSH}$ AUTO REFRESH



$\overline{WE}$, A0 ∿ 14 ..... Don't Care

Don't Care

OPERATION INFORMATION

(1) READ/SERIAL READ CYCLE

i) SERIAL READ CYCLE (Refer to Fig. 1, 2)

[1] The read address is latched at the falling edge of $\overline{CE}$. The 8 bit data read out are transferred to and latched into the read latch (RL).

[2] The data latched at the RL are transferred to serial output register (SOR) at the first rising edge of SOC after the $\overline{RS}$ goes low.

[3] The 8 bit data transferred to the SOR are shifted and output sequentially synchronized with SOC from the first rising edge of SOC after the $\overline{RS}$ falls.

Fig.1 Block Diagram

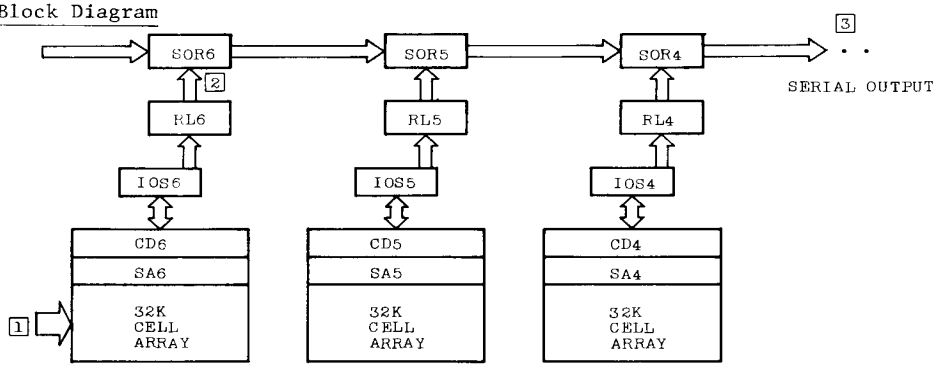
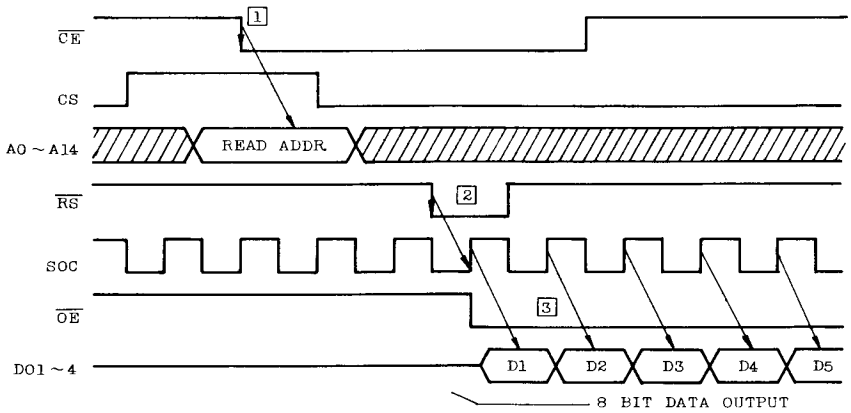


Fig.2 Timing Diagram



(2) WRITE/SERIAL WRITE CYCLE (Refer to Fig. 3, 4)

[1] The 8 bit input data are latched into the 8 bit serial input register (SIR) sequentially synchronized with SIC.

[2] The 8 bit input data latched into the SIR are transferred to the write latch (WL) at the falling edge of $\overline{WS}$.

[3] The write address is latched at the falling edge of $\overline{CE}$, same as read operation. Then the data stored in selected address to be written are read out and latched into the RL independent of this write operation, so the read data latched there can be read out through SOR by using $\overline{RS}$ and SOC (Read-Modify-Write).

[4] The 8 bit input data latched into the WL are written into the selected address location at the falling edge of $\overline{WE}$.

Fig.3 Block Diagram

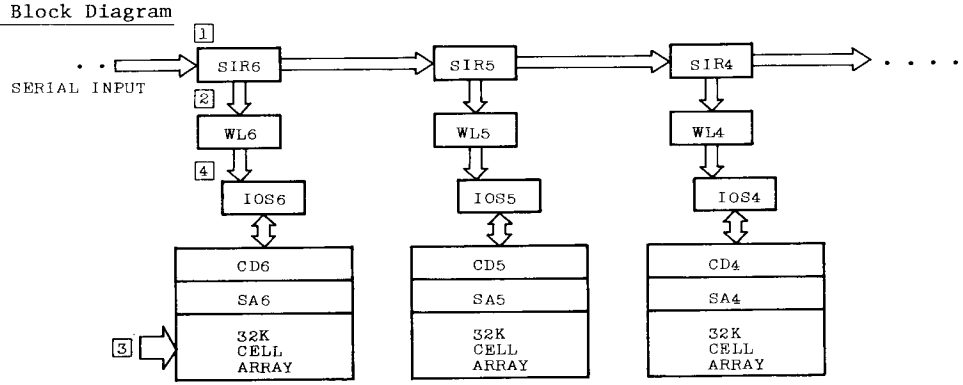
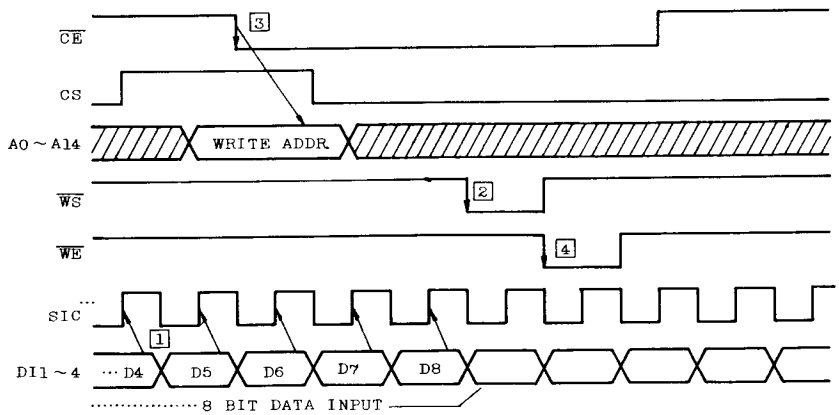


Fig.4 Timing Diagram



(3) READ-MODIFY-WRITE CYCLE

This operation is to execute write just after read in one $\overline{CE}$ cycle.

(4) READ-READ-WRITE CYCLE (Special operation) (Refer to Fig. 5, 6)

By using SF signal, three operations - the read operation for consecutive two address (16 bit data output) and write operation into the different address from read (8 bit data input) - can be performed asynchronously in two $\overline{CE}$ cycles (480ns). In this operation, the read start address must be even. This operation capability allows the field double scan in order to improve the picture quality in TV applications.

[1] The read address (even) is latched at the falling edge of $\overline{CE}$ under the condition of SF=low. Then the 8 bit read out data are transferred to and latched into the RL.

[2] The 8 bit data latched into the RL are transferred to SOR by the $\overline{RS}$, and then the data latched into the SOR are shifted and output from the first rising edge of SOC after the $\overline{RS}$ falls.

[3] Then when SF goes high, the LSB bit (A14) of coulumn addresses is changed to "1" from "0" automatically, and the data in the next column address are transferred to and latched into the RL.

[4] When the $\overline{CE}$ goes high, only memory cell array its peripheral area except for the latch and serial registers are placed in a precharge state. Then the data latched into the RL and SOR are maintained there, so the $\overline{WS}$ and $\overline{RS}$ can be input.

[5] On the other hand, the 8 bit input data are latched into the SIR sequentially synchronized with the SIC and then transferred to and latched into the WL by the $\overline{WS}$.

[6] The write address is latched at the falling edge of $\overline{CE}$, and then the data stored in the selected address is read out, but the data already latched into the RL are protected and retained there because of maintaining the SF "high".

[7] The 8 bit data latched into the RL (in [3]) are transferred to and latched into the SOR by the $\overline{RS}$.

[8] The 8 bit data latched into the WL (in [5]) are written into the selected cell locations by the $\overline{WE}$.

Fig.5 Block Diagram

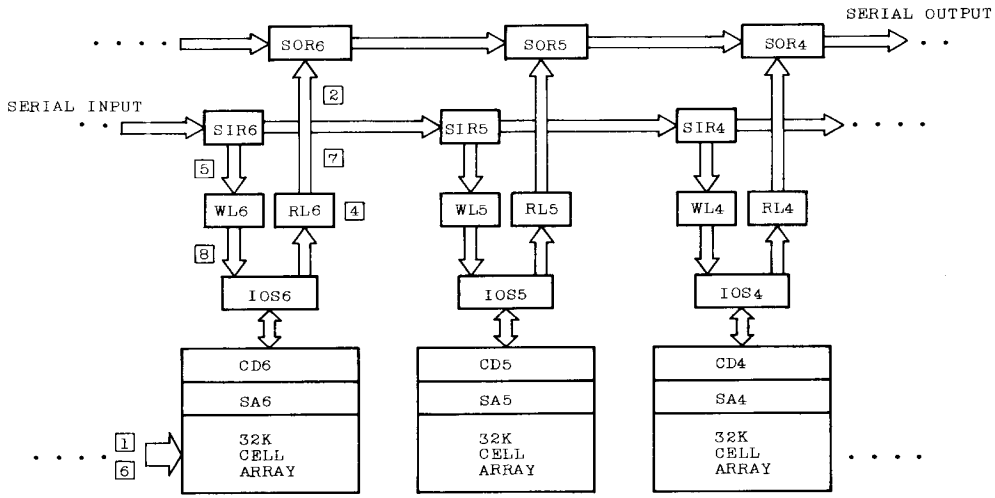
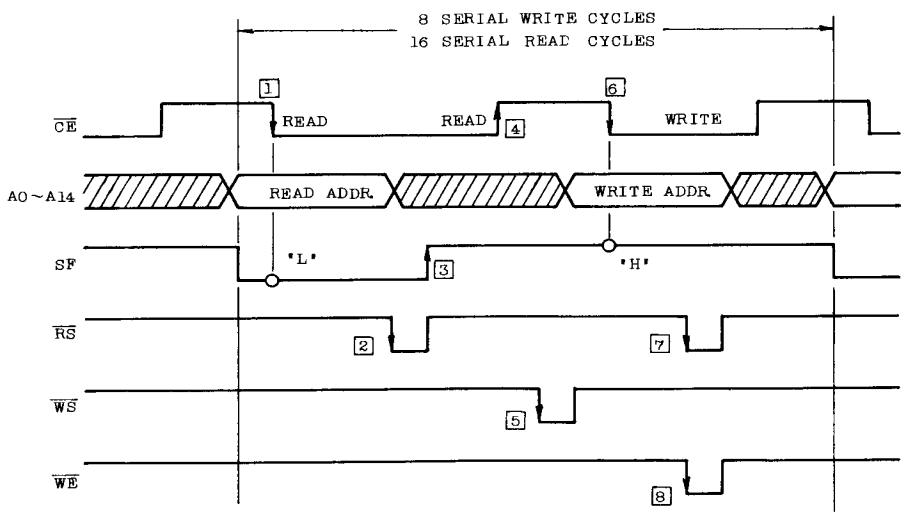


Fig.6 Timing Diagram



(5) REFRESH

The TC521000P/J's refresh period is 8ms/512 cycles.

The two types of refresh operation--$\overline{CE}$ only refresh and $\overline{RFSH}$ auto refresh--are allowed.

5-1: $\overline{CE}$ only refresh

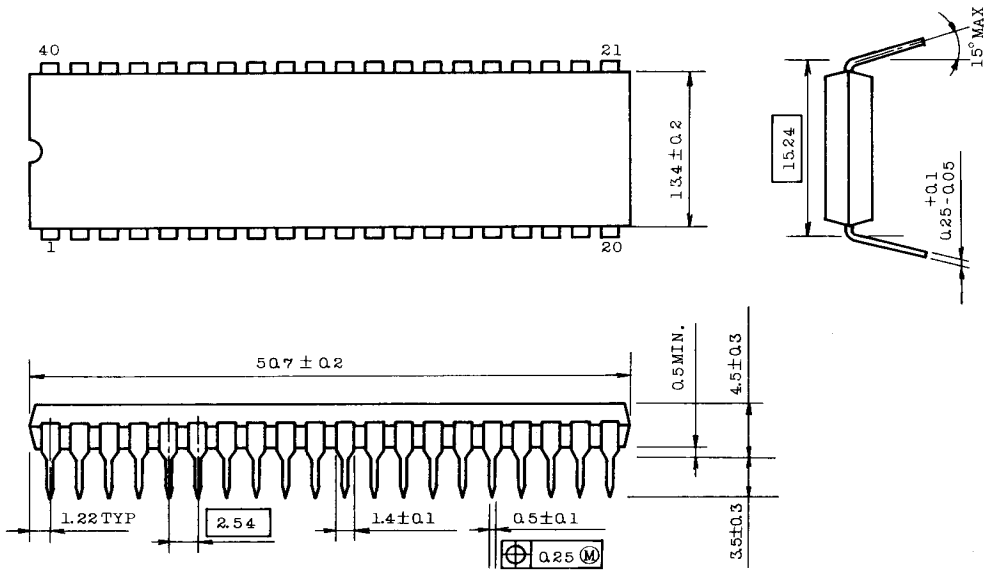
The refresh is accomplished by performing a $\overline{CE}$ cycle at each of the 512 ow address (A0-A8) within each 8ms time interval.

5-2: $\overline{RFSH}$ auto refresh

The RFSH auto refresh is available on the TC521000P/J. When the $\overline{RFSH}$ goes low under the condition of $\overline{CE}$=high, the on-chip refresh control clock generator and refresh address counters are enabled. Then, the refresh is accomplished by applying 512 clocks to the $\overline{RFSH}$ input within an 8ms time interval.

OUTLINE DRAWINGS DIP40-P-600

Unit in mm



Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their longitudinal position with respect to No.1 and No.40 leads.

o 400 mil SOJ package: