

TOSHIBA MOS MEMORY PRODUCTS

T-46-23-14

TC551001PL-70/PL-85/PL-10 TC551001FL-70/FL-85/FL-10

DESCRIPTION

The TC551001PL/FL is 1,048,576 bits static random access memory organized as 131,072 words by 8 bits using CMOS technology, and operated a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz(Typ.) and minimum cycle time of 70/85/100ns. When $\overline{CE1}$ is a logical high, or $CE2$ is low, the device is placed in low power standby mode in which standby current is 2 μ A typically. The TC551001PL/FL has three control inputs. Chip enable inputs ($\overline{CE1}$, $CE2$) allow for device selection and data retention control, and an output enable input (\overline{OE}) provides fast memory access. Thus the TC551001PL/FL is suitable for use in various microprocessor application system where high speed, low power, and battery back up are required.

The TC551001PL/FL is offered in both a dual-in-line 32 pin standard plastic package and small-out line plastic flat package.

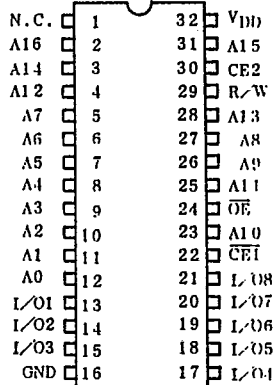
FEATURES

- Low Power Dissipation
27.5mW/MHz(Typ.)
- Standby Current: 100 μ A(Max.)
- 5V Single Power Supply
- Power Down Feature: $\overline{CE1}$, $CE2$

- Data Retention Supply Voltage: 2.0 ~ 5.5V
- Access Time

	TC551001 PL/FL-70	TC551001 PL/FL-85	TC551001 PL/FL-10
Access Time (Max.)	70ns	85ns	100ns
$\overline{CE1}$ Access Time (Max.)	70ns	85ns	100ns
$CE2$ Access Time (Max.)	70ns	85ns	100ns
\overline{OE} Access Time (Max.)	40ns	45ns	50ns

PIN CONNECTION (TOP VIEW)

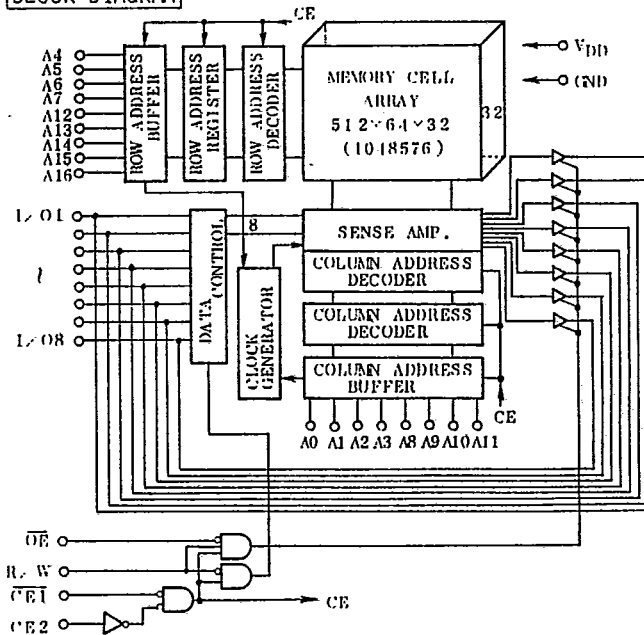


PIN NAMES

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
\overline{OE}	Output Enable Input
$\overline{CE1}$, $CE2$	Chip Enable Inputs
I/O1 ~ I/O8	Data Inputs/Outputs
VDD	Power (+5V)
GND	Ground
N.C.	No Connection

- Directly TTL Compatible: All Inputs and Outputs
- Plastic DIP and Plastic Flat Package

BLOCK DIAGRAM



TC551001PL-70/PL-85/PL-10
TC551001FL-70/FL-85/FL-10

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OPERATION MODE

OPERATION MODE	CE1	CE2	OE	R/W	I/O1 ~ I/O8	POWER
Read	L	H	L	H	DOUT	I _{DDO}
Write	L	H	*	L	DIN	I _{DDO}
Output Deselect	*	*	H	*	High-Z	I _{DDO}
Standby	H	*	*	*	High-Z	I _{DDS}
	*	L	*	*	High-Z	I _{DDS}

*: H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V _{IN}	Input Voltage	-0.3* ~ 7.0	V
V _{I/O}	Input and Output Voltage	-0.5 ~ V _{DD} +0.5	V
P _D	Power Dissipation	1.0/0.6**	W
T _{solder}	Soldering Temperature	260 ± 10	°C · sec
T _{strg.}	Storage Temperature	-55 ~ 150	°C
T _{opr.}	Operating Temperature	0 ~ 70	°C

*: -3.0V at pulse width 50ns MAX. **: SOP

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.2	-	V _{DD} +0.3	
V _{IL}	Input Low Voltage	-0.3 *	-	0.8	
V _{DH}	Data Retention Supply Voltage	2.0	-	5.5	

*: -3.0V at pulse width 50ns MAX.

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D.C. and OPERATING CHARACTERISTICS (Ta=0 ~ 70°C, VDD=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
IIL	Input Leakage Current	V _{IN} =0 ~ V _{DD}	-	-	±1.0	μA
IOH	Output High Current	V _{OH} =2.4V	-1.0	-	-	mA
IOL	Output Low Current	V _{OL} =0.4V	4.0	-	-	mA
I _{LO}	Output Leakage Current	$\overline{CE1}=V_{IH}$ or CE2=V _{IL} or $\overline{OE}=V_{IH}$, V _{OUT} =0 ~ V _{DD}	-	-	±1.0	μA
I _{DDO1}	Operating Current	$\overline{CE1}=V_{IL}$ and CE2=V _{IH} and R/W=V _{IH} , I _{OUT} =0mA Other Input=V _{IH} /V _{IL} t _{cycle} =Min. cycle	-	-	80	mA
I _{DDO2}		$\overline{CE1}=0.2V$ and CE2=V _{DD} -0.2V R/W=V _{DD} -0.2V, I _{OUT} =0mA Other Input=V _{DD} -0.2V/0.2V t _{cycle} =Min. cycle	-	-	70	mA
I _{DDS1}	Standby Current	$\overline{CE1}=V_{IH}$ or CE2=V _{IL}	-	-	3	mA
I _{DDS2}		$\overline{CE1}=V_{DD}-0.2V$ or CE2=0.2V V _{DD} =2.0V ~ 5.5V, Ta=0 ~ 70°C	-	-	100	μA

CAPACITANCE (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} =GND	10	pF
C _{OUT}	Output Capacitance	V _{OUT} =GND	10	

Note: This parameter periodically sampled is not 100% tested.

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TC551001FL-70/FL-85/FL-10

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A.C. CHARACTERISTICS (Ta=0~70°C, VDD=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC551001PL-70 TC551001FL-70		TC551001PL-85 TC551001FL-85		TC551001PL-10 TC551001FL-10		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	70	-	85	-	100	-	ns
t _{ACC}	Address Access Time	-	70	-	85	-	100	
t _{CO1}	CE1 Access Time	-	70	-	85	-	100	
t _{CO2}	CE2 Access Time	-	70	-	85	-	100	
t _{OE}	Output Enable to Output in Valid	-	40	-	45	-	50	
t _{COE}	Chip Enable (CE1, CE2) to Output in Low-Z	5	-	10	-	10	-	
t _{OEE}	Output Enable to Output in Low-Z	0	-	0	-	0	-	
t _{OD}	Chip Enable (CE1, CE2) to Output in High-Z	-	30	-	30	-	35	
t _{ODO}	Output Enable to Output in High-Z	-	30	-	30	-	35	
t _{OH}	Output Data Hold Time	10	-	10	-	10	-	

Write Cycle

SYMBOL	PARAMETER	TC551001PL-70 TC551001FL-70		TC551001PL-85 TC551001FL-85		TC551001PL-10 TC551001FL-10		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	70	-	85	-	100	-	ns
t _{WP}	Write Pulse Width	50	-	60	-	60	-	
t _{CW}	Chip Selection to End of Write	65	-	75	-	80	-	
t _{AS}	Address Set up Time	0	-	0	-	0	-	
t _{WR}	Write Recovery Time	0	-	0	-	0	-	
t _{ODW}	R/W to Output in High-Z	-	30	-	30	-	35	
t _{OEW}	R/W to Output in Low-Z	0	-	0	-	0	-	
t _{DS}	Data Set up Time	35	-	35	-	40	-	
t _{DH}	Data Hold Time	0	-	0	-	0	-	

A.C. TEST CONDITION

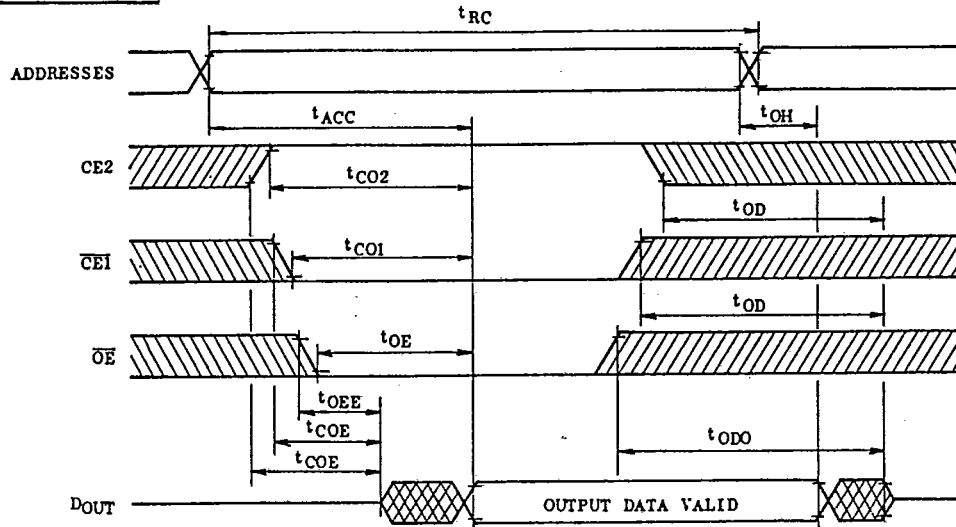
- Output Load : 100pF + 1 TTL Gate
- Input Pulse Level : 0.6V, 2.4V
- Timing Measurement V_{IN} : 0.8V, 2.2V
- Reference Levels V_{OUT} : 0.8V, 2.2V
- t_r, t_f : 5ns

TC551001PL-70/PL-85/PL-10
TC551001FL-70/FL-85/FL-10

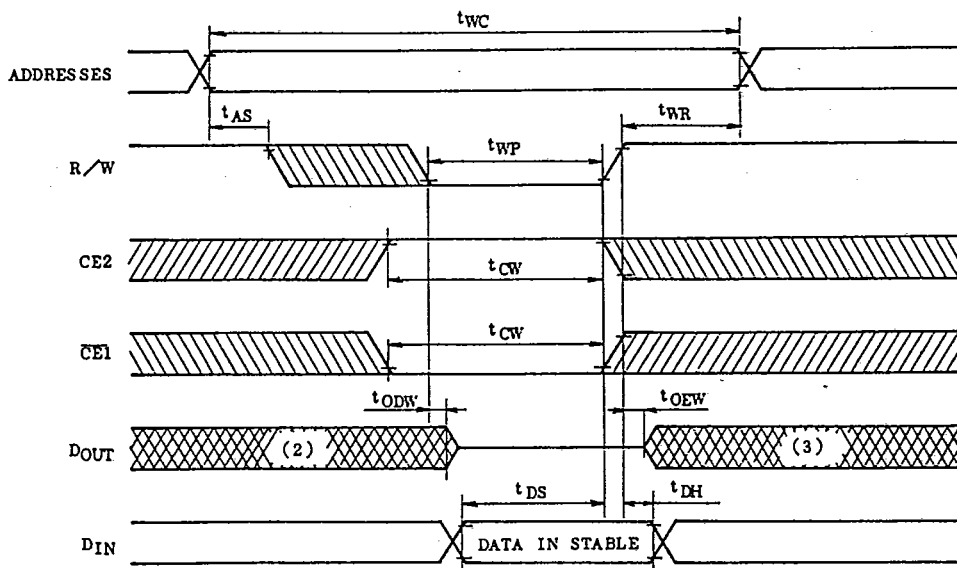
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TIMING WAVEFORMS

READ CYCLE (1)



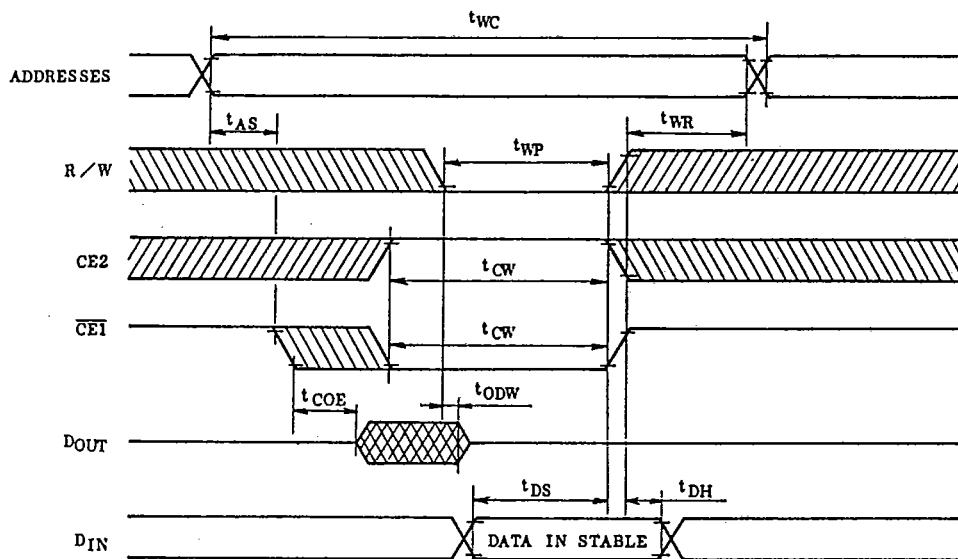
WRITE CYCLE 1 (4) (R/W Controlled Write)



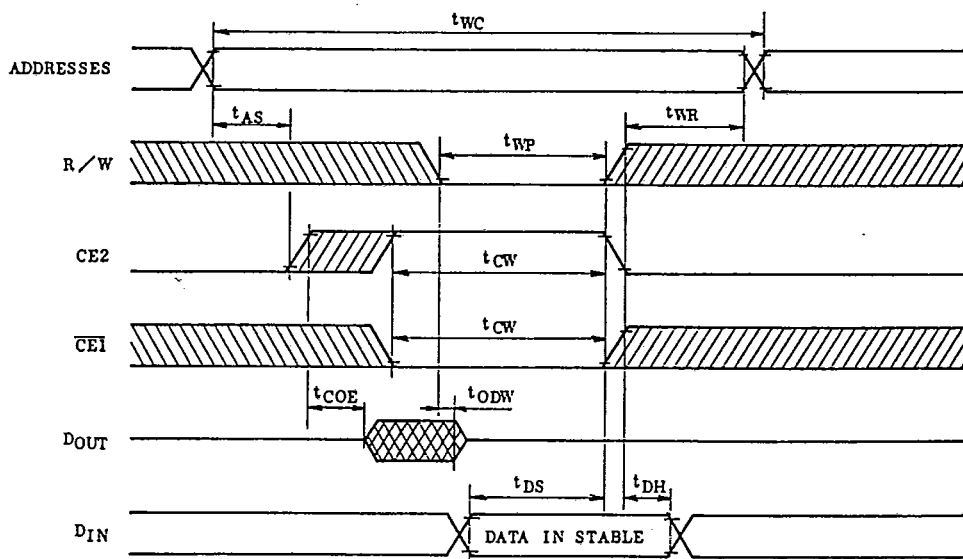
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WRITE CYCLE 2 (4) ($\overline{\text{CE1}}$ Controlled Write)



WRITE CYCLE 3 (4) (CE2 Controlled Write)

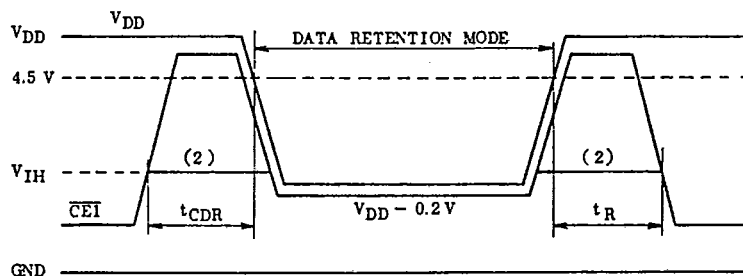


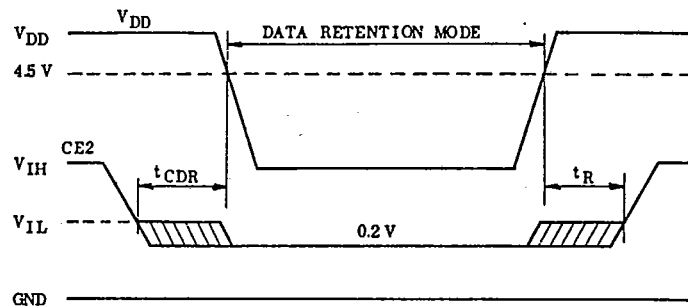
NOTE:

- (1) R/W is High for Read Cycle.
- (2) Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.
- (3) Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to R/W High transition, outputs remain in a high impedance state.
- (4) Assuming that \overline{OE} is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS ($T_a=0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage	2.0	-	5.5	V
I_{DD2}	Standby Current	$V_{DD}=3.0\text{V}$	-	50	μA
		$V_{DD}=5.5\text{V}$	-	100	
t_{CDR}	Chip Deselection to Data Retention Mode	0	-	-	nS
t_R	Recovery Time	5	-	-	mS

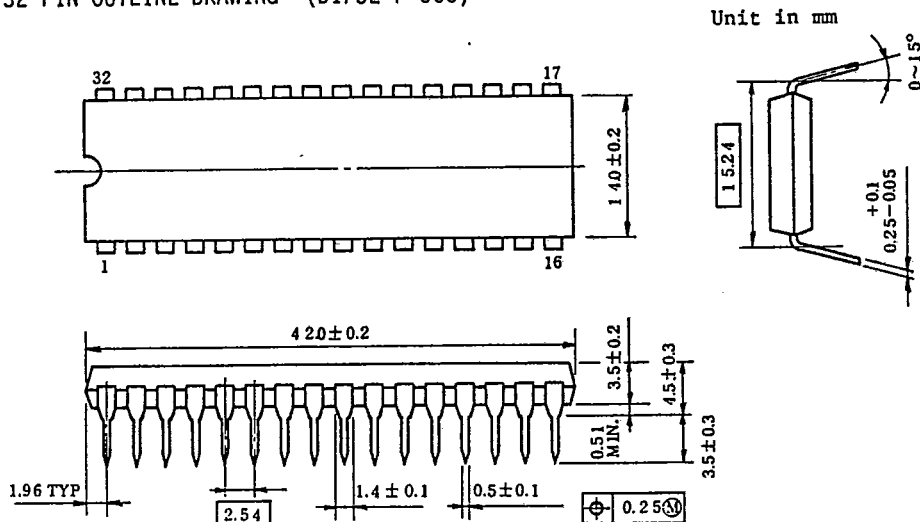
 $\overline{CE1}$ Controlled Data Retention Mode (1)

CE2 Controlled Data Retention Mode (3)

NOTE:

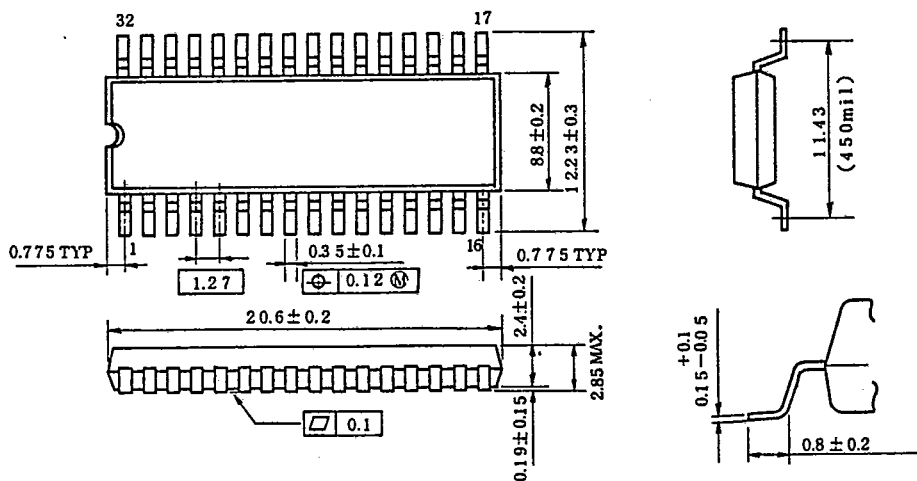
- (1) In $\overline{CE1}$ controlled data retention mode, minimum standby current mode is achieved under the condition of $CE2 \leq 0.2V$ or $CE2 \geq V_{DD}-0.2V$.
- (2) If the V_{IH} of $\overline{CE1}$ is 2.2V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4V, I_{DDs1} current flows.
- (3) In CE2 controlled data retention mode, minimum standby current mode is achieved under the condition of $CE2 \leq 0.2V$.

DIP 32 PIN OUTLINE DRAWING (DIP32-P-600)



Note) Package width and length do not include mold protrusion.
Allowable mold protrusion is 0.15mm.

MFP 32 PIN OUTLINE DRAWING (SOP32-P-450)



Note) Package width and length do not include mold protrusion.
Allowable mold protrusion is 0.15mm.